FEATURES

- Compliant with LIN 2.x/ISO 17987-4:2016 (12V)/SAE J2602
- AEC-Q100 qualified
- Compatible with K line
- Integrated over-temperature protection function (thermal shutdown)
- Integrated dominant time out function
- Integrated 30kΩ bus pull slave resistance
- Bus current limiting protection
- Supply undervoltage detection
- Very low power consumption sleep mode and standby mode
- Support remote wake-up
- Input level compatible with 3.3V/5V devices
- LIN data transmission rate up to 20kbps
- Available in QFN24L/DHVQFN24 package, small outline, no leads

PRODUCT APPEARANCE

Provide environmentally friendly lead-free package

DESCRIPTION

SIT1024Q is a four-channel Local Interconnect Network (LIN) physical layer transceiver that compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016 (12V) and SAE J2602 standards. It is mainly suitable for in-vehicle networks with a transmission rate of 1kbps to 20kbps. SIT1024Q controls the state of the LINx bus through the TXDx pin, and can convert the data stream sent by the protocol controller into a bus signal with the best slew rate and waveform shaping to minimize electromagnetic radiation emission (EME). The LIN bus output pin has an internal pull-up resistor. Only when used as a master node, the LIN bus port needs to be pulled up to V_{BATx} through an external resistor in series with a diode. SIT1024Q receives the data stream on the bus through the LINx pin, and transmits the data to the external microcontroller through the receiver's output pin RXDx.

SIT1024Q can operate from 5.5V to 27V and supports 12V applications. SIT1024Q has an extremely low quiescent current consumption in sleep mode and standby mode. It can quickly minimize power consumption in the event of a failure. The device can be placed in normal mode via a signal on the pin SLPx_N.

PIN CONFIGURATION

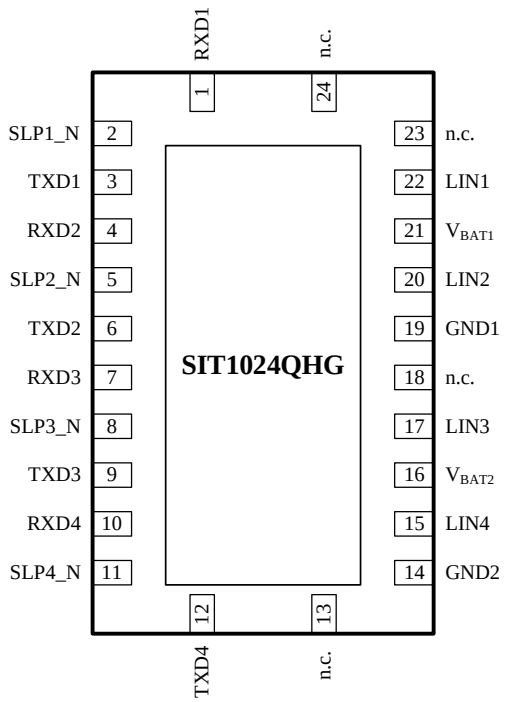


Fig 1 SIT1024QHG pin configuration diagram

PIN DESCRIPTION

Table 1 SIT1024Q pin description

Pin	Symbol	Description
1	RXD1	Receive data output 1 (open-drain); active LOW after a wake-up event.
2	SLP1_N	Enable input 1, high level enables devices into Normal mode, low level enables devices Sleep mode, reset the wake-up request on RXD1.
3	TXD1	Transmit data input 1.
4	RXD2	Receive data output 2 (open-drain); active LOW after a wake-up event.
5	SLP2_N	Enable input 2, high level enables devices into Normal mode, low level enables devices Sleep mode, reset the wake-up request on RXD2.
6	TXD2	Transmit data input 2.
7	RXD3	Receive data output 3 (open-drain); active LOW after a wake-up event.
8	SLP3_N	Enable input 3, high level enables devices into Normal mode, low level enables devices Sleep mode, reset the wake-up request on RXD3.
9	TXD3	Transmit data input 3.
10	RXD4	Receive data output 4 (open-drain); active LOW after a wake-up event.

Pin	Symbol	Description
11	SLP4_N	Enable input 4, high level enables devices into Normal mode, low level enables devices Sleep mode, reset the wake-up request on RXD4.
12	TXD4	Transmit data input 4.
13	n.c.	Not connected.
14	GND2	Ground connection for LIN3 and LIN4.
15	LIN4	LIN bus line 4 input/output.
16	V_{BAT2}	Battery supply for LIN3 and LIN4.
17	LIN3	LIN bus line 3 input/output.
18	n.c.	Not connected.
19	GND1	Ground connection for LIN1 and LIN2.
20	LIN2	LIN bus line 2 input/output.
21	V_{BAT1}	Battery supply for LIN1 and LIN2.
22	LIN1	LIN bus line 1 input/output.
23	n.c.	Not connected.
24	n.c.	Not connected.

NOTE: In the QFN24L/DHVQFN24 package, the exposed pad is connected to the GND pin of the chip. In order to obtain enhanced thermal and electrical performance, the exposed pad should be connected to a suitable "ground" on the PCB board.

LIMITING VALUES

Parameter	Symbol	Conditions	Range	Unit
Supply voltage	V_{BAT}	V_{BAT1} and V_{BAT2}, with respect to GND	-0.3 ~ +42	V
Voltage on pin TXD	V_{TXD}	TXD1 ~ TXD4	-0.3 ~ +7	V
Voltage on pin RXD	V_{RXD}	RXD1 ~ RXD4	-0.3 ~ +7	V
Voltage on pin SLP_N	V_{SLP_N}	SLP1_N ~ SLP4_N	-0.3 ~ +7	V
Voltage on pin LIN	V_{LIN}	LIN1 ~ LIN4, with respect to GND	-42 ~ +42	V
Virtual junction temperature	T_j		-40 ~ +150	°C
Storage temperature	T_{stg}		-55 ~ +150	°C

NOTE: The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

BLOCK DIAGRAM

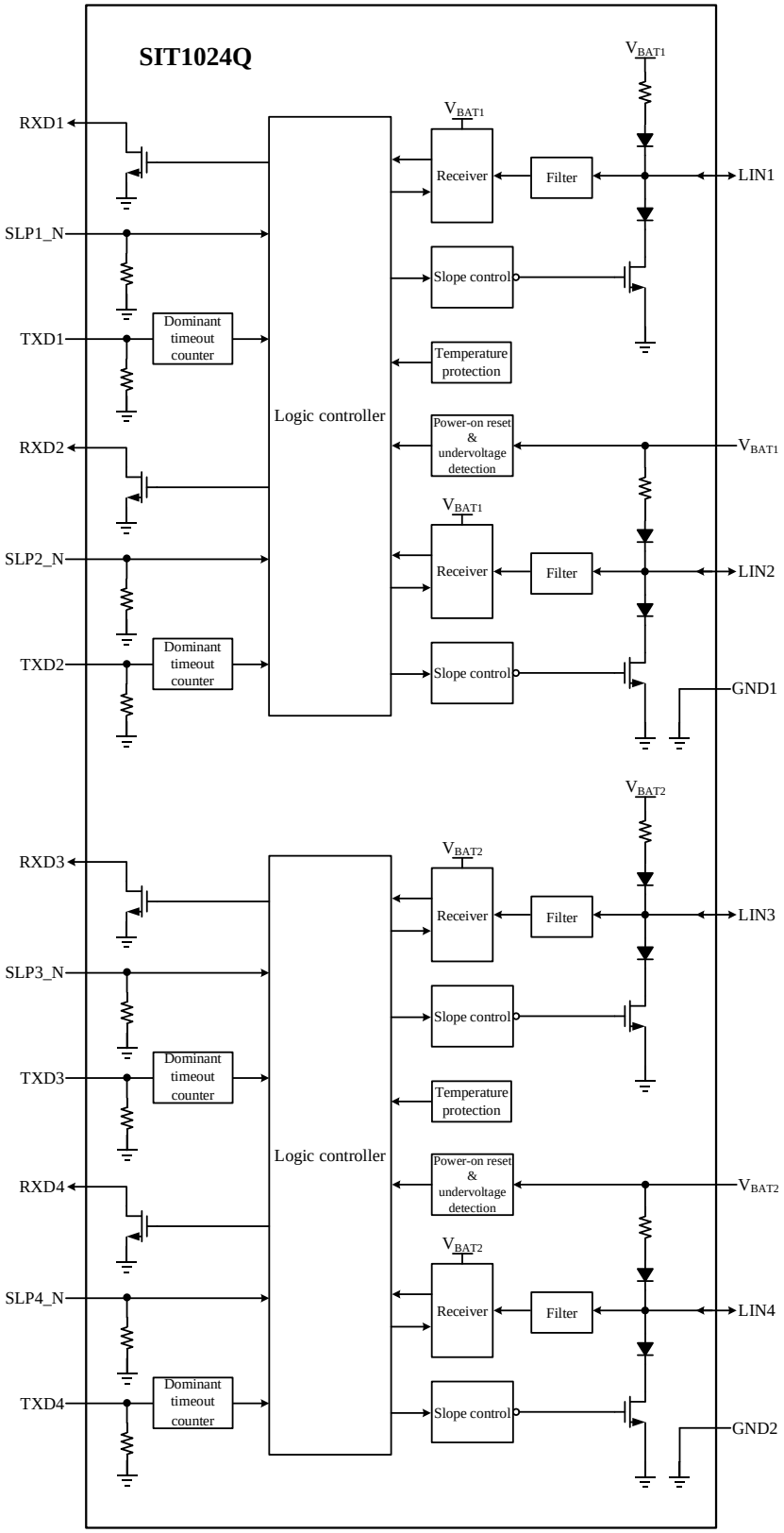


Fig 2 Block diagram of SIT1024Q

FEATURE DESCRIPTION

1 Overview

SIT1024Q is a four-channel interface chip used between LIN protocol controller and the physical bus. It can be used for in-vehicle and industrial control with a data rate up to 20kbps. As shown in Fig 2, SIT1024Q is divided into two independent control dual-channel LIN transceiver modules with LIN1/LIN2 and LIN3/LIN4, using VBAT1 and VBAT2 two power supply, respectively has independent logic control circuit, power-on detection circuit and over-temperature protection circuit. SIT1024Q receives the data stream from the protocol controller at the sending data input terminal (TXDx) and converts it into the bus signal with the best swing rate and waveform shaping. The input data on the LIN bus is received by the receiver of SIT1024Q, and converted into a low-voltage logic level signal through the RXDx port to output to the external microcontroller. This device is compliant with LIN 2.x, ISO 17987-4:2016 (12V) and SAE J2602 standards.

2 Operating modes

As shown in Fig 3, SIT1024Q supports four function modes for very-low-power operation (Sleep mode), standby operation (Standby mode), normal operation (Normal mode) and power-up (Power-on reset mode).The operating states in each mode are shown in table 2. SIT1024Q is a four-channel LIN transceiver. Except for the power-on reset mode, the working state of each channel can be controlled independently, that is, the LIN transceiver of the four channels can work in different modes respectively.

2.1 Sleep mode

In normal mode, when SLPx_N pin has a falling edge and SLPx_N remains low for longer than $t_{gotosleep}$, the LIN transceiver of the corresponding channel of SIT1024Q enters the sleep mode. SIT1024Q has very low static power consumption when all LIN transceivers of four channels enter sleep mode, but it can still remotely wake up the corresponding channel to enter standby mode through LINx pin, or directly switch to normal mode by pulling up SLPx_N pin.

In order to prevent the SIT1024Q from waking up due to unexpected wake up events caused by car transient or EMI, filters are designed at the inputs LINx pin and SLPx_N pin of the receiver. The necessary conditions for SIT1024Q to be woken up in sleep mode are as follows: the remote wake-up time through LINx pin must be longer than $t_{wake(dom)LIN}$ (dominant wake time of bus); The direct wake-up time through the SLPx_N pin must be longer than the $t_{gotonorm}$。

2.2 Standby mode

When SIT1024Qis in sleep mode, if a remote wake-up event is detected, the device will automatically enter standby mode immediately, and the low level on the RXDx pin will indicate that the wake-up process is used to send a wake up source flag to the MCU (LIN1~LIN4). The SIT1024Q has very low static power consumption when all four-channel LIN transceivers are in standby mode.

Setting pin SLPx_N high during standby mode may result in the following events:

(1) The LIN transceiver of the corresponding channel enters the normal mode if the high level on pin SLPx_N has been maintained for a certain time period $t_{gotonorm}$.

(2) An immediate reset of the wake-up request signal on pin RXDx.

2.3 Normal mode

Only in normal mode the SIT1024Q is able to transmit and receive data via the LIN bus and the communication of four-channel LIN transceiver operates independently. The receiver detects the data stream on the LIN bus and outputs it to the microcontroller via pin RXDx, and the high level of bus represents recessive and low level represents dominant. TXDx is the output of the driver, the data stream from protocol controller sent by TXDx to LINx pin output and waveform shaping to minimize electromagnetic radiation emission (EME). When SIT1024Q is used as slave node, LINx port is pulled to V_{BATx} via internal slave resistor. When SIT1024Q is used as the host node, the LINx port is pulled up to the V_{BATx} through an external resistor and a diode in series.

In sleep or standby mode, as long as the high level hold time on the SLPx_N pin is longer than the $t_{gotonorm}$, the LIN transceiver of the corresponding channel will enter the normal mode. If the low level hold time on the SLPx_N pin is longer than $t_{gotosleep}$, the LIN transceiver on the corresponding channel switches to sleep mode.

2.4 Power-on reset mode

If the voltage on V_{BAT} is less than the low-level reset threshold $V_{th(VBATL)L}$ when powering on, the SIT1024Q is in power-on reset mode and all input and output functions are disabled; when the voltage on V_{BATx} is longer than the high-level reset threshold $V_{th(VBATL)H}$, SIT1024Q enters sleep mode.

3 Remote wake up events

LINx pin remote wake-up: When the LINx pin is pulled down to a low level through a falling edge, a rising edge appears at the next moment, and the low-level holds time between the rising edge and the falling edge at the previous moment is longer than $t_{wake(dom)LIN}$, the process is regarded as effective remote wake-up (as shown in Fig 3). After the remote wake-up, the wake-up request event interrupts the microcontroller with the low level of the RXDx pin as the indicator signal.

4 Thermal shutdown

In normal mode, he over-temperature protection circuit will disable the output driver when the junction temperature of SIT1024Q exceeds the shutdown junction temperature $T_{j(sd)}$ (LIN1/LIN2 or LIN3/LIN4). When the junction temperature is lower than the hysteresis temperature, the driver is enabled again.

5 Dominant timeout function

If the TXDx pin is forced to be permanently low due to hardware and/or software application failures, the integrated TXDx dominant timeout timer circuit prevents the bus line from being driven to a permanently dominant state (blocking all network communications). The timer is triggered by the falling edge on the

TXDx pin. If the low level on the TXDx holds longer than the internal timer time ($t_{to(dom)TXD}$), the transmitter will be disabled and the drive bus will go into a recessive state. The timer is reset by the rising edge on the TXDx pin.

6 Fail-safe feature

- The interior of the TXDx pin is pulled down to the ground to prevent the undefined floating state of the TXDx pin.
- The interior of the SLPx_N pin is pulled down to the ground, and the corresponding LIN transceiver will enter the sleep mode when the SLPx_N pin is floating.
- The loss-of-ground condition has no effect on the bus port, and the bus port has no reverse current.
- The bus driver output stage current limiting to prevent the driver from burning down or functional effects when the bus short-circuits to theV_{BATx}.
- To avoid the effects caused by TXDx pins being forced to permanently low due to hardware and/or software application failures, after switching to normal mode, the LINx driver will be enabled only if a high TXDx level is detected.

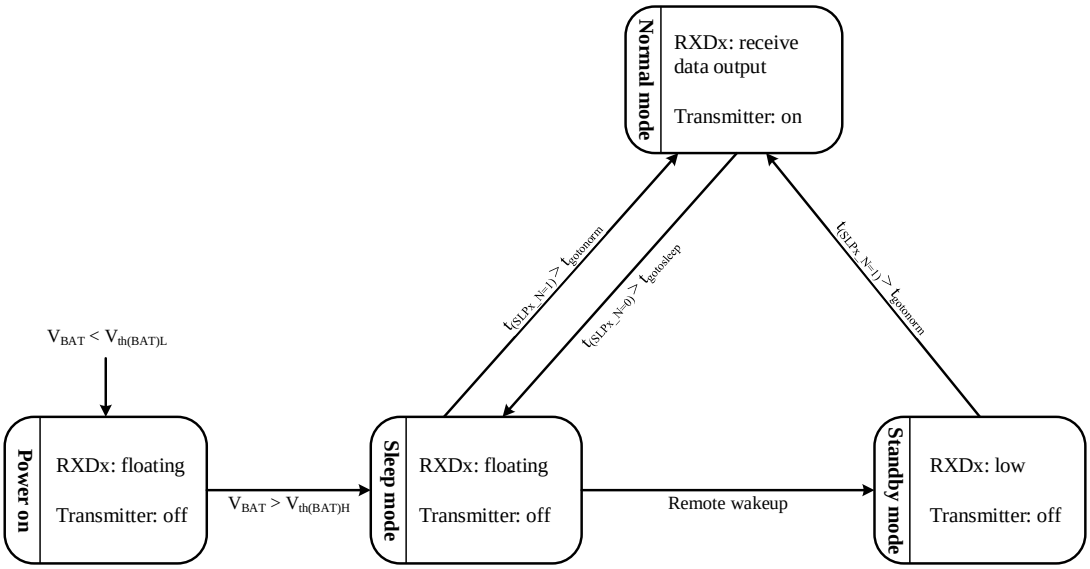


Fig 3 State diagram

Table 2 Working status of SIT1024Q in each mode

Mode	SLPx_N	RXDx	Transmitter x	Remarks
Sleep x	low	floating	off	No wake-up request detected
Standby x	low	low	off	Wake-up request detected
Normal x	high	Recessive: high Dominant: low	on	Enable bus signal shaping
Power-on	low	floating	off	Disable all input and output functions

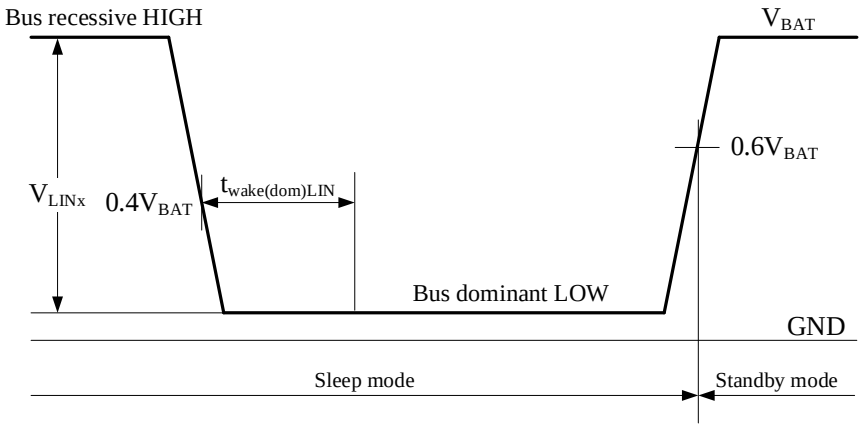


Fig 4 Remote wake-up behavior

STATIC CHARACTERISTICS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power consumption						
Supply voltage	V_{BAT}	V_{BAT1} and V_{BAT2}	5.5		27	V
battery supply current on V_{BAT1} or V_{BAT2} pins (V_{BAT1} or V_{BAT2} is denoted by V_{BAT}, the same below)	I_{BAT}	Sleep mode (dual channel); bus recessive (dual channel); V_{LINx}=V_{BAT}; V_{SLPx_N}=0V	-	5	20	μA
		Sleep mode (dual channel); bus dominant (dual channel); V_{LINx}=0V; V_{SLPx_N}=0V	-	800	2000	μA
		Standby mode (dual channel); bus recessive (dual channel); V_{LINx}=V_{BAT}; V_{SLPx_N}=0V	-	5	20	μA
		Standby mode (dual channel); bus dominant (dual channel); V_{BAT}=12V; V_{LINx}=0V; V_{SLPx_N}=0V	-	800	2000	μA
		Normal mode (dual channel); bus recessive (dual channel); V_{LINx}=V_{BAT}; V_{TXDx}=5V; V_{SLPx_N}=5V	-	240	800	μA
		Normal mode (dual channel) Bus dominant (dual channel); V_{BAT}=12V; V_{TXDx}=0V; V_{SLPx_N}=5V	-	3	8	mA
Power-on reset						
LOW-level V_{BAT} reset threshold voltage	$V_{th}(V_{BATL})L$		3.9	4.4	4.7	V
HIGH-level V_{BAT} reset threshold voltage	$V_{th}(V_{BATL})H$		4.2	4.7	5.1	V
V_{BAT} reset hysteresis voltage	$V_{hys}(V_{BATL})$		0.15	0.3	0.6	V
Pin TXDx						
HIGH-level input voltage	V_{IH}		2	-	7	V
LOW-level input voltage	V_{IL}		-0.3	-	+0.8	V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
hysteresis voltage	V_{hys}		50	200	400	mV
pull-down resistance on pin TXDx	$R_{PD(TXDx)}$	V_{TXDx}=5V	50	125	400	kΩ
LOW-level input current	I_{IL}	V_{TXDx}=0V	-5	-	5	μA
Pin SLPx_N						
HIGH-level input voltage	V_{IH}		2	-	7	V
LOW-level input voltage	V_{IL}		-0.3	-	0.8	V
hysteresis voltage	V_{hys}		50	200	400	mV
pull-down resistance on pin SLPx_N	$R_{PD(SLPx\_N)}$	V_{SLPx_N}=5V	100	250	650	kΩ
LOW-level input current	I_{IL}	V_{SLPx_N}=0V	-5	-	5	μA
Pin RXDx						
LOW-level output current	I_{OL}	Normal mode; V_{RXDx}=0.4V; V_{LINx}=0V	1.5	-	-	mA
HIGH-level leakage current	I_{LH}	Normal mode; V_{RXDx}=5V; V_{LINx}=V_{BAT}	-5	-	5	μA
Pin LINx						
current limitation for driver dominant state	I_{BUS_LIM}	V_{TXDx}=0V; V_{LINx}=V_{BAT}=18V	40	-	100	mA
receiver recessive input leakage current	$I_{BUS\_PAS\_rec}$	V_{TXDx}=5V; V_{LINx}=27V; V_{BAT}=5.5V	-	-	10	μA
receiver dominant input leakage current	$I_{BUS\_PAS\_dom}$	Normal mode; V_{TXDx}=5V; V_{LINx}=0V; V_{BAT}=12V	-600	-	-	μA
loss-of-ground bus current	$I_{L(log)}$	V_{BAT}=27V; V_{LINx}=0V	-1000	-	10	μA
loss-of-battery bus current	$I_{L(lob)}$	V_{BAT}=0V; V_{LINx}=27V	-	-	10	μA
Receiver dominant threshold voltage	$V_{th(dom)RX}$		-	-	0.4V_{BAT}	V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Receiver recessive threshold voltage	$V_{th(rec)RX}$		$0.6V_{BAT}$	-	-	V
Receiver center voltage	$V_{th(RX)cntr}$	$V_{th(RX)\ cntr}$= ($V_{th(rec)RX}$+ $V_{th(dom)RX}$)/2	$0.475V_{BAT}$	$0.5V_{BAT}$	$0.525V_{BAT}$	V
Receiver hysteresis threshold voltage	$V_{th(hys)RX}$	$V_{th(hys)RX}$= $V_{th(rec)RX}$-$V_{th(dom)RX}$	-	-	$0.175V_{BAT}$	V
Slave resistance	R_{slave}	connected between pins LIN and V_{BAT}; V_{LINx}=0V; V_{BAT}=12V; V_{TXDx}=V_{SLPx_N}=5V	20	30	60	kΩ
capacitance on pin LIN	C_{LIN} [1]		-	-	30	pF
Dominant output voltage	$V_{o(dom)}$	Normal mode; V_{TXDx}=0V; V_{BAT}=7V	-	-	1.4	V
Dominant output voltage	$V_{o(dom)}$	Normal mode; V_{TXDx}=0V; V_{BAT}=18V	-	-	2.0	V
Thermal shutdown						
shutdown junction temperature	$T_{j(sd)}$ [1]		150	-	200	°C

(Unless specified otherwise; 5.5V≤V_{BAT}≤27V, -40°C≤T_j≤150°C; typical in V_{BAT}=12V, T_{amb}=25°C).

[1] Not tested in production; guaranteed by design.

SWITCH CHARACTERISTICS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Duty cycles						
Duty cycle 1	δ1 [1][2]	$V_{th(rec)(max)}$=0.744×V_{BAT}; $V_{th(dom)(max)}$=0.581×V_{BAT}; t_{bit}=50μs; V_{BAT}=7V~18V Fig 5	0.396	-	-	
		$V_{th(rec)(max)}$=0.76×V_{BAT}; $V_{th(dom)(max)}$=0.593×V_{BAT}; t_{bit}=50μs; V_{BAT}=5.5V~7V Fig 5	0.396	-	-	
Duty cycle 2	δ2 [2][3]	$V_{th(rec)(min)}$=0.422×V_{BAT}; $V_{th(dom)(min)}$=0.284×V_{BAT}; t_{bit}=50μs; V_{BAT}=7.6V~18V Fig 5	-	-	0.581	
		$V_{th(rec)(min)}$=0.41×V_{BAT}; $V_{th(dom)(min)}$=0.275×V_{BAT}; t_{bit}=50μs; V_{BAT}=6.1V~7.6V Fig 5	-	-	0.581	
Duty cycle 3	δ3 [1][2]	$V_{th(rec)(max)}$=0.778×V_{BAT}; $V_{th(dom)(max)}$=0.616×V_{BAT}; t_{bit}=96μs; V_{BAT}=7V~18V Fig 5	0.417	-	-	
		$V_{th(rec)(max)}$=0.797×V_{BAT}; $V_{th(dom)(max)}$=0.630×V_{BAT}; t_{bit}=96μs; V_{BAT}=5.5V~7V Fig 5	0.417	-	-	
Duty cycle 4	δ4 [2][3]	$V_{th(rec)(min)}$=0.389×V_{BAT}; $V_{th(dom)(min)}$=0.251×V_{BAT}; t_{bit}=96μs; V_{BAT}=7.6V~18V Fig 5	-	-	0.590	
		$V_{th(rec)(min)}$=0.378×V_{BAT}; $V_{th(dom)(min)}$=0.242×V_{BAT}; t_{bit}=96μs; V_{BAT}=6.1V~7.6V Fig 5	-	-	0.590	
Timing characteristics						
Receiver propagation delay	$t_{PD(RX)}$ [4]		-	-	6	μs
Receiver propagation delay	$t_{PD(RX)sym}$ [4]		-2	-	2	μs

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
LIN dominant wake-up time	$t_{wake(dom)LIN}$	Sleep mode	30	68	150	μs
Go to normal time	$t_{gotonorm}$		2	6	10	μs
Go to sleep time	$t_{gotosleep}$		2	6	10	μs
Dominant time-out time	$t_{to(dom)TXD}$	start with the falling edge on TXDx	6	12	50	ms

(Unless specified otherwise; 5.5V≤V_{BAT}≤18V, -40℃≤T_j≤150℃; typical in V_{BAT}=12V, T_{amb}=25℃).

[1] $\delta 1, \delta 3 = \frac{t_{bus(rec)(\min)}}{2 \times t_{bit}}$;

[2] Bus load conditions: (1) C_{Lx}=1nF, R_{Lx}=1kΩ; (2) C_{Lx}=6.8nF, R_{Lx}=660Ω; (3) C_{Lx}=10nF, R_{Lx}=500Ω;

[3] $\delta 2, \delta 4 = \frac{t_{bus(rec)(\max)}}{2 \times t_{bit}}$;

[4] Load condition pin RXDx: C_{TXDx}=20pF, R_{RXDx}=2.4kΩ.

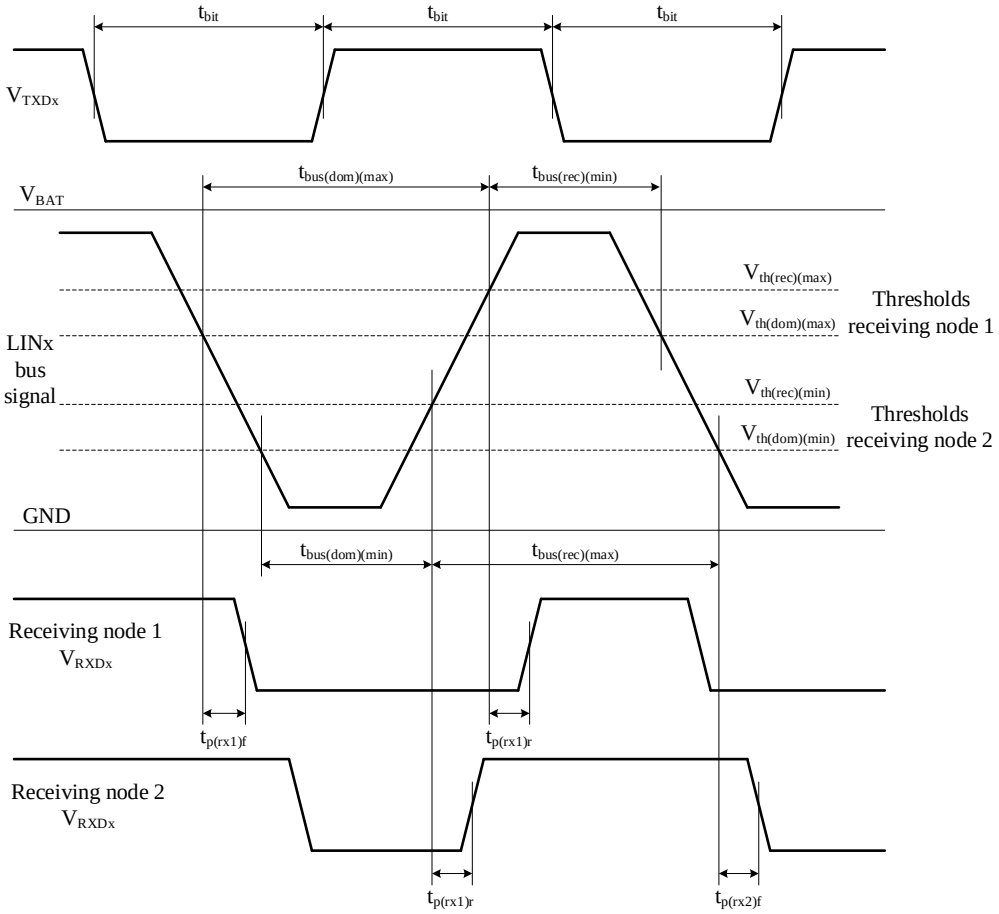


Fig 5 Bus signal transmission timing diagram

TYPICAL APPLICATION

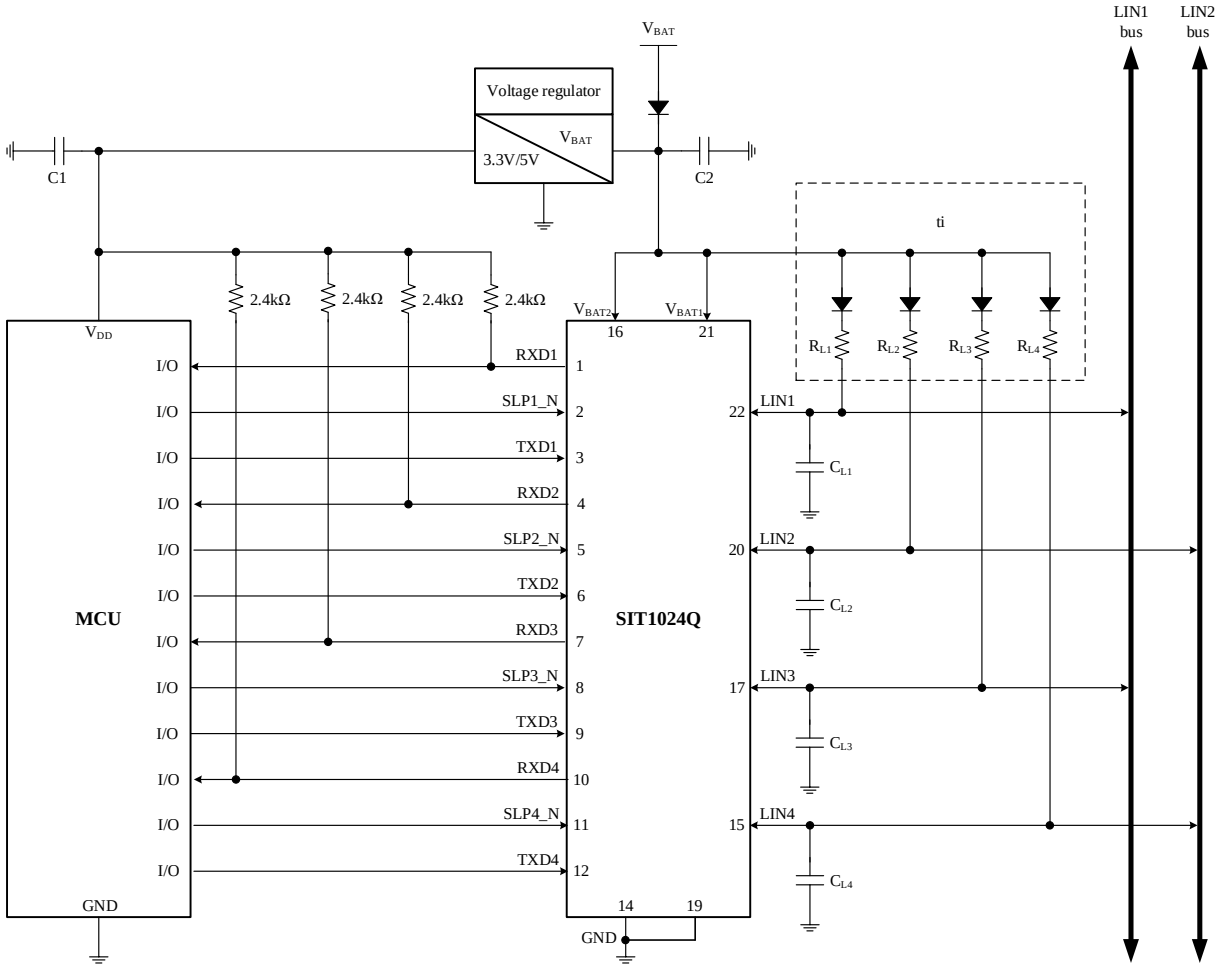


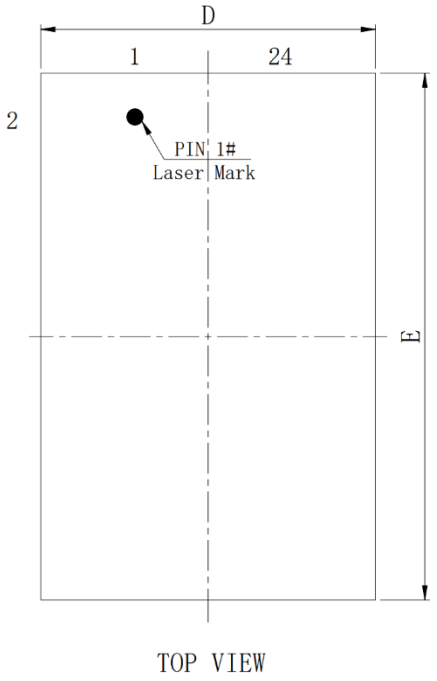
Fig 6 Typical application of the SIT1024Q

Note: C_{Lx}=220pF when used as a slave node; RLx/CLx combination of 660Ω/6.8nF is recommended when the master node is used to obtain a slower bus waveform slope.

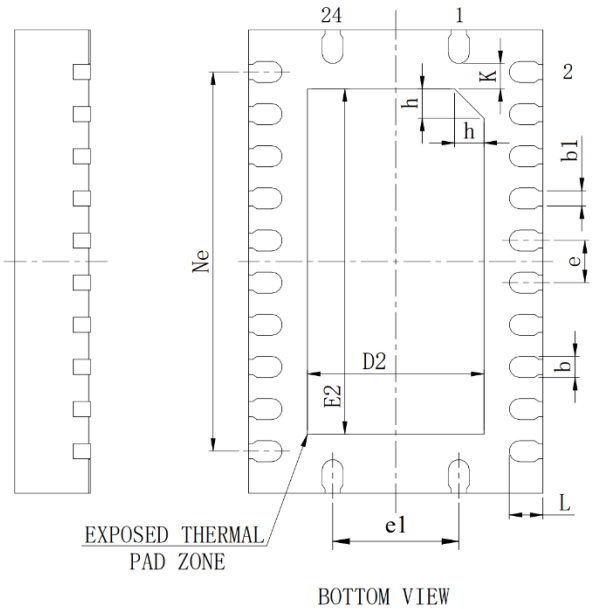
QFN24L/DHVQFN24 DIMENSIONS

PACKAGE SIZE

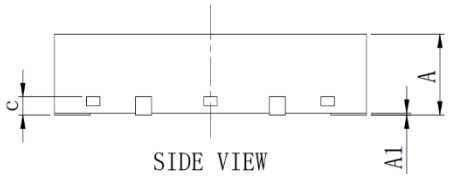
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.85	0.90	0.95
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.18REF	
c		0.203REF	
D	3.40	3.50	3.60
D2	2.00	2.10	2.20
e		0.50BSC	
e1		1.50BSC	
Ne		4.50BSC	
E	5.40	5.50	5.60
E2	4.00	4.10	4.20
L	0.35	0.40	0.45
h	0.30	0.35	0.40
K		0.30REF	



TOP VIEW

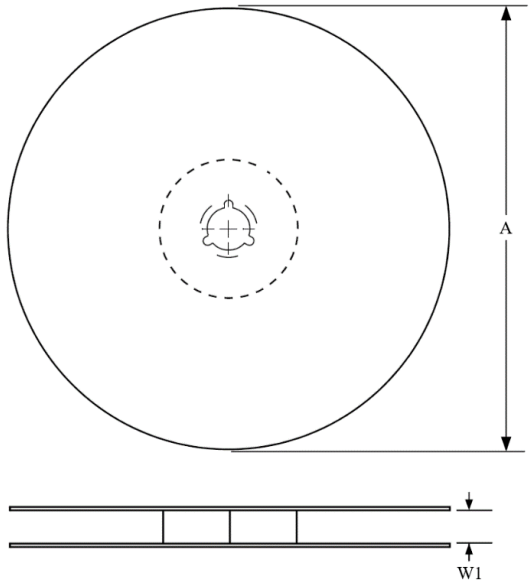


BOTTOM VIEW

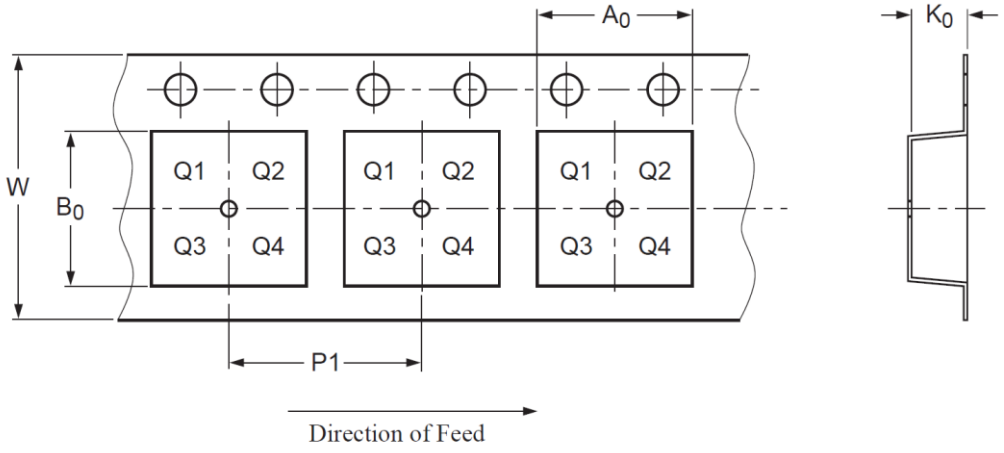


SIDE VIEW

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



PIN1 is in quadrant 1

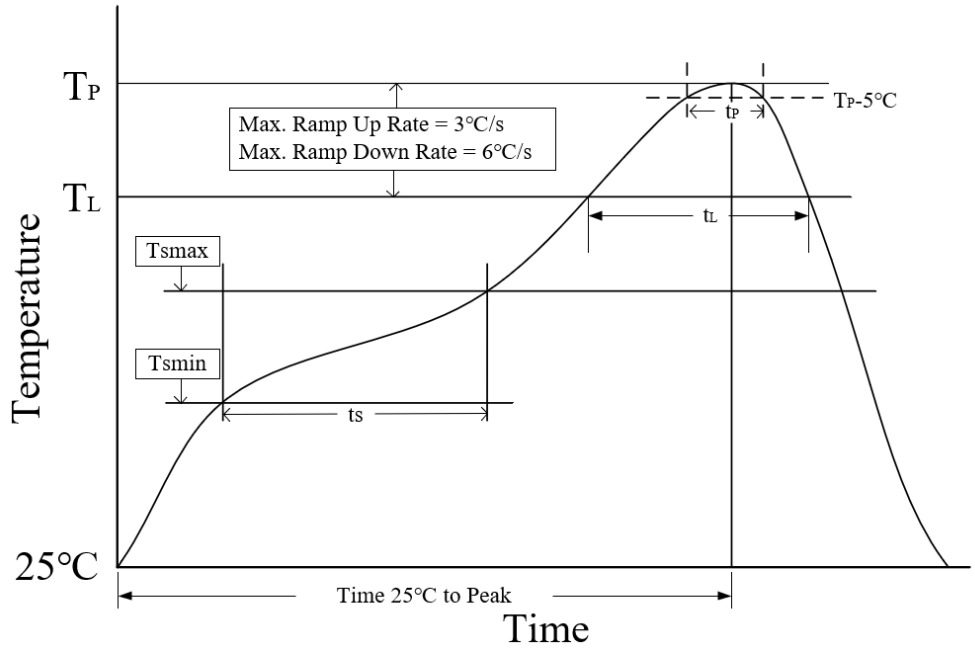
Package type	Reel diameter A (mm)	Tape width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
QFN24L	330±1	12.4	3.80±0.10	5.80±0.10	1.05±0.10	8.00±0.10	12.00±0.30

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	PACKING
SIT1024QHG	QFN24L/DHVQFN24, Small outline package (3.5mm*5.5mm), no leads	Tape and reel

Leadless QFN24L/DHVQFN24 is packed with 5000 pieces/disc in braided packaging.

REFLOW SOLDERING



parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	3 °C/second max
Preheat time t_s (T_{smin}=150 °C to T_{smax}=200 °C)	60-120 seconds
Melting time t_L (T_L=217 °C)	60-150 seconds
Peak temp T_P	260-265 °C
5°C below peak temperature t_P	30 seconds
Ave cooling rate (T_P to T_L)	6 °C/second max
Normal temperature 25°C to peak temperature T_P time	8 minutes max

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Data sheet status	Revision date
V1.0	Initial version.	March 2023
V1.1	Added “AEC-Q100 qualified”; Adjusted format.	September 2023
V1.2	Updated VBAT supply voltage range; Updated battery supply current in Sleep and Standby mode.	January 2024