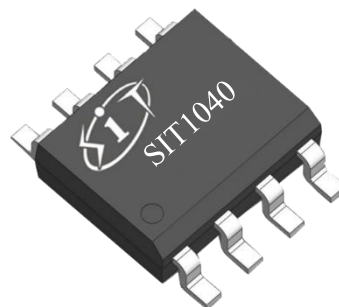


## FEATURES

- Fully compatible with the ISO 11898 standard
- Thermally protected
- Input levels compatible with 3.3 V and 5 V devices
- Transmit Data (TXD) dominant time-out function
- Very low-current standby mode with remote wake-up Capability via the bus: 5μA Typical
- Transceiver in unpowered state disengages from the bus (zero load)
- At least 110 nodes can be connected
- High speed (up to 1 Mbaud)
- Very low Electro Magnetic Emission (EME)
- Provide DFN3\*3-8, Small Outline, Leadless Package

## PRODUCT APPEARANCE



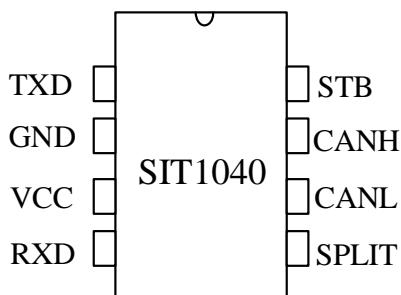
Provide Green and Environmentally  
Friendly Lead-free package

## DESCRIPTION

The SIT1040 is the interface between the Controller Area Network (CAN) protocol controller and the physical bus. It is primarily intended for high-speed applications, up to 1 Mbaud, in in-vehicle, industry control and other fields. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller.

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
Supply voltage	$V_{cc}$		4.5	5.5	V
Maximum transmission rate	$1/t_{bit}$	Non-return to zero code	1		Mbaud
CANH/CANL input or output voltage	$V_{can}$		-40	+40	V
Bus differential voltage	$V_{diff}$		1.5	3.0	V
Ambient temperature	$T_{amb}$		-40	125	°C
ESD	$V_{esd}$	HBM	±8		kV

## PIN CONFIGURATION



**PIN DESCRIPTION**

PIN	SYMBOL	DESCRIPTION
1	TXD	transmit data input
2	GND	ground supply
3	VCC	supply voltage
4	RXD	receive data output; reads out data from the bus lines
5	SPLIT	common-mode stabilization output
6	CANL	LOW-level CAN bus line
7	CANH	HIGH-level CAN bus line
8	STB	standby mode control input

**LIMITING VALUES**

PARAMETER	SYMBOL	VALUE	UNIT
Supply voltage	$V_{CC}$	-0.3~+6	V
DC voltage on TXD/RXD/STB pins	TXD, RXD, STB	-0.3~ $V_{CC}+0.3$	V
Voltage range at any bus terminal (CANH, CANL, SPLIT)	CANL, CANH, SPLIT	-40~40	V
Transient voltage on pins CANH, CANL and SPLIT see <a href="#">Fig.7</a>	$V_{tr}$	-200~+200	V
Storage temperature	$T_{stg}$	-55~150	°C
Ambient temperature	$T_{amb}$	-40~125	°C
Virtual junction temperature	$T_j$	-40~150	°C
Welding temperature range		300	°C

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

**DRIVER ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
CANH dominant output voltage	$V_{OH(D)}$	VI=0V, STB=0V, RL=60Ω, <a href="#">Fig.1</a> , <a href="#">Fig.2</a>	2.75	3.5	4.5	V
CANL dominant output voltage	$V_{OL(D)}$		0.5	1.5	2.25	V
Bus recessive output voltage	$V_{O(R)}$	VI=3V, STB=0V, RL=60Ω, <a href="#">Fig.1</a> , <a href="#">Fig.2</a>	2	2.5	3	V
Bus dominant differential output voltage	$V_{OD(D)}$	VI=0V, STB=0V, RL=60Ω, <a href="#">Fig.1</a> , <a href="#">Fig.2</a>	1.5		3	V
Bus recessive differential output voltage	$V_{OD(R)}$	VI=3V, S=0V, <a href="#">Fig.1</a> , <a href="#">Fig.2</a>	-0.012		0.012	V
		VI=3V, STB=0V, NO LOAD	-0.5		0.05	V
Transmitter dominant voltage symmetry	$V_{dom(TX)sym}$	$V_{dom(TX)sym} = V_{CC} - V_{CANH} - V_{CANL}$	-400		400	mV
Transmitter voltage symmetry	$V_{TXsym}$	$V_{TXsym} = V_{CANH} + V_{CANL}$	0.9V <sub>CC</sub>		1.1V <sub>CC</sub>	V
Common-mode output voltage	$V_{OC}$	STB=0V, <a href="#">Fig.8</a>	2	2.5	3	V
Peak-to-peak Common-mode output voltage	$\Delta V_{OC}$			30		mV
Short-circuit output current	$I_{OS}$	CANH=-12V, CANL=open, <a href="#">Fig.11</a>	-105	-72		mA
		CANH=12V, CANL=open, <a href="#">Fig.11</a>		0.36	1	mA
		CANL=-12V, CANH=open, <a href="#">Fig.11</a>	-1	0.5		mA
		CANL=12V, CANH=open, <a href="#">Fig.11</a>		71	105	mA
Recessive output current	$I_{O(R)}$	-27V<CANH<32V 0<VCC<5.25V	-2.0		2.5	mA

(V<sub>CC</sub>=5V±10% and -40°C ≤ T<sub>j</sub> ≤ 150°C unless specified otherwise; typical in V<sub>CC</sub>=+5V and T<sub>amb</sub>=25°C)

**DRIVER SWITCHING CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation delay time, low-to-high-level output	$t_{PLH}$	STB=0V, <a href="#">Fig.4</a>	25	65	120	ns
Propagation delay time, low-to-high-level output	$t_{PHL}$		25	45	90	ns
Differential output signal rise time	$t_r$			25		ns
Differential output signal fall time	$t_f$			50		ns
Enable time from standby mode to dominant	$t_{EN}$	<a href="#">Fig.7</a>			10	$\mu$ s
Bus dominant time-out time	$t_{dom}$	<a href="#">Fig.10</a>	300	450	700	$\mu$ s
Bus wake-up filter time	$t_{BUS}$		0.7		5	$\mu$ s

( $V_{CC}=5V\pm 10\%$  and  $-40^\circ C \leq T_j \leq 150^\circ C$  unless specified otherwise; typical in  $V_{CC}=+5V$  and  $T_{amb}=25^\circ C$ )

**RECEIVER ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Positive-going input threshold voltage	$V_{IT+}$	STB=0V, <a href="#">Fig.5</a>		800	900	mV
Negative-going input threshold voltage	$V_{IT-}$		500	650		mV
Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )	$V_{HYS}$		100	125		mV
High-level output voltage	$V_{OH}$	$I_O=-2mA$ , <a href="#">Fig.6</a>	4	4.6		V
Low-level output voltage	$V_{OL}$	$I_O=2mA$ , <a href="#">Fig.6</a>		0.2	0.4	V
Power-off bus input current	$I_{(OFF)}$	CANH or CANL=5V, Other pin=0V			5	$\mu$ A
Input capacitance to ground, (CANH or CANL)	$C_I$			13		pF
Differential input capacitance	$C_{ID}$			5		pF

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input resistance, (CANH or CANL)	$R_{IN}$	TXD=3V, STB=0V	15	30	40	k $\Omega$
Differential input resistance	$R_{ID}$		30		80	k $\Omega$
Input resistance matching	$R_{I_{match}}$	CANH=CANL	-3%		3%	
The range of common-mode voltage	$V_{COM}$		-12		12	V

( $V_{CC}=5V\pm 10\%$  and  $-40^{\circ}C \leq T_j \leq 150^{\circ}C$  unless specified otherwise; typical in  $V_{CC}=+5V$  and  $T_{amb}=25^{\circ}C$ )

## RECEIVER SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation delay time, high-to-low-level output	$t_{PLH}$	STB=0V or VCC, <a href="#">Fig.6</a>	60	100	130	ns
Propagation delay time, high-to-low-level output	$t_{PHL}$		45	70	90	ns
RXD signal rise time	$t_r$			8		ns
RXD signal fall time	$t_f$			8		ns

( $V_{CC}=5V\pm 10\%$  and  $-40^{\circ}C \leq T_j \leq 150^{\circ}C$  unless specified otherwise; typical in  $V_{CC}=+5V$  and  $T_{amb}=25^{\circ}C$ )

## DEVICE SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Loop delay 1, driver input to receiver output, Recessive to Dominant	$t_{d(LOOP1)}$	STB=0V, <a href="#">Fig.9</a>	90		190	ns
Loop delay 2, driver input to receiver output, Dominant to Recessive	$t_{d(LOOP2)}$		90		190	ns

( $V_{CC}=5V\pm 10\%$  and  $-40^{\circ}C \leq T_j \leq 150^{\circ}C$  unless specified otherwise; typical in  $V_{CC}=+5V$  and  $T_{amb}=25^{\circ}C$ )

## OVER TEMPERATURE PROTECTION

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Shutdown junction temperature	$T_{j(sd)}$			160		$^{\circ}C$

**TXD-PIN CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
HIGH-level input current	$I_{IH}(TXD)$	$V_I=V_{CC}$	-2		2	$\mu A$
LOW-level input current	$I_{IL}(TXD)$	$V_I=0$	-50		-10	$\mu A$
When $V_{CC}=0V$ , current on TXD pin	$I_{O(off)}$	$V_{CC}=0V$ , $TXD=5V$			1	$\mu A$
HIGH-level input voltage	$V_{IH}$		2		$V_{CC}+0.3$	V
LOW-level input voltage	$V_{IL}$		-0.3		0.8	V
Open voltage on TXD pin	$TXD_O$		H			logic

( $V_{CC}=5V\pm 10\%$  and  $-40^\circ C \leq T_j \leq 150^\circ C$  unless specified otherwise; typical in  $V_{CC}=+5V$  and  $T_{amb}=25^\circ C$ )

**STB PIN CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
HIGH-level input voltage	$V_{IH}$	S	2.0		$V_{CC}+0.3$	V
LOW-level input voltage	$V_{IL}$	S	-0.3		0.8	V
HIGH-level input current	$I_{IH}$	$V_S=V_{CC}$		0		$\mu A$
LOW-level input current	$I_{IL}$	$V_S=0V$	-1	-3	-10	$\mu A$

**COMMON-MODE STABILIZATION OUTPUT**

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Common-mode stabilization output voltage	$V_O$	$-500\mu A < I_o < 500\mu A$	$0.3V_{CC}$		$0.7V_{CC}$	V
Leakage current	$I_{O(stb)}$	STB=2, $-12V < V_O < 12V$	-5		5	$\mu A$

( $V_{CC}=5V\pm 10\%$  and  $-40^\circ C \leq T_j \leq 150^\circ C$  unless specified otherwise; typical in  $V_{CC}=+5V$  and  $T_{amb}=25^\circ C$ )

**SUPPLY CURRENT**

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Standby	$I_{CC}$	STB=VCC, $V_I=V_{CC}$		5	12	$\mu A$
Dominant		$V_I=0V$ , STB=0V, LOAD=60 $\Omega$		50	70	mA
Recessive		$V_I=V_{CC}$ , STB=0V, NO LOAD		6	10	mA

( $V_{CC}=5V\pm 10\%$  and  $-40^\circ C \leq T_j \leq 150^\circ C$  unless specified otherwise; typical in  $V_{CC}=+5V$  and  $T_{amb}=25^\circ C$ )

**FUNCTION TABLE**
**Table1.CAN TRANSCEIVER TRUTH TABLE**

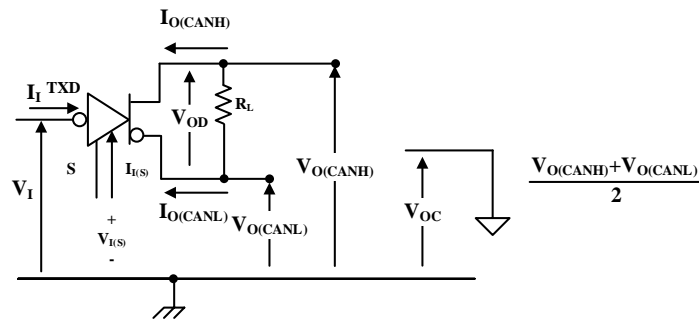
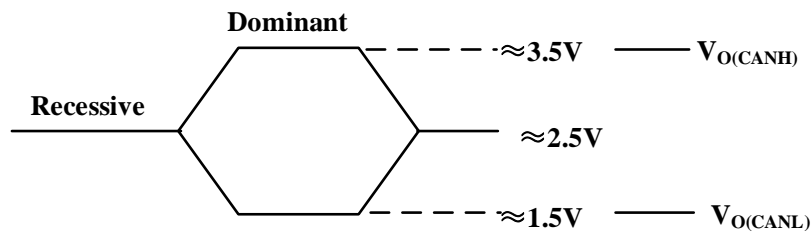
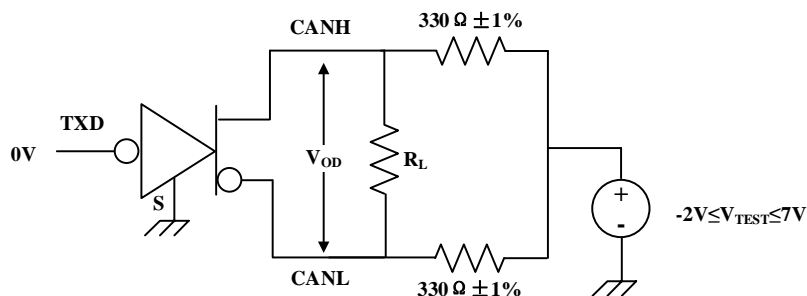
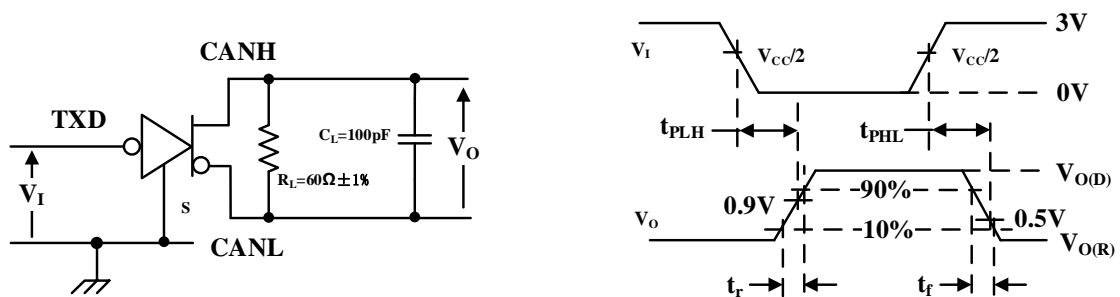
$V_{CC}$	TXD <sup>(1)</sup>	STB <sup>(1)</sup>	CANH <sup>(1)</sup>	CANL <sup>(1)</sup>	BUS STATE	RXD <sup>(1)</sup>
4.5V~5.5V	L	L	H	L	Dominate	L
4.5V~5.5V	H or Open	X	0.5 $V_{CC}$	0.5 $V_{CC}$	Recessive	H
4.5V~5.5V	X	H or Open	GND	GND	Recessive	H
0< $V_{CC}$ <4.5V	X	X	0V< $V_{CANH}$ < $V_{CC}$	0V< $V_{CANL}$ < $V_{CC}$	Recessive	X

(1) H=high level; L=low level; X=irrelevant

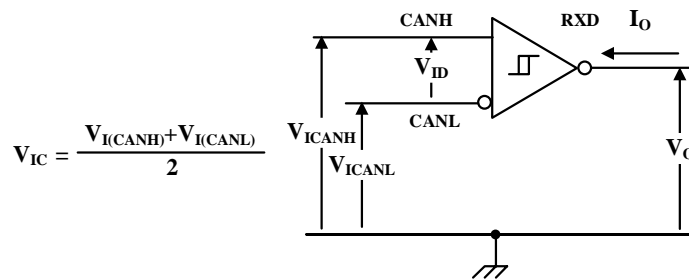
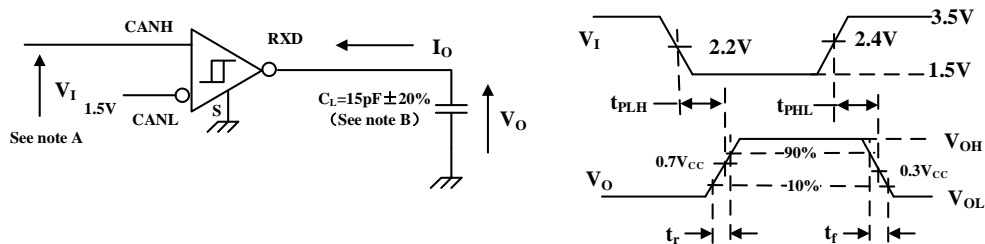
**Table 2. RECEIVER FUNCTION TABLE**

$V_{ID}=CANH-CANL$	RXD <sup>(1)</sup>	Bus State <sup>(1)</sup>
$V_{ID} \geq 0.9V$	L	Dominate
$0.5 < V_{ID} < 0.9V$	?	?
$V_{ID} \leq 0.5V$	H	Recessive
Open	H	Recessive

(1) H=high-level; L=low-level; ?=uncertain

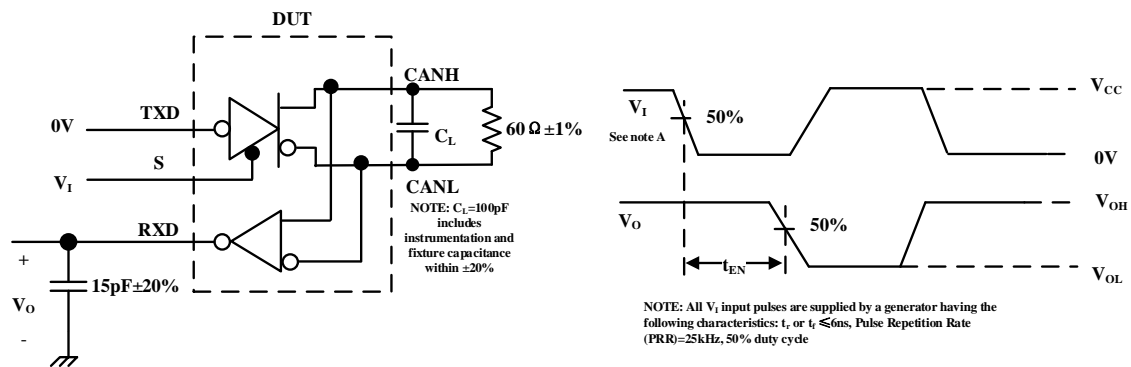
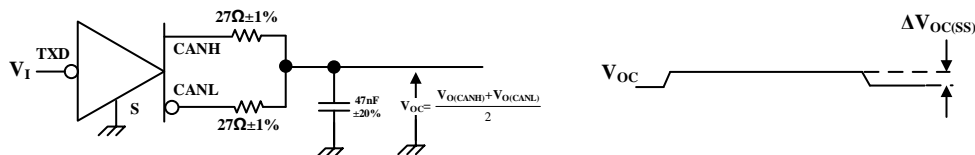
**TEST CIRCUIT**

**Fig.1 Driver Voltage, Current, and Test Definition**

**Fig.2 Bus Logic State Voltage Definition**

**Fig.3 Driver V<sub>OD</sub> Test Circuit**

**Fig.4 Driver Test Circuit and Waveform**




**Fig.5 Receiver Voltage and Current Definition**


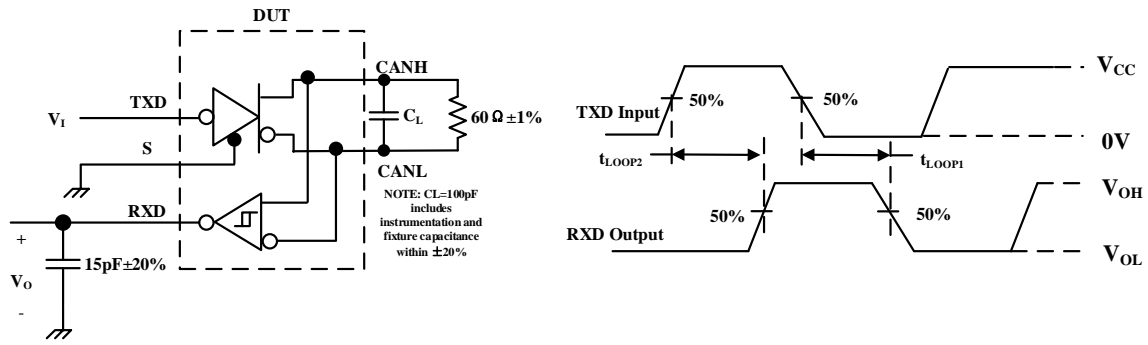
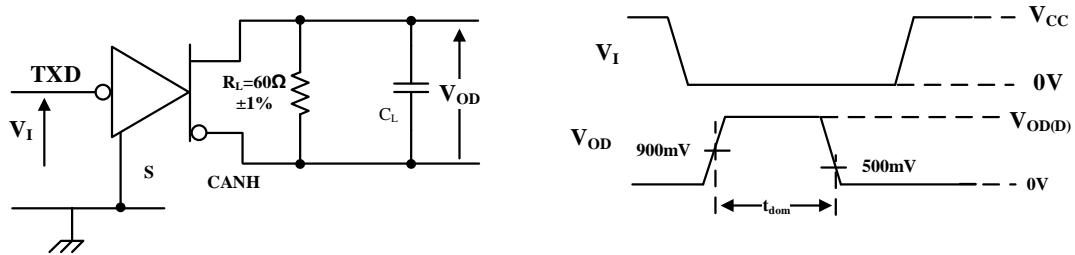
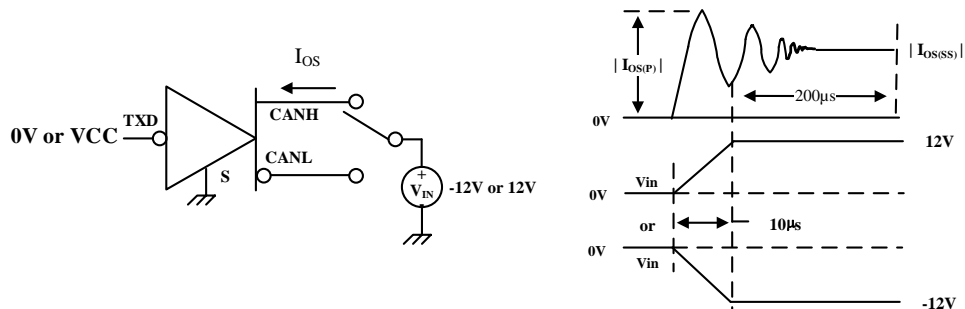
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125kHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_0 = 50\Omega$ .

B.  $C_L$  includes instrumentation and fixture capacitance within ±20%.

**Fig.6 Receiver Test Circuit and Waveform**

**Fig.7  $t_{EN}$  Test Circuit and Waveform**


A. All  $V_I$  input pulses are from 0 V to  $V_{CC}$  and supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 6$  ns, Pulse Repetition Rate (PRR) = 125kHz, 50% duty cycle.

**Fig.8 Peak-to-Peak Common Mode Output Voltage Test and Waveform**


**Fig.9  $t_{(\text{LOOP})}$  Test Circuit and Waveform**

**Fig.10 Dominant Time-Out Test Circuit and Waveform**

**Fig.11 Driver Short-Circuit Current Test Circuit and Waveform**

## ADDITIONAL DESCRIPTION

### 1 Sketch

The SIT1040 is the interface between the Controller Area Network (CAN) protocol controller and the physical bus, and can be applied to the fields of in-vehicle and industrial control etc. It is primarily intended for high-speed applications, up to 1 MBaud, in passenger cars. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller, and fully compatible with the ISO 11898 standard.

### 2 Current protection

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

### 3 Fail-safe features

Pin TXD provides a pull-up towards VCC in order to force a recessive level in case pin TXD is unpowered. Pin STB provides a pull-up towards VCC in order to force the transceiver into standby mode in case pin STB is unpowered.

In the case that the VCC is lost, pins TXD, STB and RXD will become floating to prevent reverse supplying conditions via these pins.

### 4 Over temperature protection

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature  $T_{j(sd)}$ , the output drivers will be disabled until the virtual junction temperature becomes lower than  $T_{j(sd)}$  and TXD becomes recessive again.

By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

### 5 TXD dominant time-out function

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value ( $t_{dom}$ ), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.

### 6 Operating modes

The SIT1040 provides two modes of operation which are selectable via pin STB:

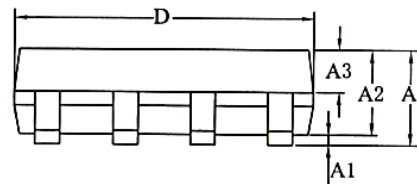
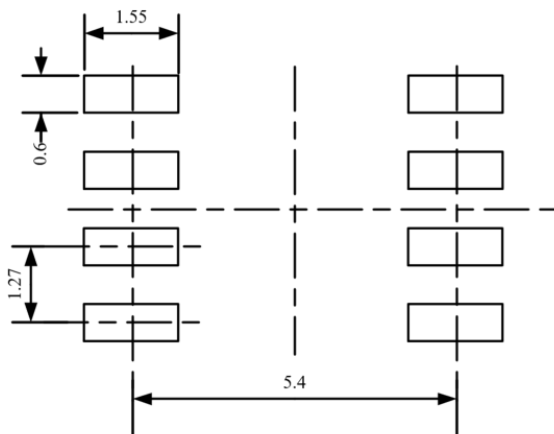
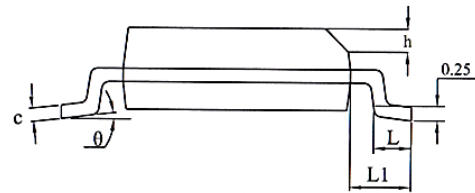
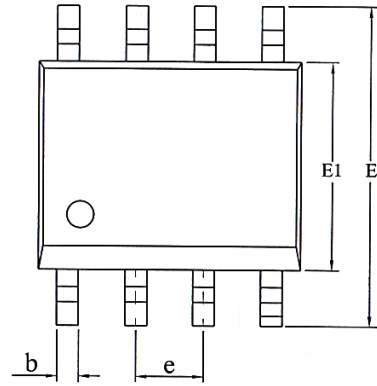
High-speed mode and standby mode.

High-speed mode is normal working mode, by connecting STB to ground to set the SIT1040 to high-speed mode. In this mode the transceiver is able to transmit and receive data via the bus lines CANH and CANL. The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD via the multiplexer (MUX).

If a logic-high or open is applied to STB, the SIT1040 enters a low-current standby mode. In this mode the transmitter and receiver are switched off, and the low-power differential receiver will monitor the bus lines. A HIGH level on pin STB activates this low-power receiver and the wake-up filter, and after  $t_{BUS}$  the state of the CAN bus is reflected on pin RXD.

**SOP8 DIMENSIONS**
**PACKAGE SIZE**

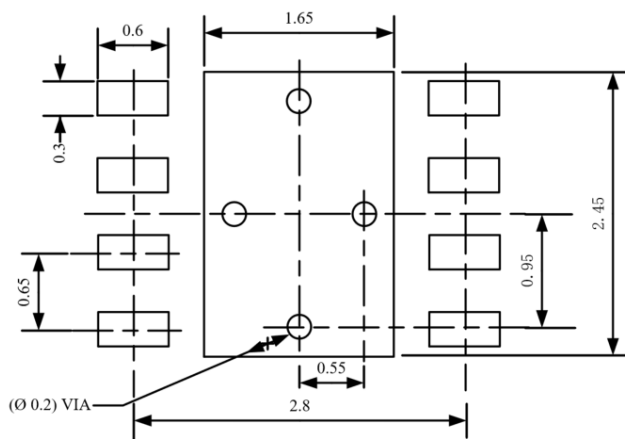
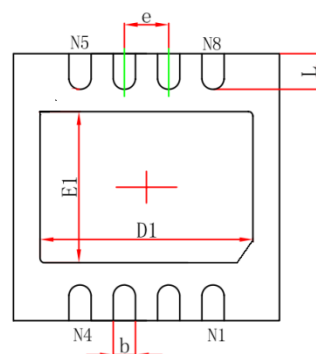
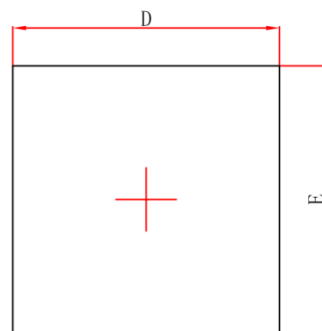
SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	1.40	-	1.80
A1	0.10	-	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.38	-	0.51
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.40	0.60	0.80
L1	1.05REF		
c	0.20	-	0.25
$\theta$	0°	-	8°



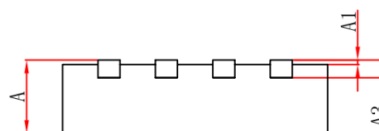
LAND PATTERN EXAMPLE (Unit: mm)

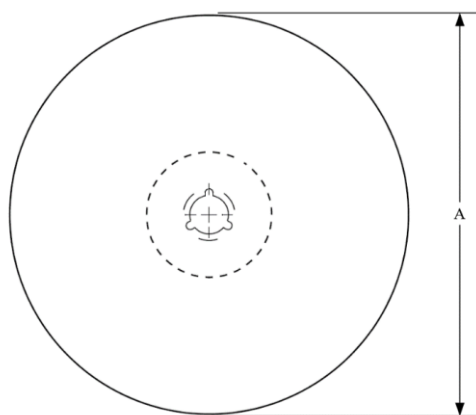
**DFN3\*3-8 DIMENSIONS**
**PACKAGE SIZE**

SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	0.70		0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	2.35	2.3	2.55
E1	1.55	1.65	1.75
b	0.2	0.25	0.33
e	0.65 TYP		
L	0.35		0.45

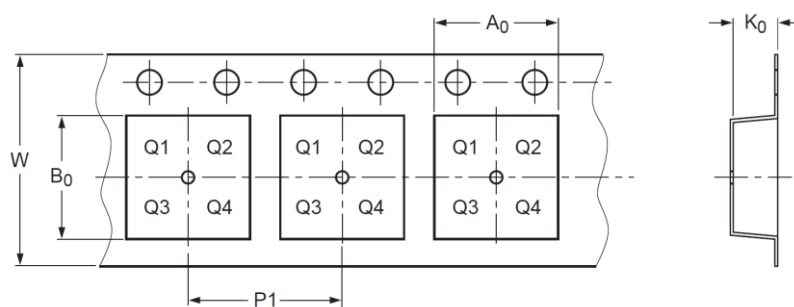


LAND PATTERN EXAMPLE (Unit: mm)



**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Direction of Feed

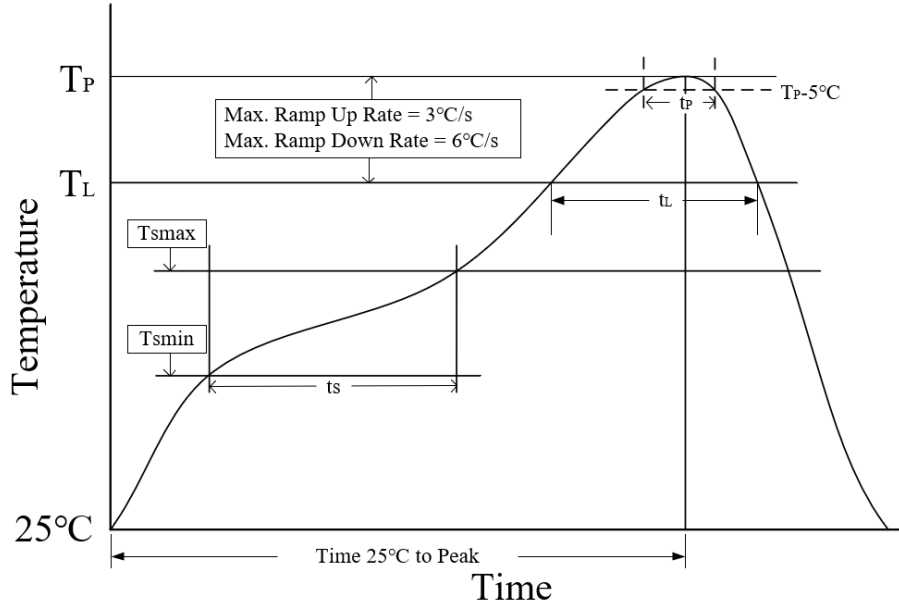
PIN1 is in quadrant 1

Package Type	Reel Diameter A (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
SOP8	330±1	12.4	6.60±0.1	5.30±0.10	1.90±0.1	8.00±0.1	12.00±0.1
DFN3*3-8	329±1	12.4	3.30±0.1	3.30±0.1	1.10±0.1	8.00±0.1	12.00±0.3

**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE	PACKING
SIT1040T	SOP8	Tape and reel
SIT1040TK	DFN3*3-8, Small shape, no leads, 8 terminals	Tape and reel

SOP8 package is 2500 pieces/disc. DFN3\*3-8 package is 5000 pieces/disc.

**REFLOW SOLDERING**


Parameter	Lead-free soldering conditions
Ave ramp up rate ( $T_L$ to $T_P$ )	3 °C/second max
Preheat time $t_s$ ( $T_{smin}=150^\circ\text{C}$ to $T_{smax}=200^\circ\text{C}$ )	60-120 seconds
Melting time $t_L$ ( $T_L=217^\circ\text{C}$ )	60-150 seconds
Peak temp $T_P$	260-265 °C
5°C below peak temperature $t_P$	30 seconds
Ave cooling rate ( $T_P$ to $T_L$ )	6 °C/second max
Normal temperature 25°C to peak temperature TP time	8 minutes max

**Important statement**

SIT reserves the right to change the above-mentioned information without prior notice.



**REVISION HISTORY**

Version number	Data sheet status	Revision date
V1.0	Initial version.	October 2018
V1.1	Modified text description of bus output voltage (recessive).	January 2019
V1.2	Modified the drive function table.	February 2019
V1.3	Modified the text error of low-level input current of TXD port.	February 2019
V1.4	Modified SPLIT withstand voltage parameters; Modified function table.	March 2019
V1.5	Modified the description text.	April 2019
V1.6	Modified the description of over temperature protection.	May 2019
V1.7	Added DFN3*3-8 package.	June 2019
V1.8	Added DFN3*3-8 ordering information.	July 2019
V1.9	Removed DIP8 package.	September 2019
V1.10	Added ESD parameters.	October 2019
V1.11	Removed continuous power consumption.	August 2020
V1.12	Added DFN3*3-8 package dimension drawing.	September 2020
V1.13	Added STB pin characteristics parameters.	December 2020
V1.14	Modified SOP8, DFN3*3-8 package size.	January 2022
V1.15	Modified the range of CANH output voltage (dominant) and CANL output voltage (dominant); Modified the output voltage description of the bus; Modified the order information; Added reflow soldering and tape and reel information; Added the revision history.	July 2022
V1.16	Updated the description of $T_{amb}$ to ambient temperature; Added virtual junction temperature range $T_j$ ; Updated function table; Updated SOP8 package dimension drawing (size unchanged).	April 2023