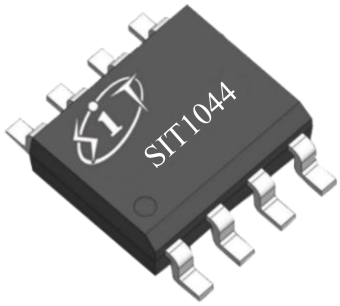
FEATURES

- Fully compatible with the ISO 11898 standard
- Thermally protected
- ±40V BUS protection
- Transmit Data (TXD) dominant time-out function
- Low-power standby mode with wake-up function
- SIT1044T/3 and SIT1044TK/3 can be interfaced directly to microcontrollers with supply voltages from 3.3V to 5V
- Under-voltage protection
- Timing guaranteed for data rates up to 5 Mbps in the (CAN FD) fast phase
- Very low ElectroMagnetic Emission (EME)
- Transceiver in unpowered state disengages from the bus (zero load)
- The typical loop delay from TXD to RXD is less than 100ns
- Provide SOP8 and DFN3*3-8/HVSON8 packages

PRODUCT APPEARANCE



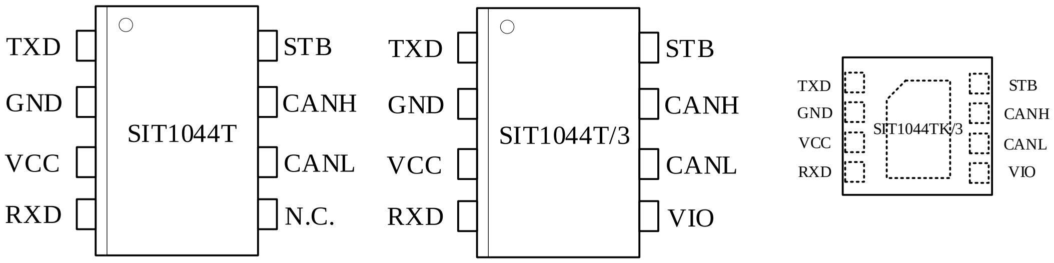
Provide Green and Environmentally Friendly Lead-free package

DESCRIPTION

SIT1044 is an interface chip used between the CAN protocol controller and the physical bus. It can be used in vehicle, industrial control and other fields. It supports 5Mbps (CAN FD) flexible data rate, and has a connection between the bus and the CAN protocol controller. The ability to perform differential signal transmission between the bus and the CAN protocol controller.

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
Supply voltage	VCC		4.75	5.25	V
VIO voltage	VIO		2.95	5.25	V
Maximum transmission rate	$1/t_{bit}$	Non-return to zero code	5		Mbaud
CANH/CANL input or output voltage	V_{can}		-40	+40	V
Bus differential voltage	V_{diff}		1.5	3.0	V
Virtual junction temperature	T_j		-40	150	℃

PIN CONFIGURATION



PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	TXD	transmit data input
2	GND	ground
3	VCC	supply voltage
4	RXD	receive data output; reads out data from the bus lines
5	VIO	transceiver I/O level conversion power supply voltage (SIT1044T/3)
5	N.C.	not connected (SIT1044T)
6	CANL	LOW-level CAN bus line
7	CANH	HIGH-level CAN bus line
8	STB	standby mode control input

Note: The metal pad on the back of the SIT1044TK/3 package is recommended to be grounded.

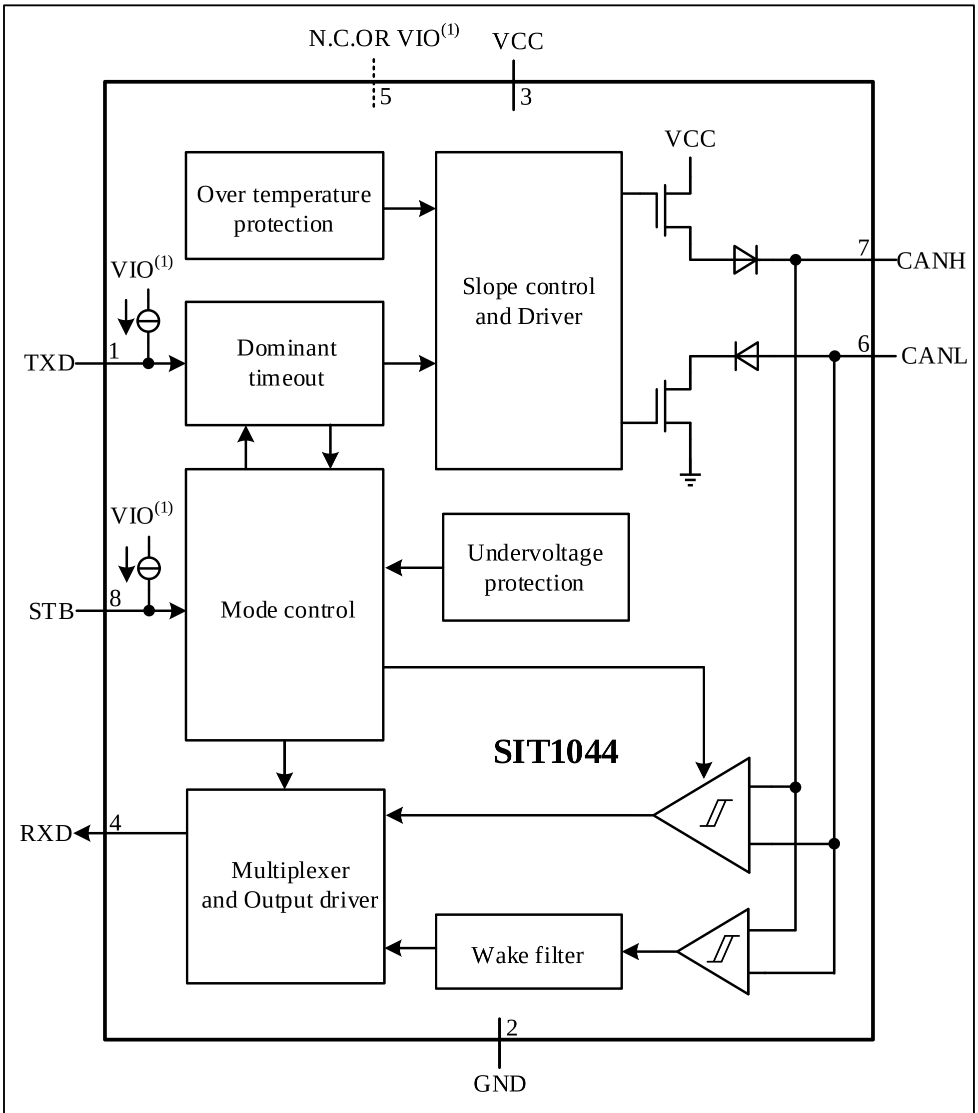
LIMITING VALUES

PARAMETER	SYMBOL	VALUE	UNIT
Supply voltage	VCC	-0.3~+7	V
MCU side port	TXD, RXD, STB, VIO	-0.3~+7	V
Bus side input voltage	CANL, CANH	-40~+40	V
Bus differential breakdown voltage	$V_{CANH-CANL}$	-27~27	V
Storage temperature	T_{stg}	-55~150	℃
Virtual junction temperature	T_j	-40~150	℃
Ambient temperature	T_{amb}	-40~125	℃

PARAMETER	SYMBOL	VALUE	UNIT
Welding temperature range		300	℃
Continuous power consumption	SOP8	400	mW

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

FUNCTIONAL BLOCK DIAGRAM



(1) VIO=VCC in SIT1044T

SIT1044 functional module diagram

DRIVER ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
CANH dominant output voltage	$V_{OH(D)}$	TXD=0V, STB=0V, R_L=50Ω to 65Ω, Fig.1, Fig.2	2.75	3.5	4.5	V
CANL dominant output voltage	$V_{OL(D)}$		0.5	1.5	2.25	V
Bus dominant differential output voltage	$V_{OD(D)}$	TXD=0V, STB=0V, $t<t_{dom\_TXD}$				
		R_L=50Ω to 65Ω	1.5		3	V
		R_L=45Ω to 70Ω	1.4		3.3	
		R_L=2240Ω	1.5		5	
Bus recessive differential output voltage	$V_{OD(R)}$	TXD=VIO, STB=VIO, no load	-0.2		0.2	V
		TXD=VIO, STB=0V, no load	-0.5		0.05	V
Bus recessive output voltage	$V_{O(R)}$	STB=0V; TXD=VIO; no load	2	0.5VCC	3	V
		STB=VIO; no load	-0.1		0.1	
Transmitter dominant voltage symmetry	$V_{dom(TX)sym}$	$V_{dom(TX)sym}=VCC-V_{CANH}-V_{CANL}$	-400		400	mV
Transmitter voltage symmetry	V_{TXsym}	$V_{TXsym}=V_{CANH}+V_{CANL}$ (1); f_{TXD}=250kHz,1MHz or 2.5MHz; C_{SPLIT}=4.7nF, Fig.7	0.9VCC		1.1VCC	V
Common-mode output voltage	V_{OC}	STB=0V, Fig.2	2	0.5VCC	3	V
Dominant short-circuit output current	I_{OS_dom}	VTXD=0V; $t<t_{dom\_TXD}$; VCC=5V				
		Pin CANH; CANH=-15V to 40V	-100		100	mA
		Pin CANL; CANL=-15V to 40V	-100		100	mA
Recessive short-circuit output current	$I_{O(R)}$	TXD=VIO; -27V<CANH=CANL<32V	-5		5	mA

(1) Not tested in production; guaranteed by design.

(VCC=5V±5% and -40°C≤T_{amb}≤125°C, unless specified otherwise; typical in VCC=+5V, VIO=+5V and T_{amb}=25°C.)

DRIVER SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Driver timing; pins CANH, CANL, RXD; see Fig.3 and Fig.5 and Fig.6; R_L=60Ω; C_L=100pF; C_{RXD}=15pF.						
Propagation delay time, TXD to bus recessive	$t_{d(TXD\_busrec)}$	STB=0V, Fig.3, Fig.6		90		ns
Propagation delay time, TXD to bus dominant	$t_{d(TXD\_busdom)}$	STB=0V, Fig.3, Fig.6		65		ns
Differential output signal rise time	t_r	STB=0V, Fig.3, Fig.6		45		ns
Differential output signal fall time	t_f	STB=0V, Fig.3, Fig.6		45		ns
Enable time from standby mode to dominant	t_{stb_nom}			10	45	µs
TXD dominant time-out	t_{dom_TXD}	Fig.4	0.8	3	6.5	ms
Bus dominant time-out time	t_{filter_WAKE}	standby, Fig.8	0.5		1.8	µs
Bus wake-up filter time	t_{dom_WAKE}	standby, Fig.8	0.8	3	6.5	ms

(VCC=5V±5% and -40°C≤T_{amb}≤125°C, unless specified otherwise; typical in VCC=+5V, VIO=+5V and T_{amb}=25°C.)

RECEIVER ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Positive-going input threshold voltage	V_{TH+_dif}	Normal mode; -12 V≤V_{CANL} ≤+12 V; -12 V≤V_{CANH}≤ +12V			900	mV
Negative-going input threshold voltage	V_{TH-_dif}	Normal mode; -12 V≤V_{CANL} ≤+12 V; -12 V≤V_{CANH}≤ +12V	500			mV
Hysteresis voltage ($V_{TH+\_dif} - V_{TH-\_dif}$)	V_{HYS}	Normal mode; -12 V≤V_{CANL} ≤+12 V; -12 V≤V_{CANH}≤ +12V		120		mV
Positive-going input threshold voltage	V_{TH+_dif}	Standby mode; -12 V≤V_{CANL} ≤+12 V; -12 V≤V_{CANH}≤ +12 V			1150	mV
Negative-going input threshold voltage	V_{TH-_dif}	Standby mode; -12 V≤V_{CANL} ≤+12 V; -12 V≤V_{CANH}≤ +12 V	400			mV

Receiver dominant differential input voltage	V_{dom_Diff}	Normal mode; -12 V≤V_{CANL} ≤+12 V; -12 V≤V_{CANH}≤ +12 V	0.9		8.0	V
		Standby mode; -12 V≤V_{CANL} ≤+12 V; -12 V≤V_{CANH}≤ +12 V	1.15		8.0	V
Receiver recessive differential input voltage	V_{rec_Diff}	Normal mode; -12 V≤V_{CANL} ≤+12 V; -12 V≤V_{CANH}≤ +12 V	-3		0.5	V
		Standby mode; -12 V≤V_{CANL} ≤+12 V; -12 V≤V_{CANH}≤ +12 V	-3		0.4	V
Power-off bus input current	$I_{(OFF)}$	CANH=CANL=5V, GND=VCC=VIO=0V	-5		5	μA
Input capacitance to ground, (CANH or CANL)	C_I	(1)			24	pF
Differential input capacitance	C_{ID}	(1)			12	pF
Slew Rate	SR	Edge dominant to recessive (1)			70	V/μs
Input resistance, (CANH or CANL)	R_{IN}	TXD=VIO, STB=0V; (1) -2 V≤VCANL ≤+7 V; -2 V≤VCANH≤ +7 V;	9	15	28	kΩ
Differential input resistance	R_{ID}		19	30	52	kΩ
Input resistance matching	RI_{match}	CANH=CANL; (1) 0 V≤VCANL ≤+5 V; 0 V≤VCANH≤ +5 V;	-2		2	%
The range of common-mode voltage	V_{COM}		-12		12	V

(1) Not tested in production; guaranteed by design.

(VCC=5V±5% and -40°C≤T_{amb}≤125°C, unless specified otherwise; typical in VCC=+5V, VIO=+5V and T_{amb}=25°C.)

RECEIVER SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Receive timing; pins CANH, CANL, RXD; see Fig.3 and Fig.5 and Fig.6; R_L=60Ω; C_L=100pF; C_{RXD}=15pF;						
Propagation delay time, bus recessive to RXD	$t_{d(busrec\_RXD)}$	STB=0V, Fig3, Fig.6		65		ns
Propagation delay time, bus dominant to RXD	$t_{d(busdom\_RXD)}$	STB=0V, Fig3, Fig.6		60		ns
RXD signal rise time	t_r	STB=0V, Fig3, Fig.6		10		ns
RXD signal fall time	t_f	STB=0V, Fig3, Fig.6		10		ns

(VCC=5V±5% and -40°C≤T_{amb}≤125°C, unless specified otherwise; typical in VCC=+5V, VIO=+5V and T_{amb}=25°C.)

DEVICE SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Transceiver timing; pins CANH, CANL, TXD and RXD; see Fig.3 and Fig.5 and Fig.6; R_L=60Ω; C_L=100pF; C_{RXD}=15pF.						
Loop delay1, driver input to receiver output, Recessive to Dominant	t_{loop1}	STB=0V, Fig.3, Fig.6		80	220	ns
Loop delay 2, driver input to receiver output, Dominant to Recessive	t_{loop2}	STB=0V, Fig.3, Fig.6		90	220	ns
Bit time of BUS output pin	$t_{bit(BUS)}$	$t_{bit(TXD)}$=500ns (1), Fig.5, Fig.6	435		530	ns
		$t_{bit(TXD)}$=200ns (2), Fig.5, Fig.6	155		210	ns
Bit time of RXD output pin	$t_{bit(RXD)}$	$t_{bit(TXD)}$=500ns (1), Fig.5, Fig.6	400		550	ns
		$t_{bit(TXD)}$=200ns (2), Fig.5, Fig.6	120		220	ns
Receiver timing symmetry	Δtrec	$t_{bit(TXD)}$=500ns (1), Fig.5, Fig.6	-65		+40	ns

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Receiver timing symmetry	Δtrec	$t_{bit(TXD)}$=200ns (2), Fig.5, Fig.6	-45		+15	ns

(1) Transmitted recessive bit width at 2Mbit/s.

(2) Transmitted recessive bit width at 5Mbit/s.

(VCC=5V±5% and -40°C≤T_{amb}≤125°C, unless specified otherwise; typical in VCC=+5V, VIO=+5V and T_{amb}=25°C.)

OVER TEMPERATURE PROTECTION

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Shutdown junction temperature	$T_{j(sd)}$			190		°C

(VCC=5V±5% and -40°C≤T_{amb}≤125°C, unless specified otherwise; typical in VCC=+5V, VIO=+5V and T_{amb}=25°C.)

UNDER-VOLTAGE PROTECTION

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
VCC under-voltage protection	V_{uvd_VCC}		3.5	3.9	4.3	V
VIO under-voltage protection	V_{uvd_VIO}		2.1	2.5	2.7	V

(VCC=5V±5% and -40°C≤T_{amb}≤125°C, unless specified otherwise; typical in VCC=+5V, VIO=+5V and T_{amb}=25°C.)

TXD PIN CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
HIGH-level input current	I_{IH}(TXD)	TXD=VIO	-5		5	μA
LOW-level input current	I_{IL}(TXD)	TXD=0V	-260	-150	-30	μA
When VCC=0V, current on TXD pin	I_O(off)	VCC=VIO=0V，TXD=VIO	-1		1	μA
HIGH-level input voltage	V_{IH}		0.7V_{IO} (1)		V_{IO}(1)+0.3	V
LOW-level input voltage	V_{IL}		-0.3V_{IO} (1)		0.3V_{IO} (1)	V
Open voltage on TXD pin	TXD_O		H			logic

(1) SIT1044T model V_{IO}=V_{CC}.

(VCC=5V±5% and -40°C≤T_{amb}≤125°C, unless specified otherwise; typical in VCC=+5V, VIO=+5V and T_{amb}=25°C.)

STB PIN CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
HIGH-level input current	I_{IH}(STB)	STB=VIO	-2		2	µA
LOW-level input current	I_{IL}(STB)	STB=0V	-15		-1	µA
When VCC=0V， current on STB pin	I_O(off)	VCC=VIO=0V， STB=VIO	-1		1	µA
HIGH-level input voltage	V_{IH}		$0.7V_{IO}$ (1)		V_{IO}(1)+0.3	V
LOW-level input voltage	V_{IL}		$-0.3V_{IO}$ (1)		$0.3V_{IO}$ (1)	V
Open voltage on STB pin	STB_O		H			logic

(1) SIT1044T model $V_{IO}=V_{CC}$;

(VCC=5V±5% and -40°C≤T_{amb}≤125°C, unless specified otherwise; typical in VCC=+5V, VIO=+5V and T_{amb}=25°C.)

RXD PIN CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
HIGH-level input current	I_{OH}(RXD)	VIO=VCC, RXD=VIO-0.4V	-8	-3	-1	mA
LOW-level input current	I_{OL}(RXD)	RXD=0.4V, bus dominant	1		12	mA
When VCC=0V， current on STB pin	I_O(off)	VCC=VIO=0V, RXD=VIO	-1		1	µA

(VCC=5V±5% and -40°C≤T_A≤125°C, unless specified otherwise; typical in VCC=+5V, VIO=+5V and T_A=25°C.)

SUPPLY CURRENT

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
VCC current (standby mode)	I_{CC}	STB=VCC, TXD=VIO, SIT1044T/3			5	μA
		STB=VCC, XD=VCC, SIT1044T		15	30	μA
VCC current (Dominant)		TXD=VIO, STB=0V, LOAD=60Ω		45	70	mA
VCC current (Recessive)		TXD=VIO, STB=0V, NO LOAD		5	10	mA
VIO current (standby mode)	I_{IO}	STB=TXD=VIO		14	28	μA
VIO current (Dominant)		TXD=0V, STB=0V		180	500	μA
VIO current (Recessive)		TXD=VIO, STB=0V		30	200	μA

(VCC=5V±5% and -40℃≤T_{amb}≤125℃, unless specified otherwise; typical in VCC=+5V, VIO=+5V and T_{amb}=25℃.)

ESD PERFORMANCE

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
CAN bus pin contact discharge model (IEC)	V_{ESD_IEC}	IEC 61000-4-2: Contact discharge	-4		+4	kV
CAN bus pin human body discharge model (HBM)	V_{ESD_HBM}		-8		+8	kV

FUNCTION TABLE

Table1. CAN TRANSCEIVER TRUTH TABLE

TXD (1)	STB (1)	CANH (1)	CANL (1)	BUS STATE	RXD (1)
L	L	H	L	Dominate	L
H or Open	L	0.5VCC	0.5VCC	Recessive	H
X	H or Open	GND	GND	Recessive	H

(1) H=high level; L=low level; X=irrelevant.

Table 2. RECEIVER FUNCTION TABLE

V_{ID}=CANH-CANL	RXD (1)	Bus State (1)
$V_{ID} \geq 0.9V$	L	Dominate
$0.5 < V_{ID} < 0.9V$	?	?
$V_{ID} \leq 0.5V$	H	Recessive
Open	H	Recessive

(1) H=high-level; L=low-level; ?=uncertain.

Table 3. UNDER-VOLTAGE PROTECTION STATUS TABLE

VCC	VIO (1)	BUS STATE	BUS OUT (2)	RXD (2)
$VCC>V_{uvd\_VCC}$	$VIO>V_{uvd\_VIO}$	normal	According to STB and TXD	Follow the bus
$VCC<V_{uvd\_VCC}$	$VIO>V_{uvd\_VIO}$	Protected state	GND	H
$VCC>V_{uvd\_VCC}$	$VIO<V_{uvd\_VIO}$	Protected state	Z	H
$VCC<V_{uvd\_VCC}$	$VIO<V_{uvd\_VIO}$	Protected state	Z	H

(1) Only SIT1044T/3 version;

(2) H=high level; Z=high impedance state.

TEST CIRCUIT

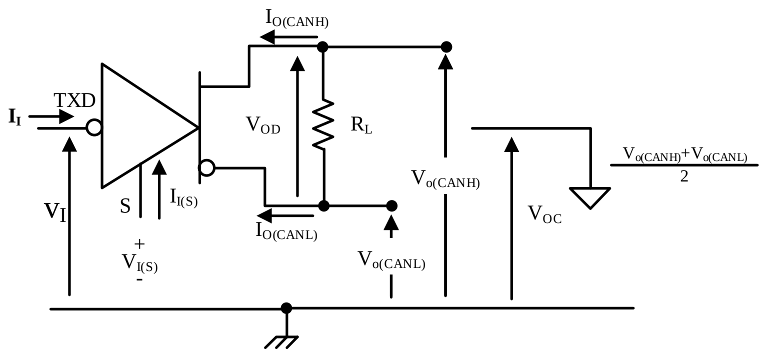


Fig.1 Driver Voltage, Current, and Test Definition

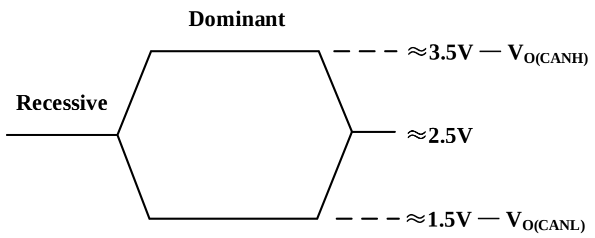


Fig.2 Bus Logic State Voltage Definition

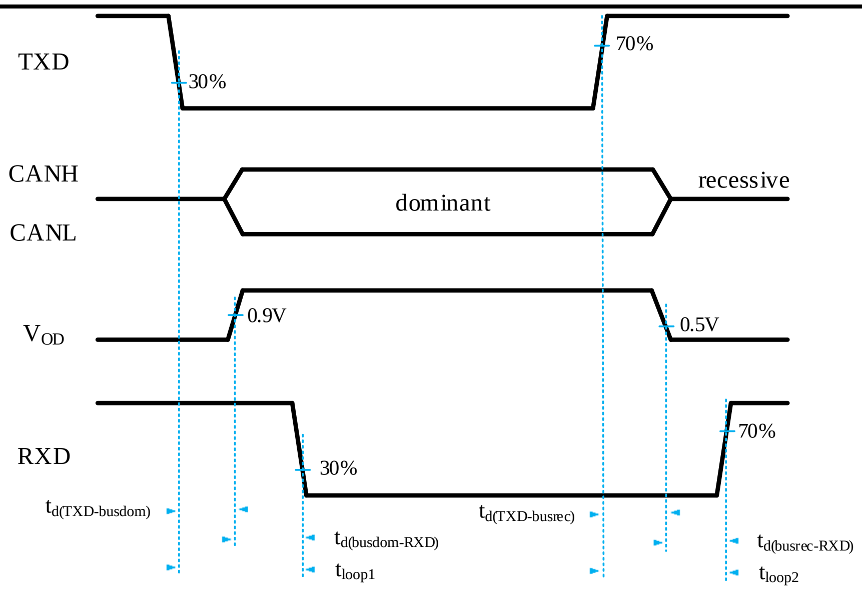
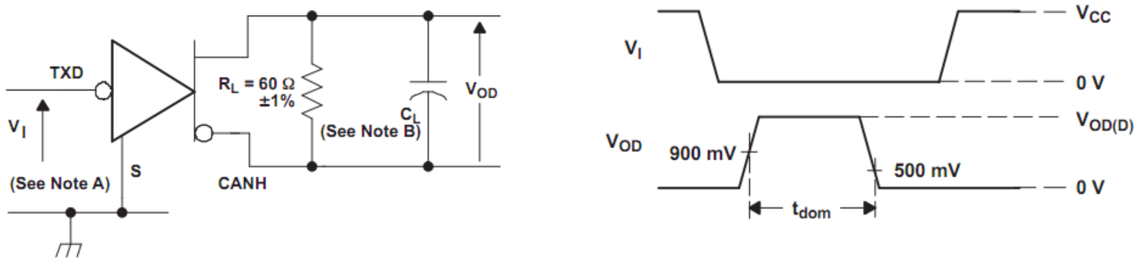


Fig.3 Transceiver timing diagram



A. The input pulse is supplied by a generator having the following characteristics: $t_r \le 6$ ns, $t_f \le 6$ns, $Z_O = 50\ \Omega$;

B. C_L includes instrumentation and fixture capacitance with ±20%.

Fig.4 Dominant overtime test circuit and waveform

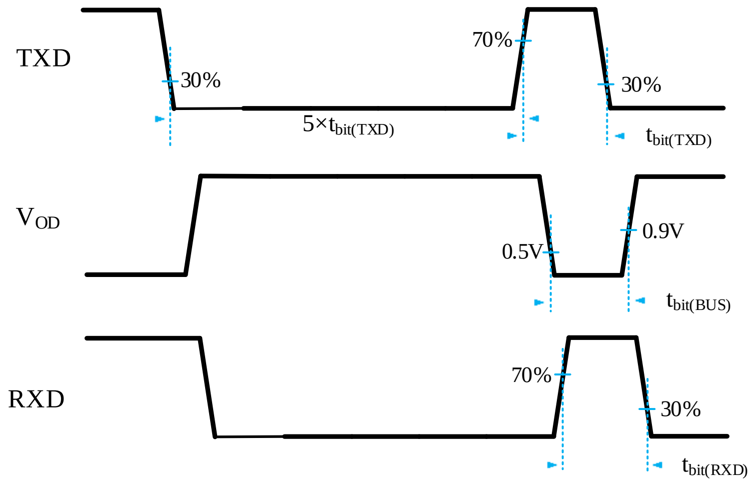
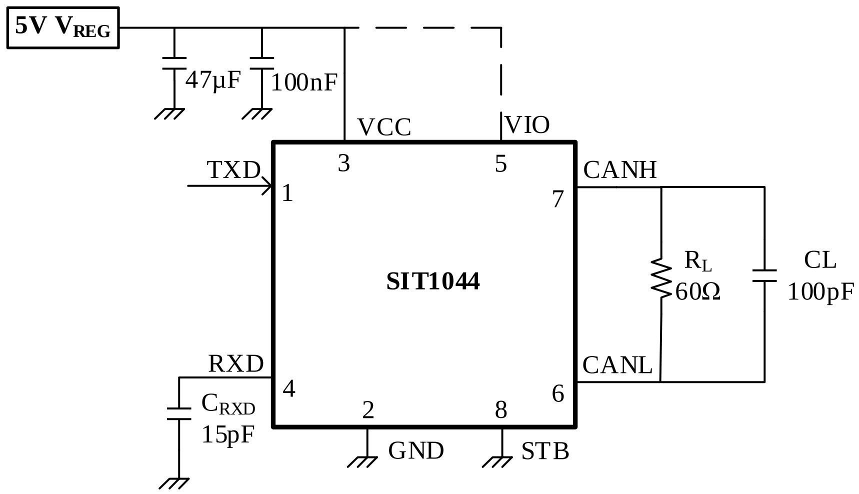


Fig.5 t_{bit} test circuit and waveform



The VIO pin is internally connected to pin VCC in the non-VIO product variants SIT1044T

Fig.6 CAN transceiver timing test circuit

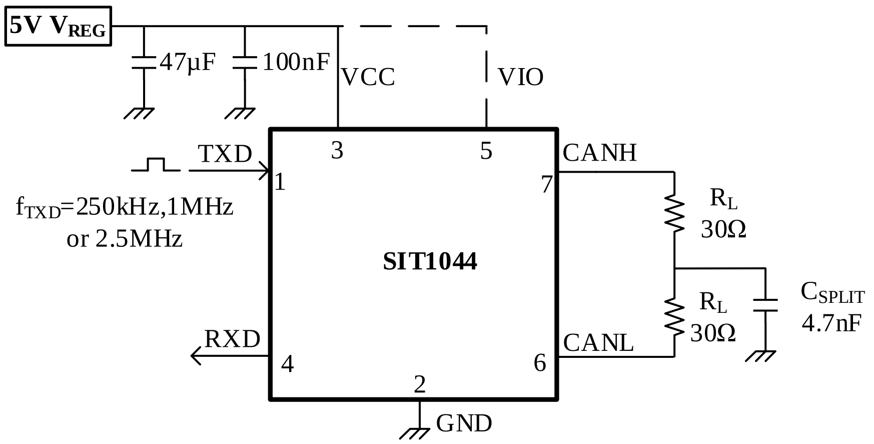
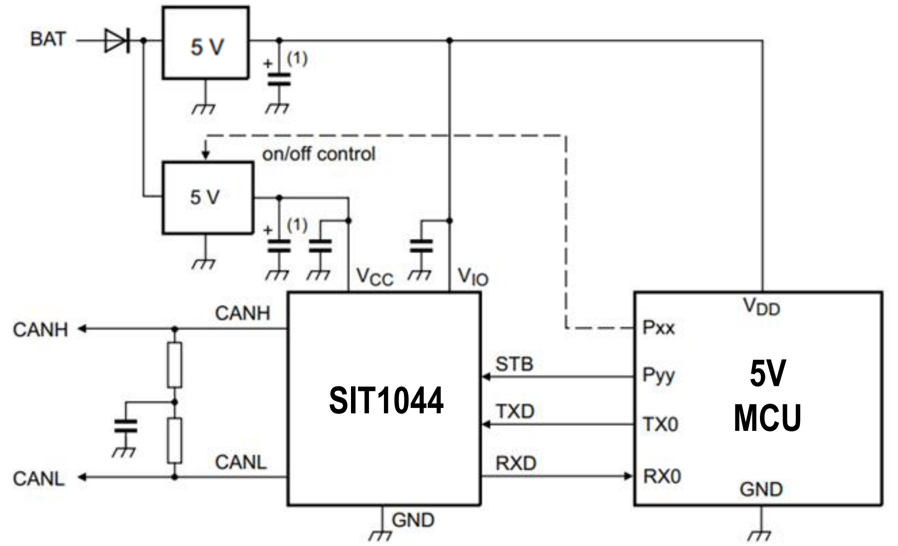


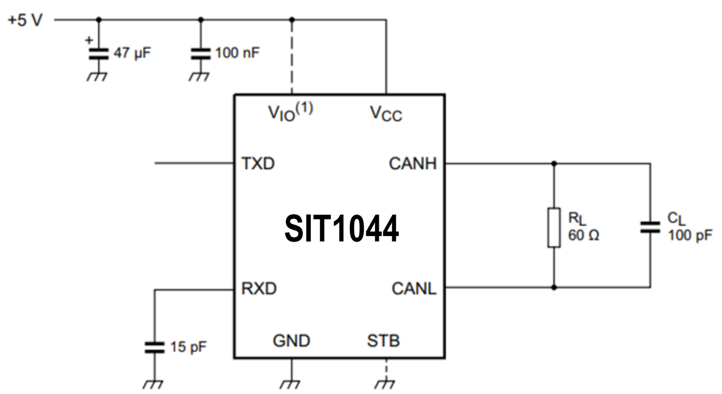
Fig.7 Test circuit for measuring transmitter driver symmetry

TYPICAL APPLICATION TEST INFORMATION



（1） SIT1044T/3 can be applied to 3V or 5V MCU

SIT1044 typical application diagram



（1） VIO is limited to SIT1044T/3, VIO=VCC in SIT1044T

SIT1044 typical high-speed mode test chart

ADDITIONAL DESCRIPTION

1 Sketch

SIT1044 is an interface chip applied between the CAN protocol controller and the physical bus. It can be used in vehicle, industrial control and other fields. It supports 5Mbps (CAN FD) flexible data rate, and has a connection between the bus and the CAN protocol controller. The ability to perform differential signal transmission between them is fully compatible with the "ISO 11898-2: 2016" standard.

2 Over temperature protection

SIT1044 has an over-temperature protection function. After the over-temperature protection is triggered, the drive tube will be turned off, because the drive tube is the main energy-consuming component. Turning off the drive tube can reduce power consumption and thus reduce the chip temperature. At the same time, other parts of the chip are still working normally.

3 Under-voltage protection

The SIT1044 power supply pin has an under-voltage detection function, which can put the device in a protected mode. This protects the bus when VCC is lower than V_{uvd_VCC} or VIO is lower than V_{uvd_VIO} (if applicable).

4 Operating modes

The control pin STB allows two working modes to be selected: high-speed mode and standby mode.
The high-speed mode is a normal operating mode and is selected by grounding the pin STB. Both the CAN driver and the receiver can operate normally and CAN communication is carried out in both directions.
Set the pin STB to high level, and the standby module will detect the signal on the bus. When complete dominant-recessive-dominant pattern within t_{dom_WAKE} to be recognized as a valid wake up pattern (see Figure12) Otherwise, the internal wake up is reset. The complete wake up pattern will then need to be re-transmitted to trigger a wake-up event. Pin RXD remains HIGH until the wake-up event has been triggered.

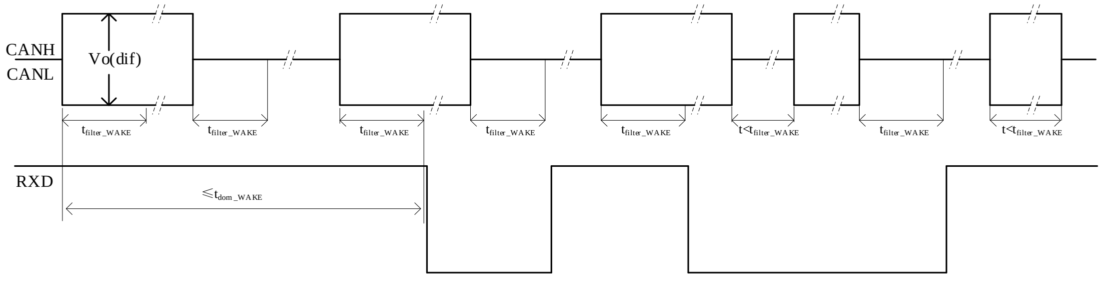


Fig.8 Wake-up timing

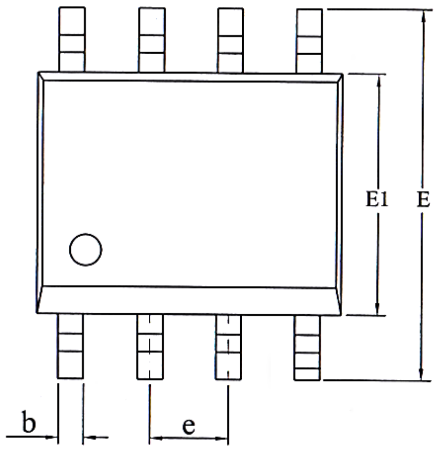
5 Dominant timeout function

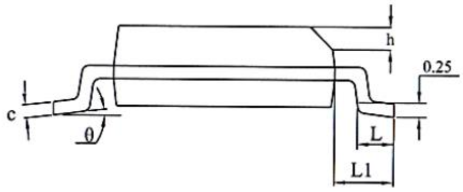
In high-speed mode, if the low-level duration on pin TXD exceeds the internal timer value (t_{dom_BUS}), the transmitter will be disabled and drive the bus into a recessive state. It can prevent the pin TXD from being forced to a permanent low level due to a hardware or software application failure, causing the bus line to be driven to a permanent dominant state (blocking all network communications). A rising edge signal on pin TXD can be reset.

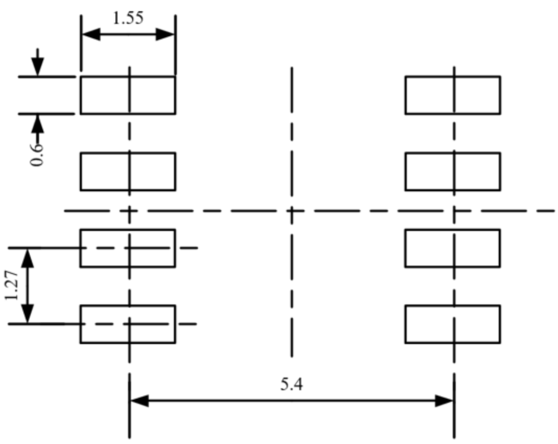
SOP8 DIMENSIONS

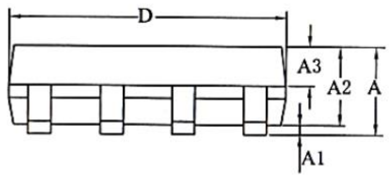
PACKAGE SIZE

SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	1.40	-	1.80
A1	0.10	-	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.38	-	0.51
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.40	0.60	0.80
L1	1.05REF		
c	0.20	-	0.25
θ	0°	-	8°







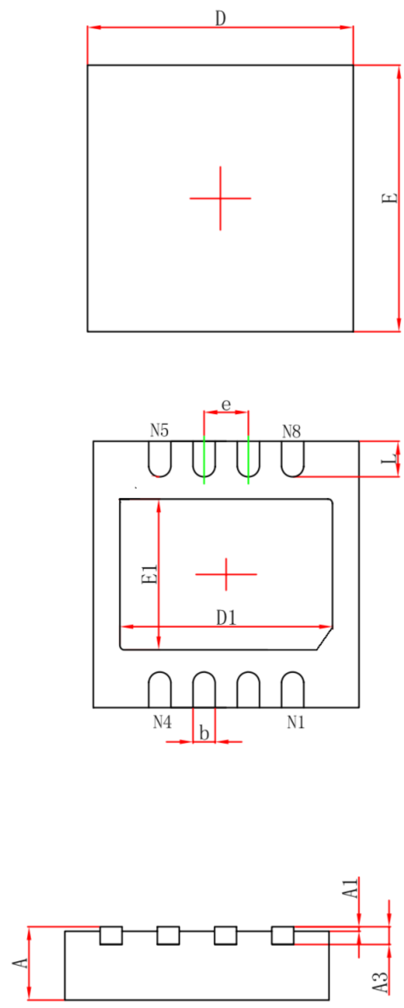


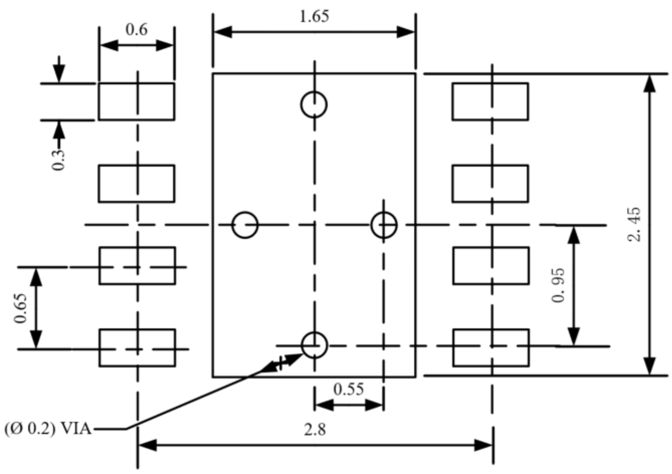
LAND PATTERN EXAMPLE (Unit: mm)

DFN3*3-8/HVSON8 DIMENSIONS

PACKAGE SIZE

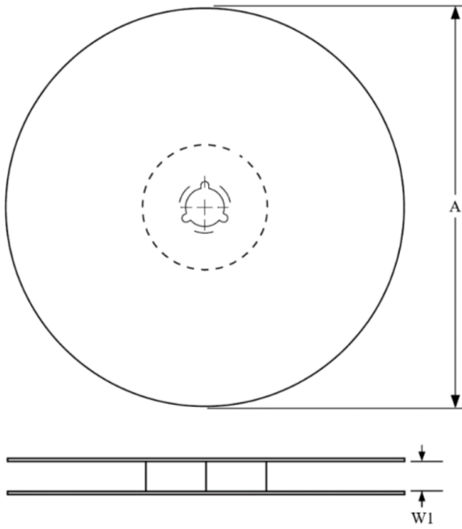
SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	0.70		0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	2.35	2.45	2.55
E1	1.55	1.65	1.75
b	0.2	0.25	0.33
e	0.65 TYP		
L	0.35		0.45



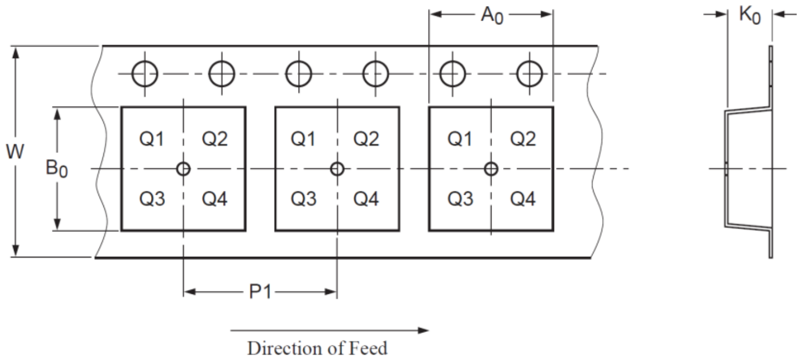


LAND PATTERN EXAMPLE (Unit: mm)

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



PIN1 is in quadrant 1

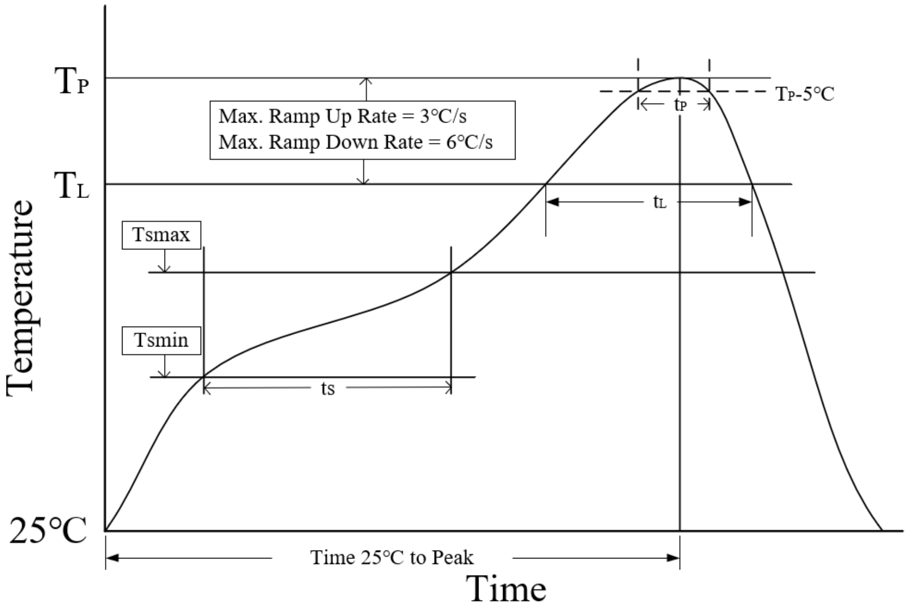
Package Type	Reel Diameter A (mm)	Tape Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
SOP8	330±1	12.4	6.60±0.1	5.30±0.10	1.90±0.1	8.00±0.1	12.00±0.1
DFN3*3-8	329±1	12.4	3.30±0.1	3.30±0.1	1.10±0.1	8.00±0.1	12.00±0.3

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	PACKING
SIT1044T	SOP8	Tape and reel
SIT1044T/3	SOP8	Tape and reel
SIT1044TK/3	DFN3*3-8/HVSON8, Small shape, no leads, 8 terminals	Tape and reel

SOP8 is packed with 2500 pieces/disc in braided packing. Leadless DFN3*3-8/HVSON8 is packed with 5000 pieces/disc in braided packing.

REFLOW SOLDERING



Parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	3 °C/second max
Preheat time ts (T_{smin}=150 °C to T_{smax}=200 °C)	60-120 seconds
Melting time t_L (T_L=217 °C)	60-150 seconds
Peak temp T_P	260-265 °C
5°C below peak temperature t_P	30 seconds
Ave cooling rate (T_P to T_L)	6 °C/second max
Normal temperature 25°C to peak temperature T_P time	8 minutes max

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Data sheet status	Revision date
V1.0	Initial version	April 2021
V1.1	Modified the typical value of t_{loop1}; Modified the typical value of t_{loop2}; Modified the VCC standby mode current of the SIT1044T; Modified VIO standby mode current, VIO dominant current, VIO recessive current;	July 2021
V1.2	Added DFN3*3-8/HVSON8, small outline, leadless package; Added DFN pin diagram;	August 2021
V1.3	Added TXD and STB pin input voltage description for SIT1044T/3；	October 2021
V1.4	Added slew rate indicator and added superscript description；	December 2021
V1.5	Modified the busbar withstand voltage index; Modified package size；	January 2022
V1.6	Added test conditions for dominant differential voltage; Added differential voltage test index; increased bus output voltage condition; increased output voltage symmetry condition; modified explicit and recessive output short-circuit current index; added superscript description; Added receiver threshold test conditions； Added dominant and recessive output differential voltage indicators； Added input differential resistor and Input resistance matching； Added receive timing condition； Added transceiver timing description conditions； Increased receive time symmetry parameter； Modified the high-level input current of the STB； Deleted the driver VOD test circuit in Figure 3, and add the transceiver timing diagram; Deleted the driver test circuit and voltage waveform diagram in Figure 4; Deleted the definition of receiver voltage and current in Figure 5; Deleted the receiver test circuit and voltage waveform in Figure 6; Deleted the common mode output voltage test and waveform in Figure 7; Deleted the t_{loop} test circuit and waveform in Figure 8; Deleted the short-circuit current test and waveform of the driver in Figure 10;	April 2022

Version number	Data sheet status	Revision date
	Added Figure 6 Transceiver Test Circuit; Added Figure 7 Transceiver Driver Symmetry Test Circuit.	
V1.7	Updated SOP8 package dimensions diagram (size unchanged).	January 2023
V1.8	Added the limit value of ambient temperature T_{amb}; Updated the test condition of electrical characteristics; Updated the parameters of VIL on TXD and STB pins.	June 2023