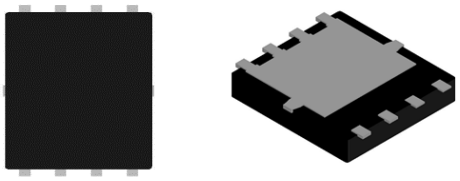
FEATURES

- Drain-Source Withstand Voltage: 80V
- Max. $R_{DS(on)}$: 18.0mΩ @ V_{GS}=10V
  30.0mΩ @ V_{GS}=4.5V
- Automotive applications
- AEC-Q101 Qualified
- Excellent ON resistance
- General footprint package PDFN5×6-8L
- 100% Rg and Avalanche tested
- MSL1

PRODUCT APPEARANCE



PDFN5×6-8L

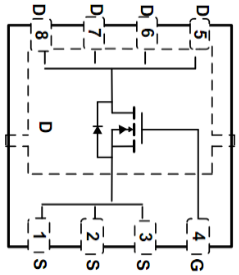
DESCRIPTION

The SNM0818DNAQ is N-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in high performance automotive DC-DC conversion, power switch and charging circuit. Standard Product SNM0818DNAQ is in compliance with RoHS.

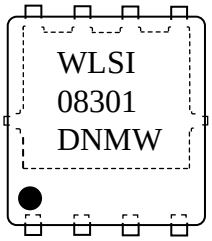
Applications:

- Automotive systems
- DC/DC converters
- Power supply converters circuit
- Load/Power Switching for portable device

PIN CONFIGURATION



MARKING



WLSI = Company (Group) Code
08301 = Device Code
DN = Special Code
M = Month
W = Week

LIMITING VALUES

Parameter	Symbol	Condition	Value	Unit
Drain-Source Voltage	V_{DS}		80	V
Gate-Source Voltage	V_{GS}		±20	V
Continuous Drain Current (4)	I_D	T_C=25°C	38	A
		T_C=100°C	27	A
Pulsed Drain Current (3)	I_{DM}		84	A
Continuous Drain Current	I_D	T_A=25°C	8.9	A
		T_A=100°C	6.3	A
Avalanche Energy L=0.3mH	E_{AS}		33	mJ
Power Dissipation (2)	P_D	T_C=25°C	56	W
		T_C=100°C	28	W
Power Dissipation (1)	P_D	T_A=25°C	3.0	W
		T_A=25°C	1.5	W
Operating Junction Temperature	T_J		-55 to 175	°C
Storage Temperature Range	T_{STG}		-55 to 175	°C

THERMAL RESISTANCE RATINGS

Single Operation					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Junction-to-Ambient Thermal Resistance (1)	Steady State	$R_{\theta JA}$	41	49	°C/W
Junction-to-Case Thermal Resistance (2)	Steady State	$R_{\theta JC}$	1.9	2.7	

ELECTRONICS CHARACTERISTICS

Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0 V, I_D = 250μA	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	BV_{DSS}/T_J			41.4		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V, V_{GS}= 0V, T_J=25°C			1	μA
		V_{DS}=80V, V_{GS}= 0V, T_J=125°C			250	μA
Gate-to-source Leakage Current	I_{GSS}	V_{DS}=0 V, V_{GS}= 20V			100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS}=V_{DS}, I_D= 250μA	1.3	1.7	2.1	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-4.6		mV/°C
Drain-to-source On-resistance (4)	$R_{DS(on)}$	V_{GS} =10V, I_D =10A		14.0	18.0	mΩ
		V_{GS} =4.5V, I_D =10A		22.0	30.0	
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0V, f = 1.0MHz, V_{DS}=25 V		685		pF
Output Capacitance	C_{OSS}			360		
Reverse Transfer Capacitance	C_{RSS}			35		
Total Gate Charge (5)	$Q_{G(TOT)}$	V_{GS}=10V, V_{DS}= 64V, I_D =10A		15.2		nC
Total Gate Charge (5)	$Q_{G(TOT)}$	V_{GS}=4.5V, V_{DS}= 64V, I_D =10A		8.0		

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Gate-to-Source Charge (5)	Q_{GS}	V_{GS}=10V, V_{DS}= 64V, I_D =10A		2.2		
Gate-to-Drain Charge (5)	Q_{GD}			3.7		
Gate Resistance	Rg	f = 1MHz		1.0		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	td(ON)	V_{GS}=4.5V, V_{DS}= 64V, I_D=10A, R_G=1Ω		7.5		ns
Rise Time	tr			2.8		
Turn-Off Delay Time	td(OFF)			12.3		
Fall Time	tf			6.4		
Body Diode Reverse Recovery Time	trr	I_F=10A, dI/dt= 100A/μs		26.5		ns
Body Diode Reverse Recovery Charge	Qrr	I_F=10A, dI/dt= 100A/μs		16.0		nC
BODY DIODE CHARACTERISTICS						
Forward Voltage (4)	V_{SD}	V_{GS}=0 V, I_S=10A	0.5	0.85	1.2	V

(T_J=25℃, unless otherwise noted.)

Note:

(1) FR-4 board (38mm×38mm×t1.6mm, 70μm Copper) partially covered with copper (645mm^2 area). The power dissipation P_{DSM} is based on Junction-to-Ambient thermal resistance value and the $T_{J(MAX)}$=175°C. The value is only for reference, any application depends on the user's specific board design.

(2) The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

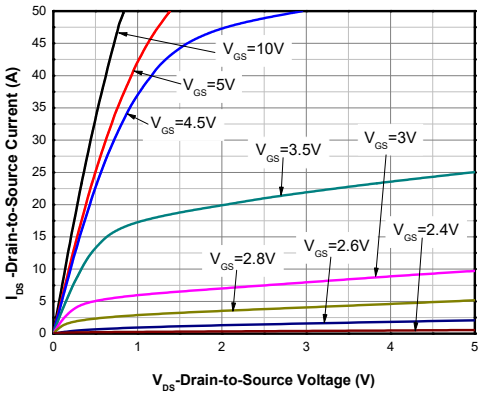
(3) Repetitive rating, pulsed, duty cycle ~1%, keep initial T_J=25°C, the maximum allowed junction temperature of 175°C.

(4) The static characteristics are obtained using ~380μs pulse, duty cycle ~1%.

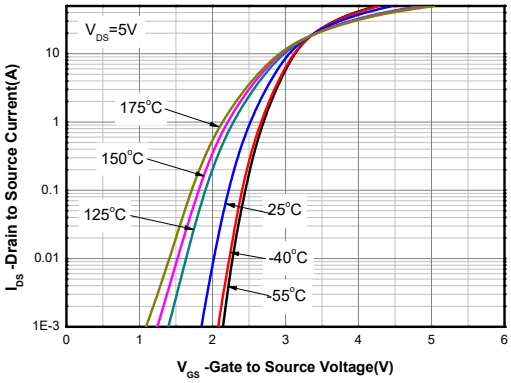
(5) The parameter is not subject to production test – verified by design / characterization.

TYPICAL CHARACTERISTICS

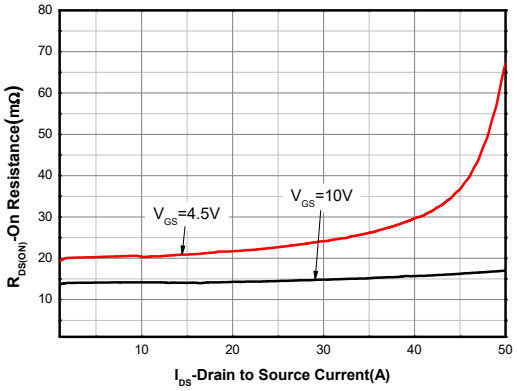
Ta=25℃, unless otherwise noted.



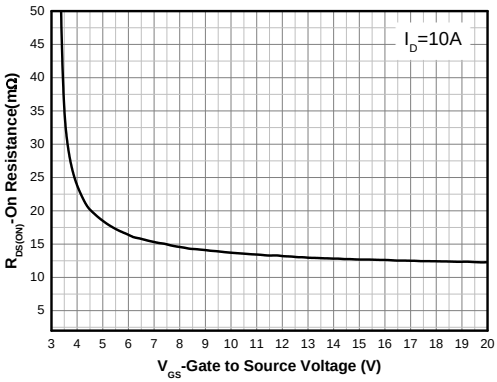
Output Characteristics [(4)]



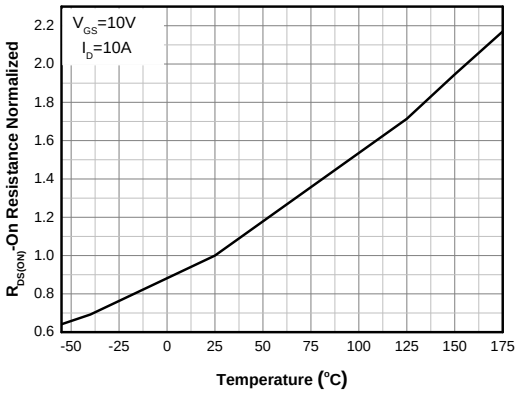
Transfer Characteristics [(4)]



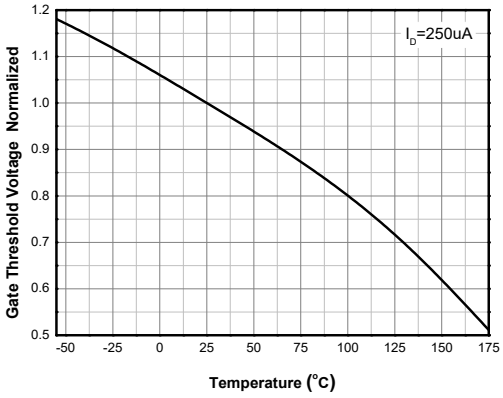
On-Resistance vs. Drain Current [(4)]



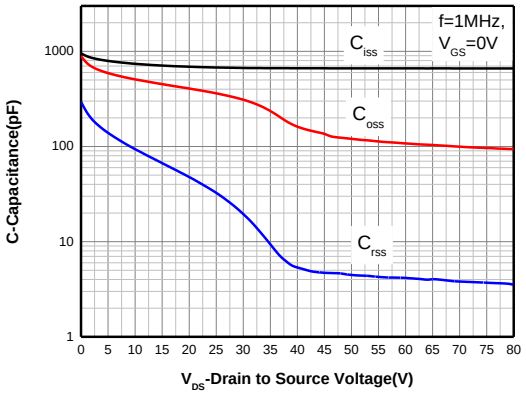
On-Resistance vs. Gate-to-Source Voltage [(4)]



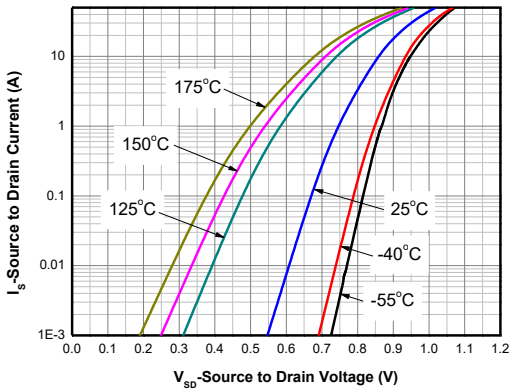
On-Resistance vs. Junction Temperature [(4)]



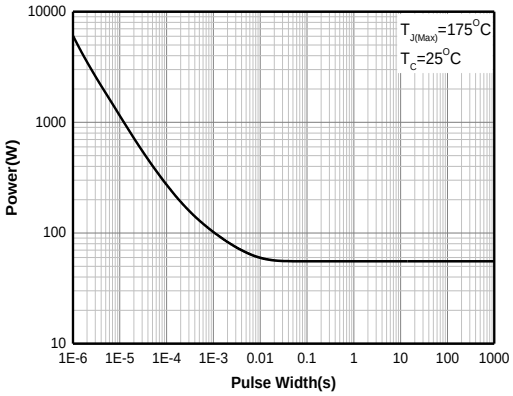
Threshold Voltage vs. Temperature



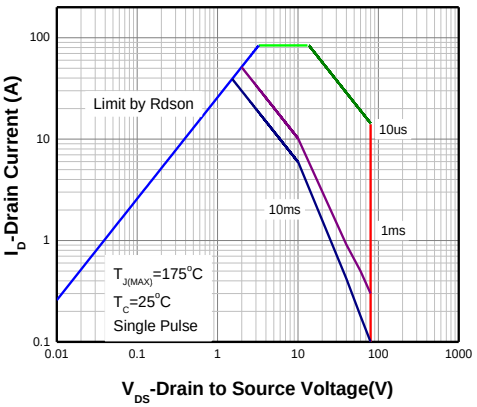
Capacitance



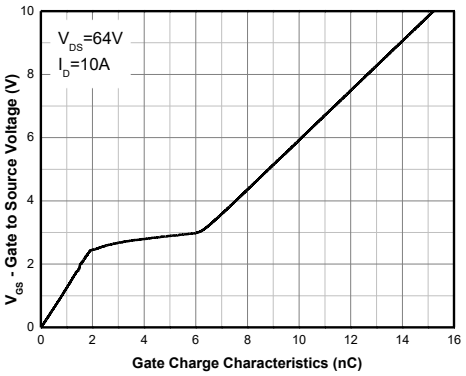
Body Diode Forward Voltage [(4)]



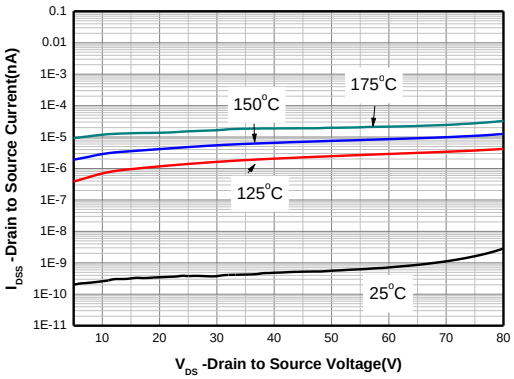
Single Pulse power



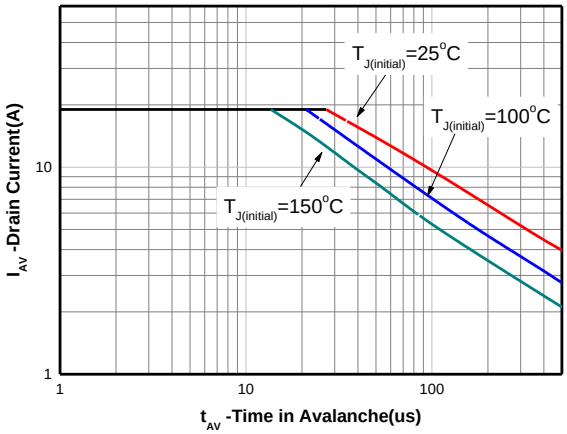
Safe Operating Area



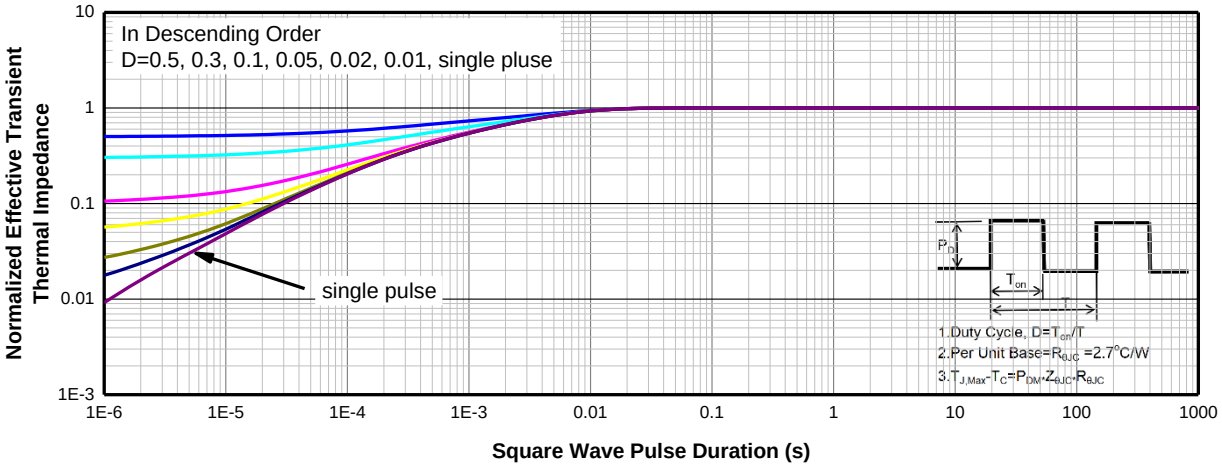
Gate Charge Characteristics



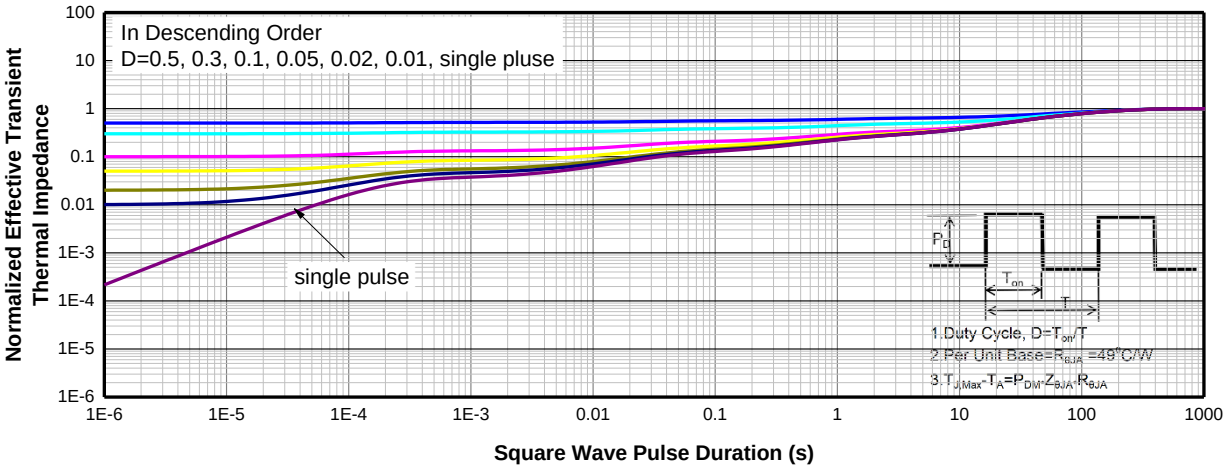
Drain Current vs. Drain Voltage



Avalanche characteristics



Transient Thermal Response (Junction-to-Case)

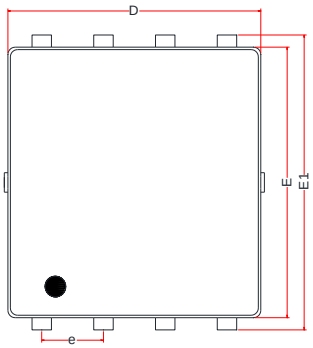


Transient Thermal Response (Junction-to-Ambient)

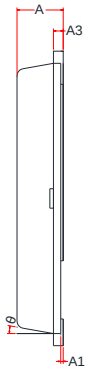
PDFN5×6-8L DIMENSIONS

PACKAGE SIZE

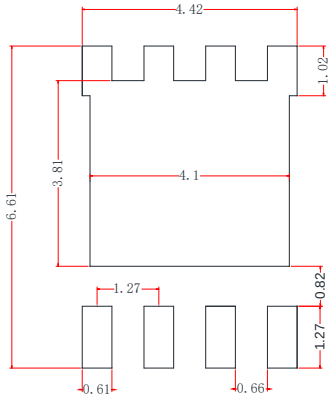
Symbol	Min.	Typ.	Max.
A	0.85	0.95	1.00
A1	0.00	---	0.05
A3	---	0.2 Ref	---
b	0.30	0.40	0.50
D	5.10	5.20	5.30
E	5.45	5.55	5.65
e	1.27 BSC		
D1	4.25	4.35	4.45
E1	5.95	6.05	6.15
E2	3.525	3.625	3.725
E3	1.175	1.275	1.375
L	0.45	0.55	0.65
L1	0	---	0.15
L2	0.68 Ref		
θ	0 °	---	10 °



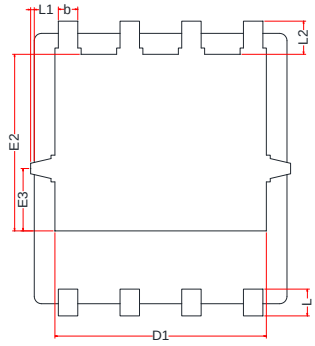
TOP VIEW



SIDE VIEW



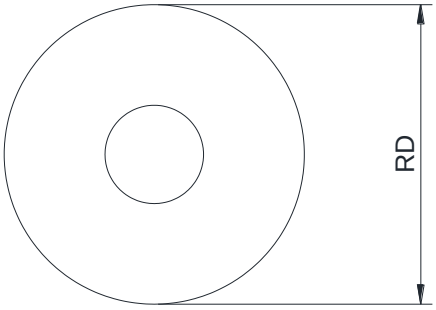
RECOMMENDED LAND PATTERN(Unit:mm)



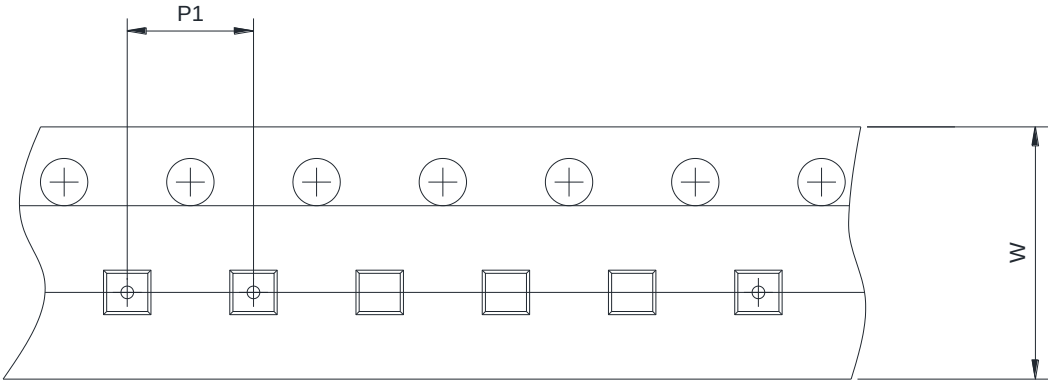
BOTTOM VIEW

TAPE AND REEL INFORMATION

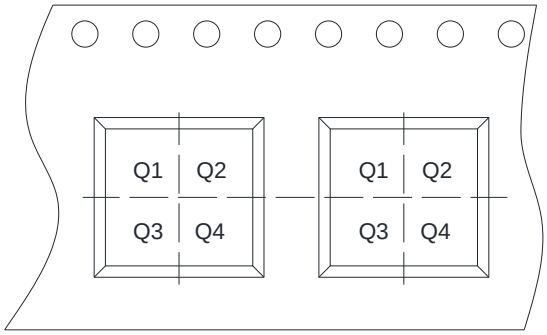
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



User Direction of Feed

RD	Reel Dimension	☐ 7inch	☑ 13inch		
W	Overall width of the carrier tape	☐ 8mm	☑ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☐ 4mm	☑ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	PACKING
SNM0818DNAQ-8/TR	PDFN5×6-8L	Tape and reel

PDFN5×6-8L is packed with 5000 pieces/disc in braided packaging.

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Datasheet status	Revision date
V1.0	Initial version.	April 2024