

**FEATURES**

- Fully compatible with the ISO 11898 standard
- Thermally protected
- High CMTI: 100 kV/μs
- Transmit Data (TXD) dominant time-out function
- Bus fault protection of -40V to +40V
- Input levels compatible with 3.3 V and 5 V devices
- Low loop delay: 150ns (Typical) 210ns (Max)
- At least 110 nodes can be connected
- High speed (up to 1 Mbaud)
- High system level EMC performance
- packages: DUB8  $V_{ISO}=2500 V_{RMS}$   
SOPW16,  $V_{ISO}=5000 V_{RMS}$

**PRODUCT APPEARANCE**

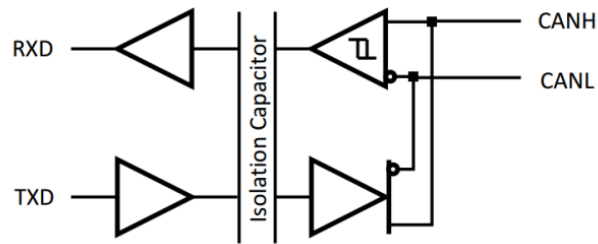

Provide green and environmentally friendly lead-free package

**DESCRIPTION**

SIT1050ISO is a capacitively isolated CAN transponder, which complies with the technical specifications of the ISO11898 standard. It contains multiple logic input and output buffers separated by silicon dioxide (SiO<sub>2</sub>) insulation barriers. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller.

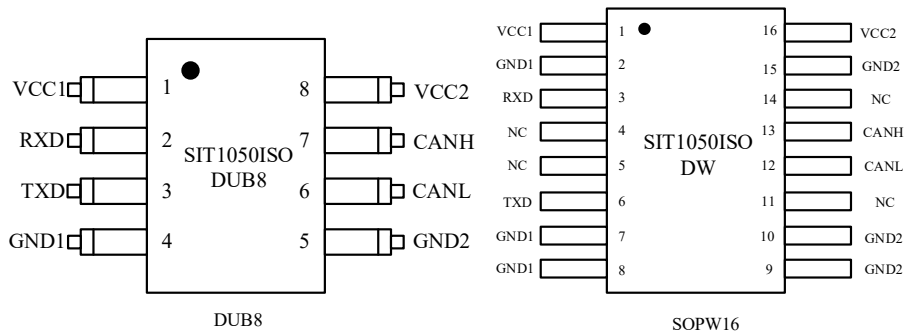
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
<b>WB DUB8</b> Withstand isolation voltage	$V_{ISO}$		2500 typ		$V_{RMS}$
<b>WB SOPW16</b> Withstand isolation voltage	$V_{ISO}$		5000 typ		$V_{RMS}$
<b>Common-Mode Transients</b>	CMTI		50	100	kV/μs
<b>Supply voltage</b>	$V_{CC}$		4.5	5.5	V
<b>Maximum transmission rate</b>	$1/t_{bit}$	Non-return to zero code	1		Mbaud
<b>CANH/CANL input or output voltage</b>	$V_{CAN}$		-40	+40	V
<b>Bus differential voltage</b>	$V_{DIFF}$		1.5	3.0	V
<b>High-level input voltage</b>	$V_{IH}$	TXD	2	5.25	V
<b>Low-level input voltage</b>	$V_{IL}$	TXD	0	0.8	V
<b>High-level output current</b>	$I_{OH}$	Driver	-70		mA

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
High-level output current	$I_{OH}$	Receiver	-4		mA
Low-level output current	$I_{OL}$	Driver		70	mA
		Receiver		4	mA
Virtual junction temperature	$T_j$		-40	150	°C



Function diagram

## PIN CONFIGURATION



## PIN DESCRIPTION

### DUB8 pin description

PIN	SYMBOL	DESCRIPTION
1	VCC1	Power Supply for Logic Side, range 3.0V~5.5V.
2	RXD	Receive data output.
3	TXD	Transmit data input.
4	GND1	Ground 1, the ground reference for Isolator Logic Side.
5	GND2	Ground 2, the ground reference for Isolator Bus Side.
6	CANL	LOW-level CAN bus line.
7	CANH	HIGH-level CAN bus line.

PIN	SYMBOL	DESCRIPTION
8	V <sub>CC2</sub>	Power supply for Bus Side, range 4.5V~5.5V.

**SOPW16 pin description**

PIN	SYMBOL	DESCRIPTION
1	VCC1	Power Supply for Logic Side, range 3.0V~5.5V.
2	GND1	Ground 1, the ground reference for Isolator Logic Side.
3	RXD	Receive data output.
4	NC	No Connection.
5	NC	No Connection.
6	TXD	Transmit data input.
7	GND1	Ground 1, the ground reference for Isolator Logic Side.
8	GND1	Ground 1, the ground reference for Isolator Logic Side.
9	GND2	Ground 2, the ground reference for Isolator Bus Side.
10	GND2	Ground 2, the ground reference for Isolator Bus Side.
11	NC	Not connect.
12	CANL	LOW-level CAN bus line.
13	CANH	HIGH-level CAN bus line.
14	NC	Not connect.
15	GND2	Ground 2, the ground reference for Isolator Bus Side.
16	V <sub>CC2</sub>	Power supply for Bus Side, range 4.5V~5.5V.

**LIMITING VALUES**

PARAMETER	SYMBOL	VALUE	UNIT
Supply voltage	$V_{CC1}, V_{CC2}$	-0.5~+6.5	V
TXD voltage	TXD	-0.5~ $V_{CC1}+0.5$	V
Voltage range at any bus terminal	CANL, CANH	-40~40	V
Transient voltage on pins CANH, CANL see <a href="#">Fig.7</a>	$V_{tr}$	-200~+200	V
Storage temperature	$T_{stg}$	-40~150	°C
Virtual junction temperature	$T_j$	-40~150	°C
Welding temperature range		300	°C

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

**DRIVER ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
CANH dominant output voltage	$V_{OH(D)}$	$V_I=0V, R_L=60\Omega,$ <a href="#">Fig.1, Fig.2</a>	2.9	3.4	4.5	V
CANL dominant output voltage	$V_{OL(D)}$		0.8		1.5	V
Bus recessive output voltage	$V_{O(R)}$	$V_I=3V, R_L=60\Omega,$ <a href="#">Fig.1, Fig.2</a>	2	2.5	3	V
Bus dominant differential output voltage	$V_{OD(D)}$	$V_I=0V, R_L=60\Omega,$ <a href="#">Fig.1, Fig.2</a>	1.5		3	V
Bus recessive differential output voltage	$V_{OD(R)}$	$V_I=3V,$ <a href="#">Fig.1, Fig.2</a>	-0.012		0.012	V
		$V_I=3V, NO\ LOAD$	-0.5		0.05	V
Transmitter dominant voltage symmetry	$V_{dom(TX)sym}$	$V_{dom(TX)sym}=V_{CC}-$ $V_{CANH} - V_{CANL}$	-400		400	mV
Transmitter voltage symmetry	$V_{TXsym}$	$V_{TXsym}= V_{CANH} +$ $V_{CANL}$	$0.9V_{CC}$		$1.1V_{CC}$	V

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Common-mode output voltage	$V_{OC}$	<a href="#">Fig.8</a>	2	2.5	3	V
Peak-to-peak Common-mode output voltage	$\Delta V_{OC}$			30		mV
Short-circuit output current	$I_{OS}$	CANH=-12V, CANL=open, <a href="#">Fig.11</a>	-105	-72		mA
		CANH=12V, CANL=open, <a href="#">Fig.11</a>		0.36	1	mA
		CANL=-12V, CANH=open, <a href="#">Fig.11</a>	-1	0.5		mA
		CANL=12V, CANH=open, <a href="#">Fig.11</a>		71	105	mA
Recessive output current	$I_{O(R)}$	-27V<CANH<32V 0<VCC<5.25V	-2.0		2.5	mA
Common-Mode Transients	CMTI	<a href="#">Fig.12</a>	±50		±100	kV/μs

( $V_{CC1}=V_{CC2}=5V\pm 10\%$ , Temp= $T_{MIN}\sim T_{MAX}$ , typical in  $V_{CC1}=V_{CC2}=+5V$ , Temp=25°C.)

### DRIVER SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation delay time, low-to-high-level output	tPLH	<a href="#">Fig.4</a>	31	65	120	ns
Propagation delay time, low-to-high-level output	tPHL		25	45	90	ns
Differential output signal rise time	tr			25		ns
Differential output signal fall time	tf			50		ns
Bus dominant time-out time	t <sub>dom</sub>	<a href="#">Fig.10</a>	300	450	700	μs

( $V_{CC1}=V_{CC2}=5V\pm 10\%$ , Temp= $T_{MIN}\sim T_{MAX}$ , typical in  $V_{CC1}=V_{CC2}=+5V$ , Temp=25°C.)

**RECEIVER**
**ELECTRICAL**

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Positive-going input threshold voltage	$V_{IT+}$	<a href="#">Fig.5</a>		800	900	mV
Negative-going input threshold voltage	$V_{IT-}$		500	650		mV
Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )	$V_{HYS}$		100	125		mV
High-level output voltage	$V_{OH}$	$I_O = -2mA$ , <a href="#">Fig.6</a>	4	4.6		V
Low-level output voltage	$V_{OL}$	$I_O = 2mA$ , <a href="#">Fig.6</a>		0.2	0.4	V
Power-off bus input current	$I_{(OFF)}$	CANH or CANL=5V, Other pin=0V		165	250	$\mu A$
Input capacitance to ground, (CANH or CANL)	$C_I$			13		pF
Differential input capacitance	$C_{ID}$			5		pF
Input resistance, (CANH or CANL)	$R_{IN}$	TXD=3V	15	30	40	k $\Omega$
Differential input resistance	$R_{ID}$		30		80	k $\Omega$
Input resistance matching	$R_{I_{match}}$	CANH=CANL	-3%		3%	
The range of common-mode voltage	$V_{COM}$		-12		12	V

( $V_{CC1} = V_{CC2} = 5V \pm 10\%$ , Temp =  $T_{MIN} \sim T_{MAX}$ , typical in  $V_{CC1} = V_{CC2} = +5V$ , Temp = 25°C.)

**RECEIVER SWITCHING CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation delay time, low-to-high-level output	$t_{PLH}$	<a href="#">Fig.6</a>	60	100	130	ns

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation delay time, low-to-high-level output	t <sub>PHL</sub>		45	70	105	ns
RXD signal rise time	t <sub>r</sub>			8		ns
RXD signal fall time	t <sub>f</sub>			8		ns

(V<sub>CC1</sub>=V<sub>CC2</sub>=5V±10%, Temp=T<sub>MIN</sub>~T<sub>MAX</sub>, typical in V<sub>CC1</sub>=V<sub>CC2</sub>=+5V, Temp=25°C.)

## DEVICE SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Loop delay 1, driver input to receiver output, Recessive to Dominant	t <sub>d</sub> (LOOP1)	<a href="#">Fig.9</a>	112		210	ns
Loop delay 2, driver input to receiver output, Dominant to Recessive	t <sub>d</sub> (LOOP2)		112		210	ns

(V<sub>CC1</sub>=V<sub>CC2</sub>=5V±10%, Temp=T<sub>MIN</sub>~T<sub>MAX</sub>, typical in V<sub>CC1</sub>=V<sub>CC2</sub>=+5V, Temp=25°C.)

## LOGIC SIDE ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
High level input voltage	V <sub>IH</sub>	TXD pin	2			V
Low level input voltage	V <sub>IL</sub>	TXD pin			0.8	V
High level input current	I <sub>IH</sub>	TXD pin			10	μA
Low level input current	I <sub>IL</sub>	TXD pin	-10			μA
Output Voltage High	V <sub>OH</sub>	I <sub>OH</sub> =-4mA, RXD pin	VDD1-0.4			V
Output Voltage Low	V <sub>OL</sub>	I <sub>OL</sub> =4mA, RXD pin			0.4	V
Input Capacitance	C <sub>IN</sub>	TXD pin		2		pF

**OVER TEMPERATURE PROTECTION**

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Shutdown junction temperature	$T_{j(sd)}$			160		°C

**SUPPLY CURRENT**

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
$V_{CC1}$ Supply current	$I_{CC1}$	$V_I=0V$ or $V_{CC1}$ , $V_{CC1}=3.3V$		1.8	2.8	mA
		$V_I=0V$ or $V_{CC1}$ , $V_{CC1}=5V$		2.3	3.6	mA
$V_{CC2}$ Supply current	$I_{CC2}$	$V_I=0V$ LOAD=60Ω		50	70	mA
		$V_I=V_{CC}$		6	10	mA

( $V_{CC1}=V_{CC2}=5V\pm 10\%$ , Temp= $T_{MIN}\sim T_{MAX}$ , typical in  $V_{CC1}=V_{CC2}=+5V$ , Temp=25°C.)

**FUNCTION TABLE**
**Table1.CAN TRANSCEIVER TRUTH TABLE**

DRIVER			RECEIVER			
INPUTS	OUTPUTS		BUS STATE	CANH- CANL	RXD	BUS STATE
TXD	CANH	CANL				
L	H	L	Dominate	$V_{ID}\geq 0.9V$	L	Dominate
H	Z	Z	Recessive	$0.5V < V_{ID} < 0.9V$	?	?
Open	Z	Z	Recessive	$V_{ID}\leq 0.5V$	H	Recessive
X	Z	Z	Recessive	Open	H	Recessive

(1) H=high level; L=low level; X=irrelevant.

**Table 2. DRIVER FUNCTION TABLE**

INPUTS	OUTPUTS		Bus State
TXD <sup>(1)</sup>	CANH <sup>(1)</sup>	CANL <sup>(1)</sup>	
L	H	L	Dominate
H	Z	Z	Recessive

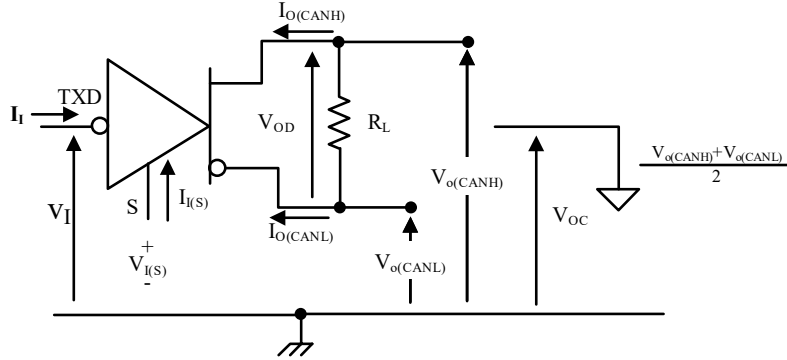
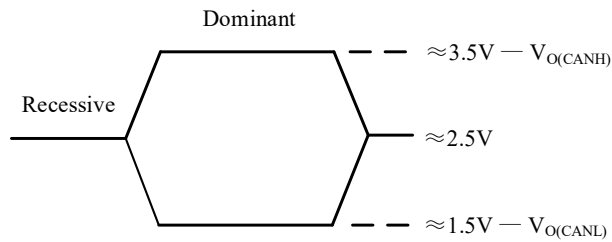
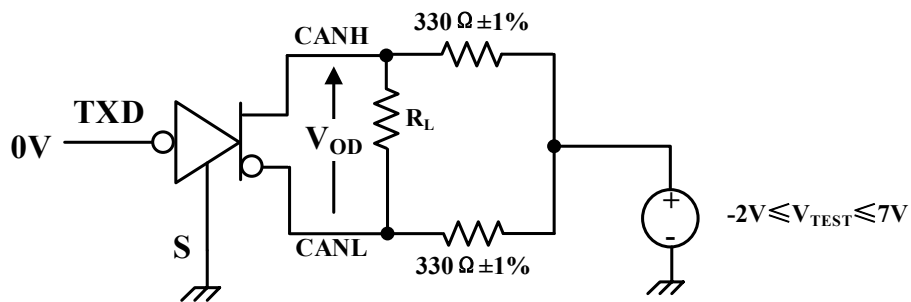
(1) H=high level; L=low level; X=irrelevant; Z=high impedance.

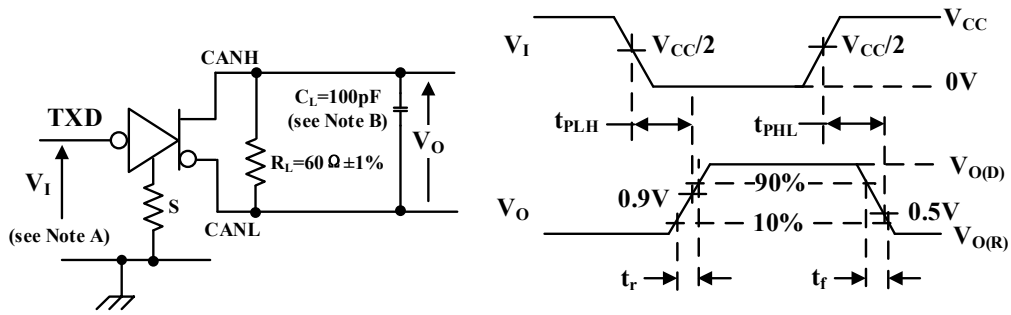


Table 3. RECEIVER FUNCTION TABLE

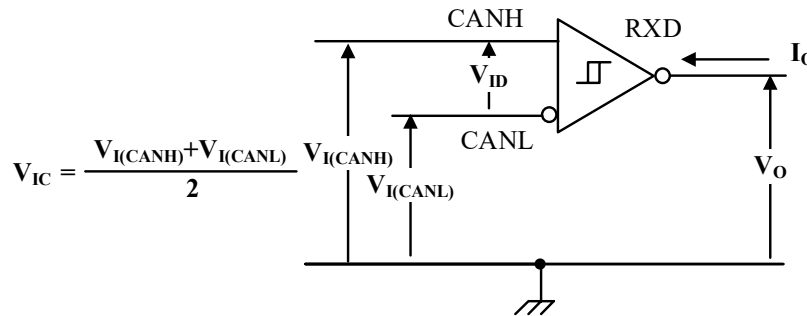
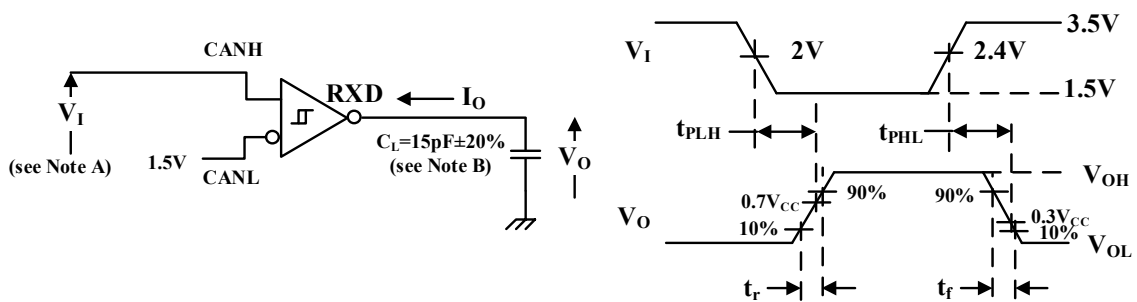
$V_{ID}=\text{CANH}-\text{CANL}$	$V_{ID}=\text{CANH}-\text{CANL}$	Bus State	Bus State
Normal or Silent	$V_{ID} \geq 0.9V$	Dominate	Dominate
	$0.5 < V_{ID} < 0.9V$	?	?
	$V_{ID} \leq 0.5V$	Recessive	Recessive
	Open ( $V_{ID} \approx 0V$ )	OPEN	Recessive

(1) H=high-level; L=low-level; ?=uncertain.

**TEST CIRCUIT**

**Fig.1 Driver Voltage, Current, and Test Definition**

**Fig.2 Bus Logic State Voltage Definition**

**Fig.3 Driver  $V_{OD}$  Test Circuit**

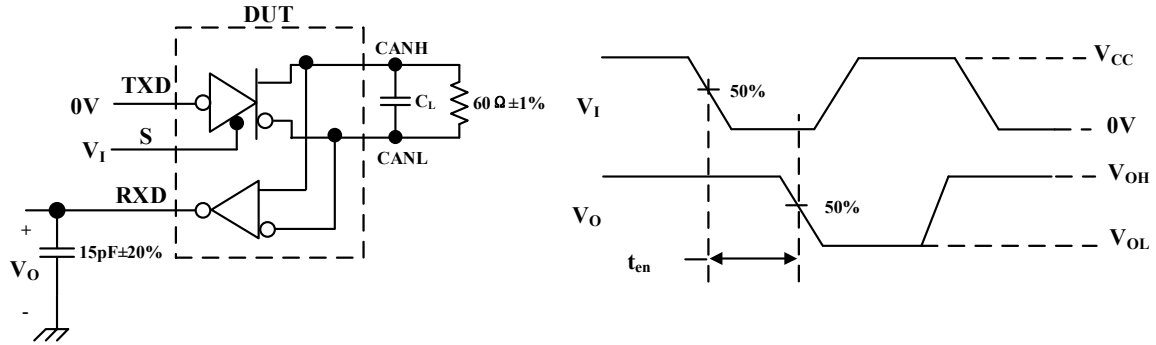


- A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 125$  kHz, 50% duty,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes instrumentation and fixture capacitance within  $\pm 20\%$

**Fig.4 Driver Test Circuit and Waveform**

**Fig.5 Receiver Voltage and Current Definition**


- A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 125$  kHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes instrumentation and fixture capacitance within  $\pm 20\%$ .

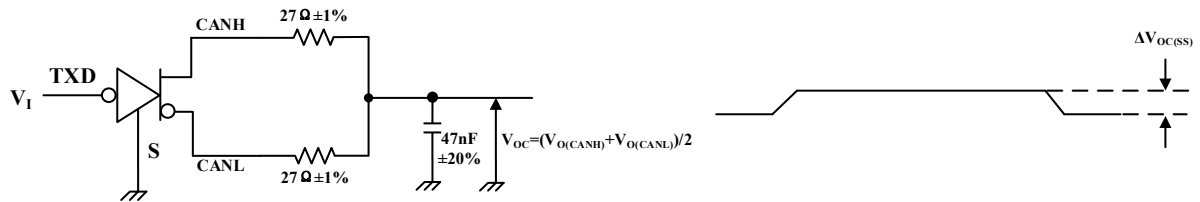
**Fig.6 Receiver Test Circuit and Waveform**



NOTE:  $C_L=100\text{pF}$  includes instrumentation and fixture capacitance with  $\pm 20\%$ ;

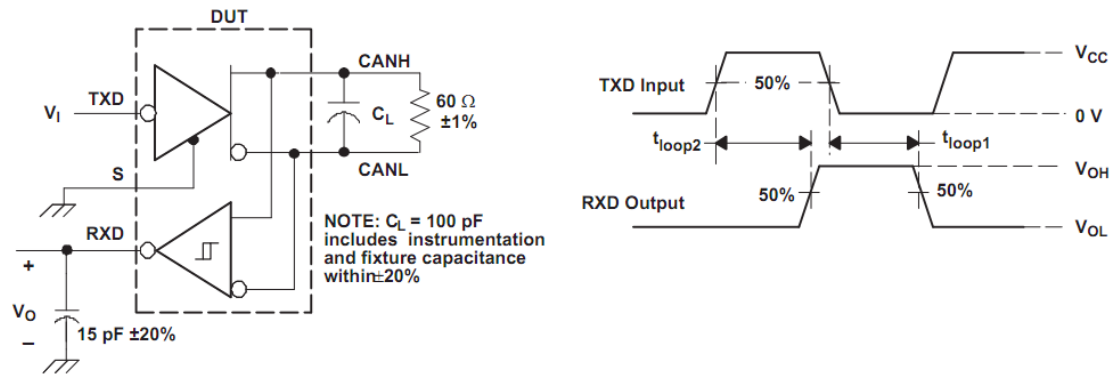
All  $V_L$  input pulses are supplied by a generator having the following characteristics:  $t_r \leq 6\text{ ns}$ ,  $t_f \leq 6\text{ ns}$ , Pulse Repetition Rate (PRR)=25kHz, 50% duty cycle.

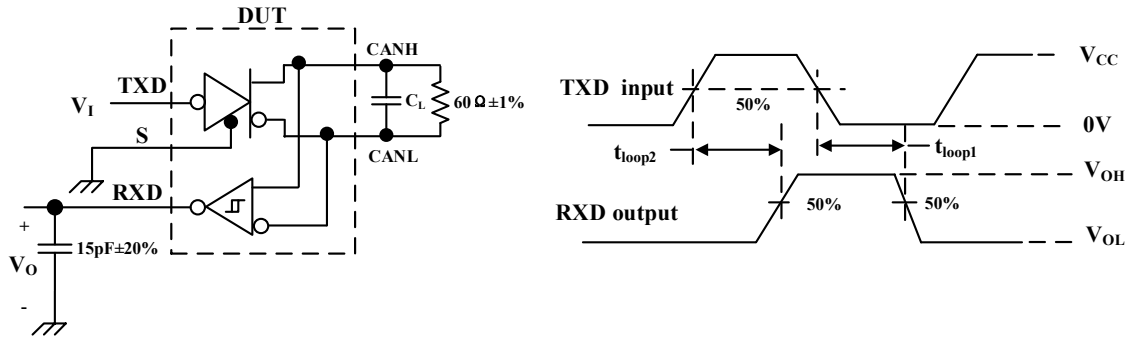
**Fig.7  $t_{EN}$  Test Circuit and Waveform**



A. All  $V_L$  input pulses are from 0 V to  $V_{CC}$  and supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 6\text{ ns}$ . Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

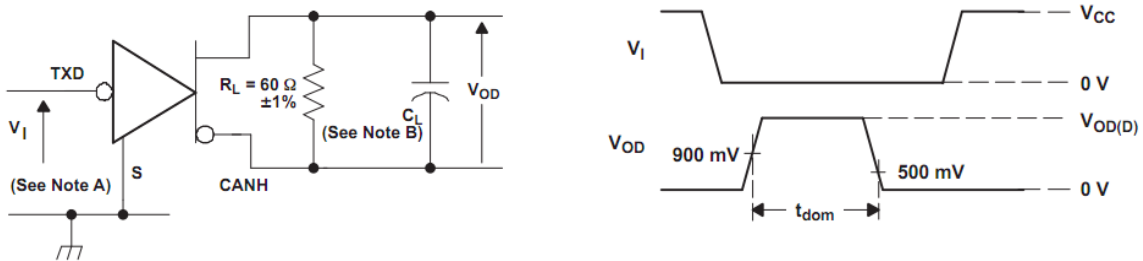
**Fig.8 Peak-to-Peak Common Mode Output Voltage Test and Waveform**





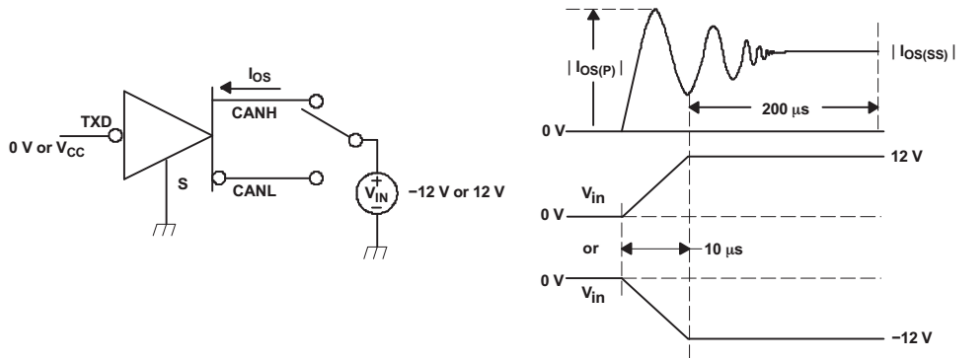
NOTE:  $C_L=100\text{pF}$  includes instrumentation and fixture capacitance within  $\pm 20\%$ .

**Fig.9  $t_{(LOOP)}$  Test Circuit and Waveform**

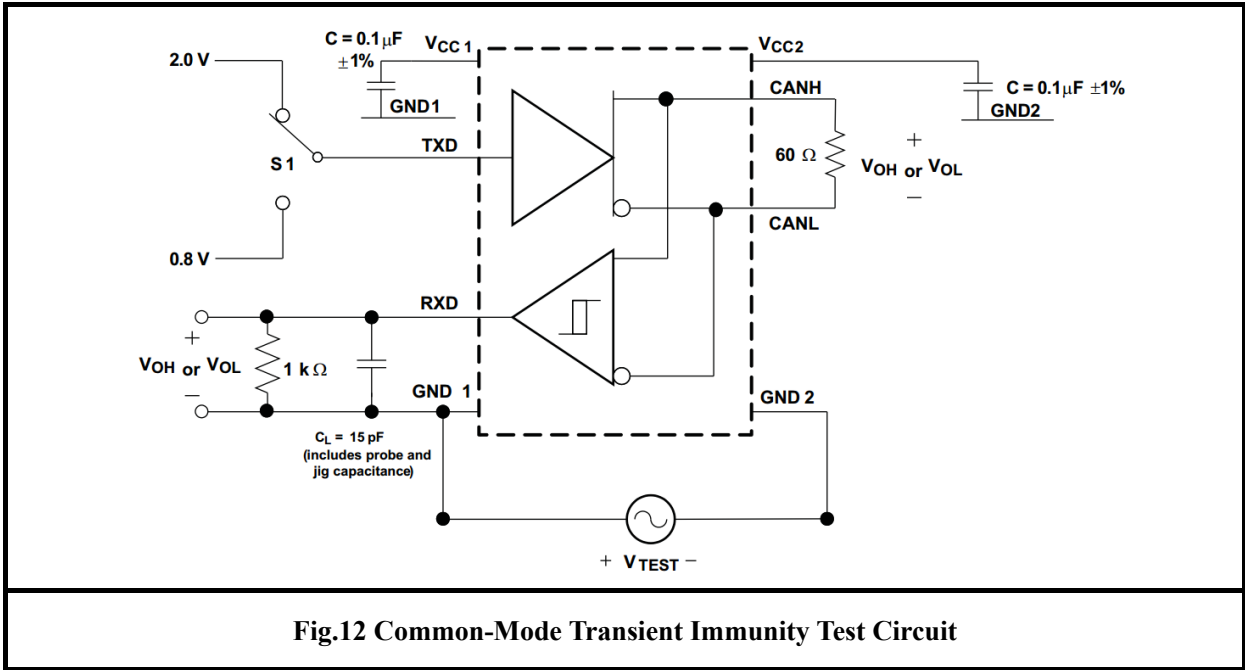


- A. The input pulse is supplied by a generator having the following characteristics:  $t_r \leq 6\text{ ns}$ ,  $t_f \leq 6\text{ ns}$ ,  $Z_O = 50\ \Omega$ ;
- B.  $C_L$  includes instrumentation and fixture capacitance with  $\pm 20\%$

**Fig.10 Dominant Time-Out Test Circuit and Waveform**



**Fig.11 Driver Short-Circuit Current Test Circuit and Waveform**



**Fig.12 Common-Mode Transient Immunity Test Circuit**

**ADDITIONAL DESCRIPTION****1 Sketch**

SIT1050ISO is an interface chip with isolation function for CAN protocol controller and physical bus, and can be applied to the fields of in-vehicle, industrial control etc. It is primarily intended for high-speed applications, up to 1 MBaud, in passenger cars. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller, and fully compatible with the ISO 11898 standard.

Provide wide body SOPW16 package, isolation withstand voltage  $5000V_{RMS}$ .

Provide wide-body DUB8 package, isolation withstand voltage  $2500V_{RMS}$ , Common-Mode Transients up to  $100kV/\mu s$ .

**2 Current protection**

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

**3 Over temperature protection**

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature  $T_{j(sd)}$ , the output drivers will be disabled until the virtual junction temperature becomes lower than  $T_{j(sd)}$  and TXD becomes recessive again. By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

**4 TXD dominant time-out function**

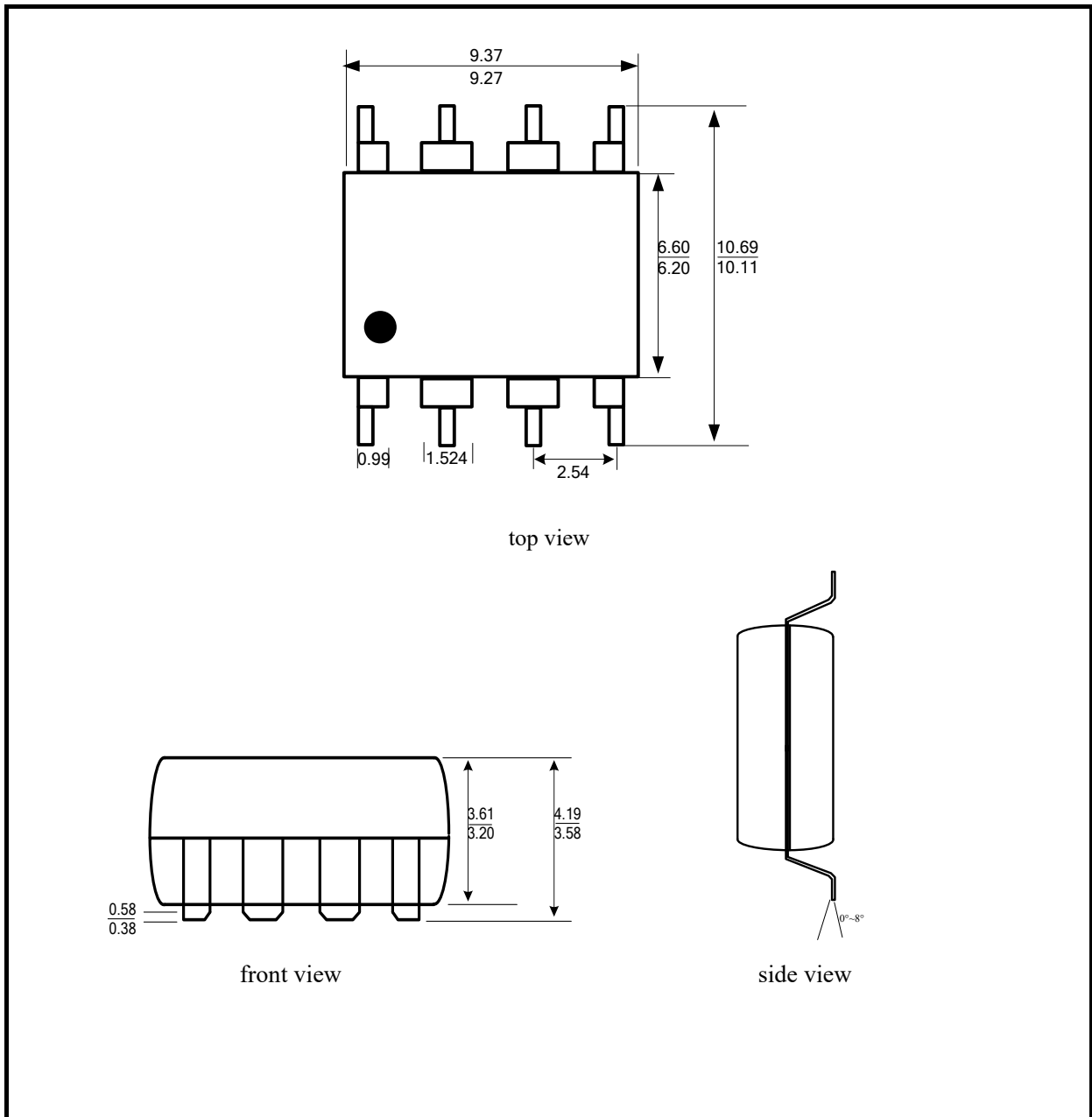
A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value ( $t_{dom}$ ), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.

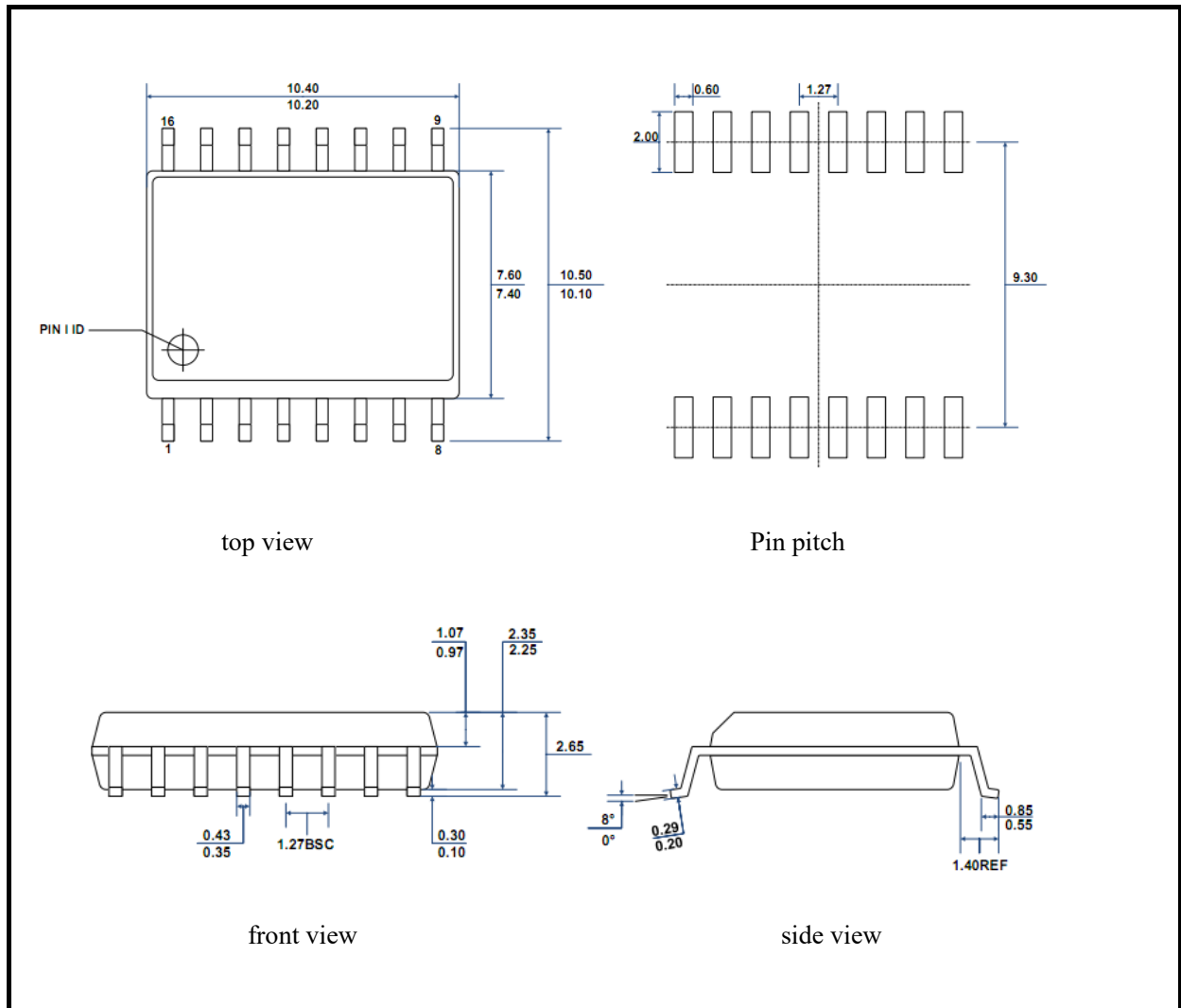
**5 Operating mode**

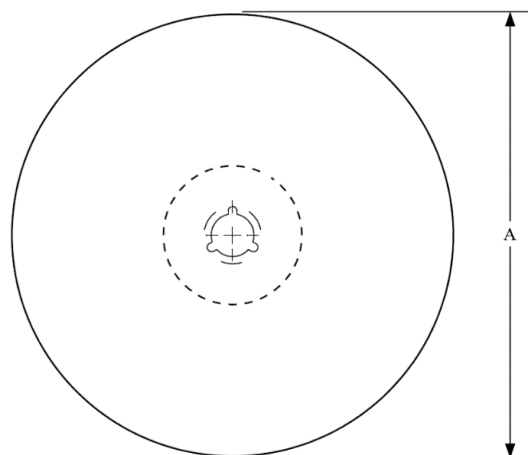
SIT1050ISO works in high-speed mode, which is the default working mode.

DUB8 DIMENSIONS

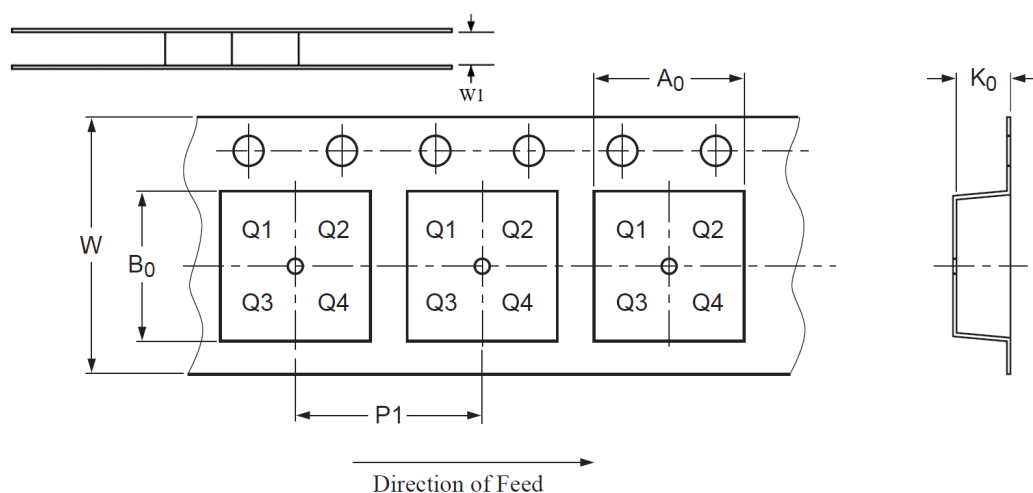




**SOPW16 DIMENSIONS**


**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



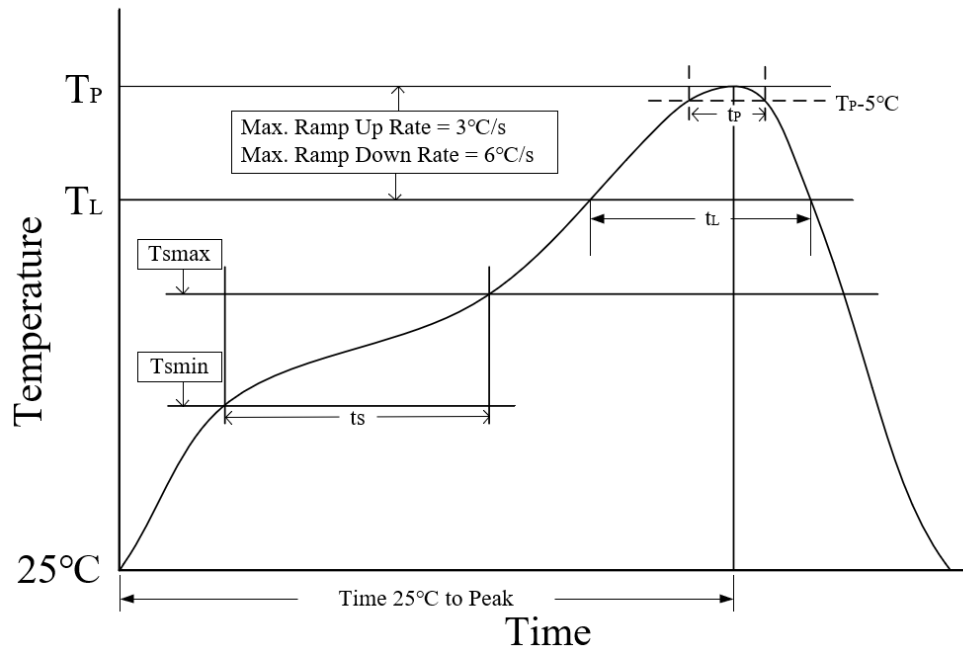
PIN1 is in quadrant 1

Package Type	Reel Diameter A (mm)	Tape width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
DUB8	330±2.0	24.4 <sup>+2.0</sup> <sub>-0.0</sub>	11.00±0.10	9.60±0.10	4.40±0.10	16.00	24.00 <sup>+0.3</sup> <sub>-0.1</sub>
SOPW16	330±2.0	16.4 <sup>+2.0</sup> <sub>-0.0</sub>	10.75±0.10	10.70±0.10	2.80±0.10	12.00±0.10	16.00±0.20

**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE	PACKING
SIT1050ISODUB8	DUB8	Tape and reel
SIT1050ISODW	SOPW16	Tape and reel

DUB8 is packed with 800 pieces/disc in braided packaging. SOPW16 is packed with 1000 pieces/disc in braided packaging.

**REFLOW SOLDERING**


Parameter	Lead-free soldering conditions
Ave ramp up rate ( $T_L$ to $T_P$ )	3°C/second max
Preheat time $t_s$ ( $T_{smin}=150^\circ C$ to $T_{smax}=200^\circ C$ )	60-120 seconds
Melting time $t_L$ ( $T_L=217^\circ C$ )	60-150 seconds
Peak temp $T_P$	260-265°C
5°C below peak temperature $t_p$	30 seconds
Ave cooling rate ( $T_P$ to $T_L$ )	6°C/second max
Normal temperature 25°C to peak temperature $T_P$ time	8 minutes max

**Important statement**

SIT reserves the right to change the above-mentioned information without prior notice.

**VERSION HISTORY**

Version number	Data sheet status	Revision date
V1.0	Initial version.	March 2022
V1.1	Adjusted the format.	November 2020
V1.2	Updated the maximum value of low loop delay; Updated DUB8 schematic.	February 2021
V1.3	Added $V_{IH}$ , $V_{IL}$ , $I_{OH}$ and $I_{OL}$ ; Added “logical side electrical characteristics”; Deleted the information of SOPW8; Added “tape and reel information”; Updated ordering information; Added “reflow soldering”; Added “important statement”; Added “revision history”.	December 2022