FEATURES

- Compliant with LIN 2.x, ISO 17987-4:2016 (12V) and SAE J2602
- AEC-Q100 qualified
- 5V/3.3V voltage regulator output with high voltage LDO
- Integrated over-temperature protection function (thermal shutdown)
- Integrated dominant timeout function
- Bus current limiting protection
- 5V/3.3V voltage regulator and current limiting protection
- Voltage regulator output undervoltage detection
- Very low power consumption sleep mode
- Support remote wake-up
- LIN data transmission rate up to 20kbps
- Available in SOP8 and DFN3*3-8 packages

PRODUCT APPEARANCE

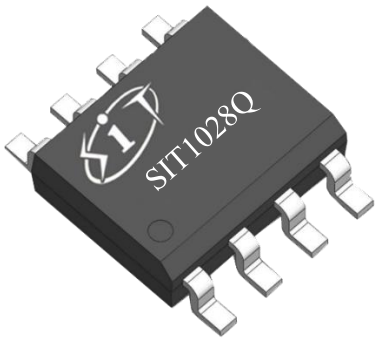


Fig. 1 Provide environmentally friendly lead-free package

DESCRIPTION

The SIT1028Q is a Local Interconnect Network (LIN) physical layer transceiver with internal integrated high voltage LDO. It can provide stable 5V/3.3V power supply for external ECU (Electronic Control Unit) microcontroller or related peripherals. The LIN transceiver is compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016(12V) and SAE J2602 standards. It is mainly suitable for in-vehicle networks with a transmission rate of 1kbps to 20kbps. The LIN bus output pin of the SIT1028Q has an internal pull-up resistor with a bus output waveform shaping function to reduce electromagnetic radiation (EME). TXD pin is used as the input end to send the low-voltage signal of the microcontroller to LIN bus. Meanwhile, LIN pin receives the data stream on the bus, and the data is transmitted back to the microcontroller or to other microcontrollers by RXD output pin of the receiver.

The SIT1028Q can operate in the range of 5.5V~28V and supports 12V application. The SIT1028Q features extremely low current consumption in sleep mode, quickly minimizes power consumption in the event of failure, and can be remotely woken up via the LIN bus or placed in normal operating mode via a signal on the EN pin. SIT1028Q provides a 5V/3.3V voltage regulator power on and power off detection output pin RSTN to facilitate the microcontroller to monitor the power supply of the regulator.

PIN CONFIGURATION

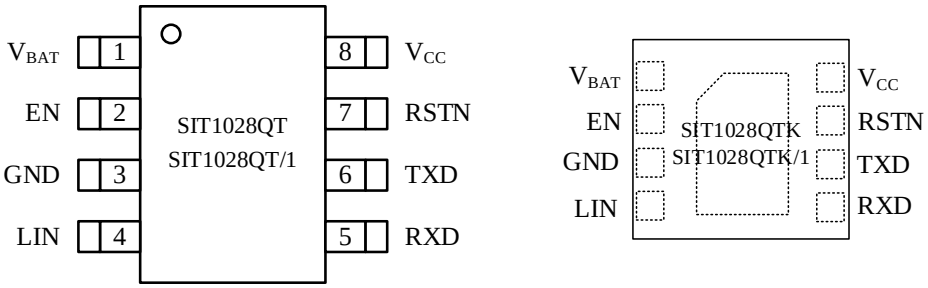


Fig. 2 SIT1028Q pin configuration diagrams

PIN DESCRIPTION

Table 1. SIT1028Q pin description

Pin	Symbol	Description
1	V_{BAT}	battery supply voltage
2	EN	enable input
3	GND	ground
4	LIN	LIN bus line input/output
5	RXD	receive data output; active LOW after a wake-up event
6	TXD	transmit data input
7	RSTN	voltage regulator reset signal output
8	V_{CC}	voltage regulator output

NOTE: In the DFN3*3-8 package, the pad on the back is connected to the GND pin of the chip. In order to obtain better heat dissipation performance, the pad on the back can be connected to a suitable "ground" on the PCB board.

LIMITING VALUES

Parameter	Symbol	Conditions	Value	Unit
battery supply voltage	V_{BAT}	with respect to GND	-0.3 ~ +40	V
voltage on pins	V_{CC}	with respect to GND	-0.3 ~ +7	V
	V_{RXD}	with respect to GND	-0.3 ~ V_{CC}+0.3	V
	V_{EN}	with respect to GND	-0.3 ~ V_{CC}+0.3	V
	V_{RSTN}	with respect to GND	-0.3 ~ V_{CC}+0.3	V
	V_{TXD}	with respect to GND	-0.3 ~ V_{CC}+0.3	V
	V_{LIN}	with respect to GND and V_{BAT}	-40 ~ +40	V
virtual junction temperature	T_j		-40 ~ 150	°C
ambient temperature	T_{amb}		-40 ~ 125	°C
storage temperature	T_{stg}		-55 ~ 150	°C

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

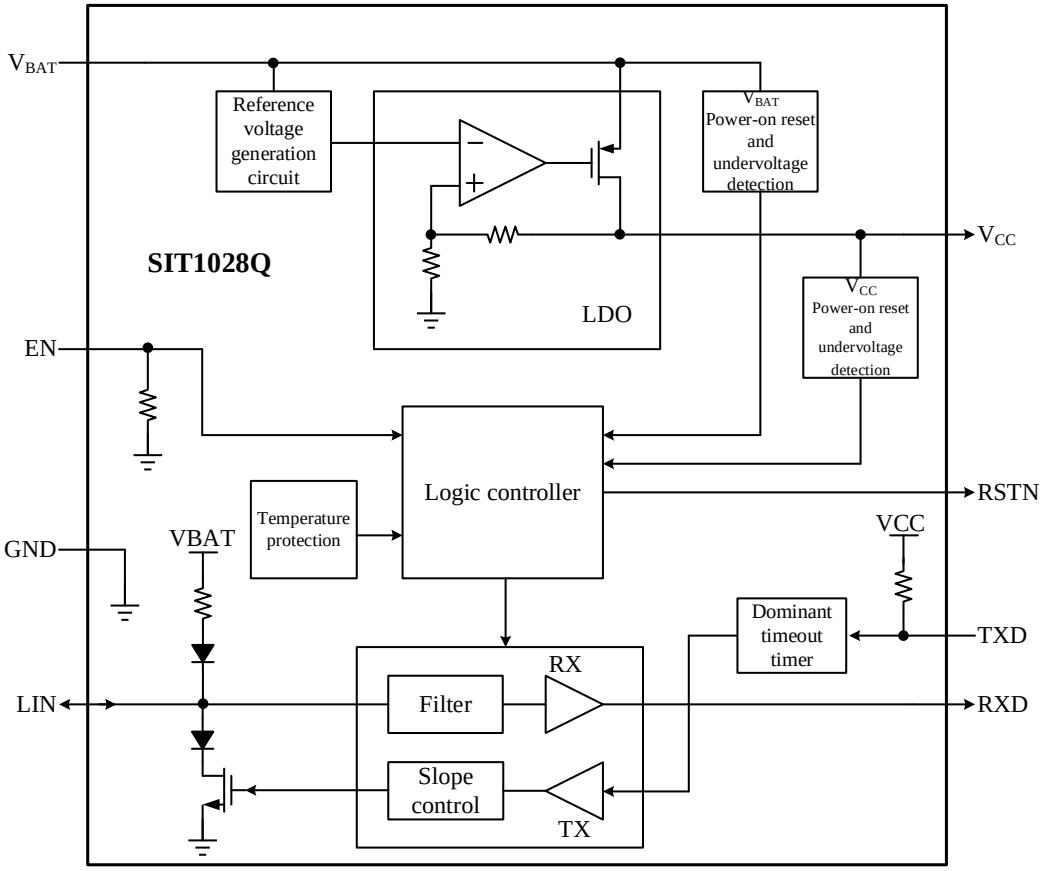


Fig. 3 SIT1028Q Block diagram

FEATURE DESCRIPTION

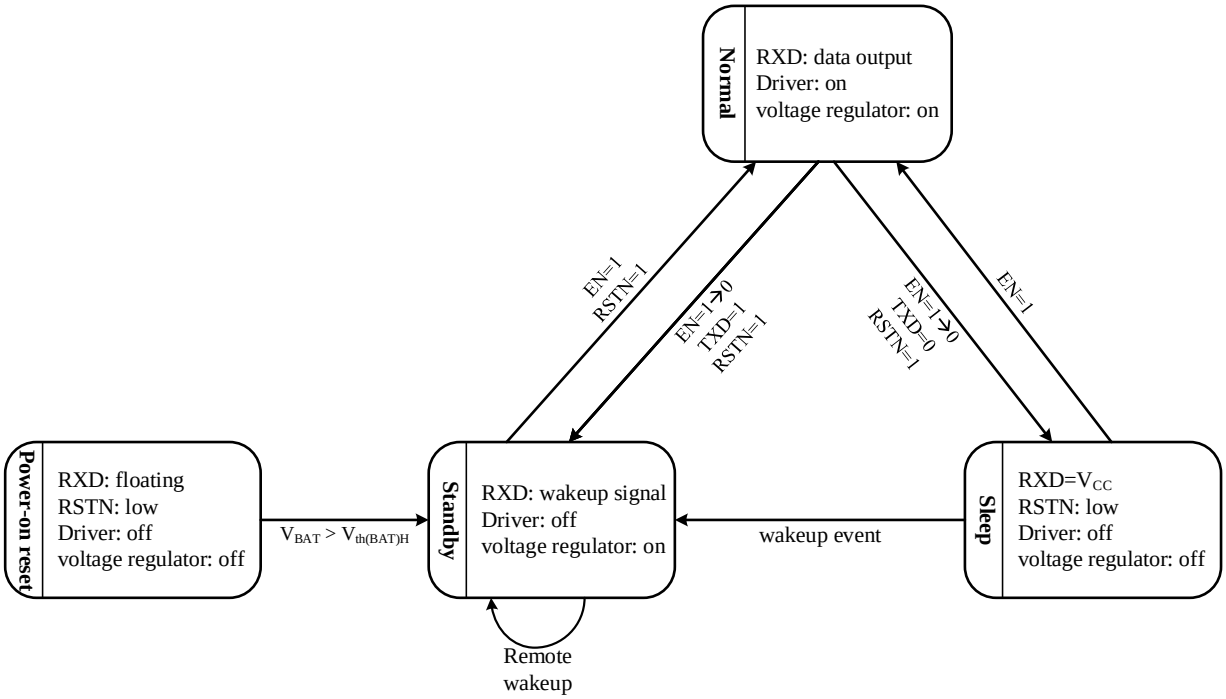


Fig. 4 State diagram

1 Overview

The SIT1028Q is an internally integrated high-voltage LDO chip that can be applied to the interface between the LIN protocol controller and the physical bus. It can be applied to the fields of in-vehicle and industrial control, and the transmission rate is up to 20kbps. The SIT1028Q receives the transmit data stream from the protocol controller at the TXD terminal and converts it into the bus signal with the best voltage swing rate and waveform shaping; The input data on the LIN bus is output from the RXD port of the receiver to the external microcontroller. This device is compatible with the "LIN 2.x/ISO 17987-4:2016 (12V)/SAE J2602" standard.

2 Operating modes

As shown in Fig 4, the SIT1028Q supports four operating modes for Power-on mode, Standby mode, Normal mode and Sleep mode.

2.1 Power-on mode

If the voltage on V_{BAT} is less than the power-on detection threshold $V_{th(det)off}$ or an overtemperature event occurs, the SIT1028Q will be in Power-on mode and both the voltage regulator and LIN transceiver will be off, RSTN = 0.

2.2 Standby mode

The SIT1028Q can switch to Standby mode via other three operating modes and the voltage regulator remains on. LIN transceiver is off and bus remote wake up function is enable (RXD = 0 as wake up flag).

When V_{BAT} voltage is greater than the power on detection threshold $V_{th(det)pon}$ and no over temperature event, SIT1028Q will automatically switch from Power-on mode to Standby mode.

When SIT1028Q is in normal mode, during the mode selection window, if EN = 0, TXD = 1 and RSTN = 1, SIT1028Q will switch from Normal mode to Standby mode (as shown in Fig. 5).

When SIT1028Q is in sleep mode, it can switch to standby mode through the bus remote wake-up, the remote wake up behavior as shown in Fig. 6.

2.3 Normal mode

After the SIT1028Q is powered on and started normally, SIT1028Q enters Standby mode firstly. When the EN is raised at RSTN = 1, SIT1028Q switches from Standby mode to Normal mode. If SIT1028Q is in Sleep mode, it can switch to Normal mode after raising the EN.

In normal mode, SIT1028Q can normally send and receive data through LIN bus with the voltage regulator and LIN transceiver on. At this time, the microcontroller can send data to LIN bus through TXD input pins to convert low level logic level signals into high level V_{BAT} (battery) level signals (high level represents recessive, low level represents dominant), and perform bus waveform shaping to inhibit electromagnetic emission (EME). At the same time, the signal on the bus can be received by the pin LIN and output to the pin RXD via the SIT1028Q receiver, which can be converted into low level logic level data for processing by the external microcontroller.

2.4 Sleep mode

It is the mode with the lowest power consumption of SIT1028Q. In this case, both the voltage regulator and LIN transceiver are shut down, and RSTN is forced to pull down, which can be remotely awakened through LIN bus.

As shown in Fig. 4, only Normal mode can switch to Sleep mode. During the mode selection window, if EN = 0, TXD = 0 and RSTN = 1, SIT1028Q will switch from Normal mode to Sleep mode (as shown in Fig 5).

2.5 Switch from Normal to Sleep/Standby mode

As shown in Fig 5, SIT1028Q first blocks the transmission path from TXD to LIN after EN is pulled down, and then enters the mode selection window after waiting for $t_{msel(min)}$. At this time, if TXD = 1, it enters the Standby mode, and if TXD = 0, it enters the Sleep mode. The total mode selection time after EN is pulled down is $t_{msel(max)}$.

3 Internal integrated voltage regulator V_{CC}

The SIT1028Q is powered by a single power supply. With the pin V_{BAT} as the input, the internal integrated high voltage LDO (input voltage withstand 40V) provides stable 5V/3.3V to the external microcontroller and related peripherals through the pin V_{CC}, and the output current can reach 70mA, SIT1028Q/1 can reach 150

mA room temperature (25°C). The undervoltage of V_{CC} can be reflected by the output signal of RSTN. When the V_{CC} is lower than the undervoltage detection threshold V_{UVD}, the RSTN output is low.

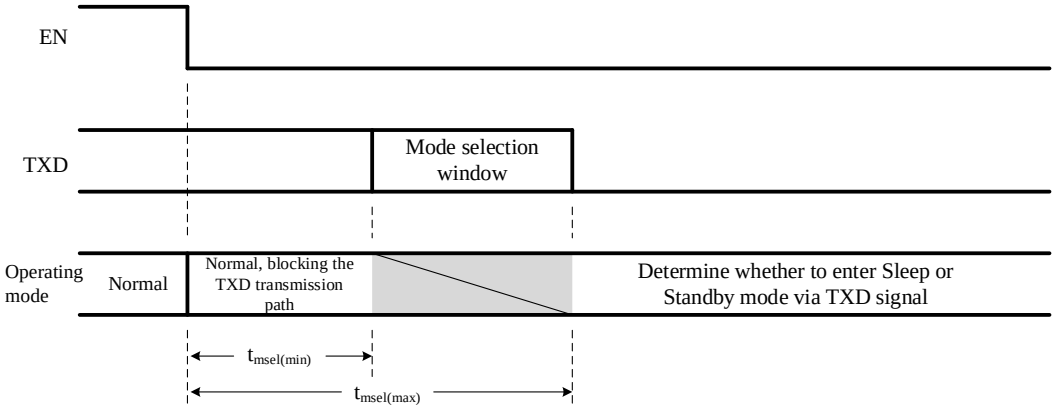


Fig. 5 Timing waveform of switching Normal to Standby/Sleep

4 Remote wake-up

Remote wake up on the LIN pin: When the LIN pin is pulled down to the low level through a falling edge, a rising edge appears at the next time, and the low-level maintenance time between the rising edge and the previous falling edge is greater than $t_{wake(busdom)min}$, then the process is regarded as an effective remote wake up (as shown in Fig 6). RXD is set to a low level to indicate the wake-up flag after a remote wake up occurs.

5 Dominant time-out function

If the TXD pin due to hardware and/or software application failure is forced to permanent low level, the integrated TXD dominant timeout timer circuit can prevent the bus line are driven to permanent dominant status (blocking all network communication). The timer is triggered by the falling edge on the pin TXD. If the low level on the pin TXD maintain time longer than the internal timer ($t_{to\ (dom)\ TXD}$), the transmitter will be disabled, to drive the bus into the recessive state. The timer is reset by the rising edge on the pin TXD.

6 Overtemperature protection function

If an overtemperature event occurs when the SIT1028Q is in normal or standby mode, it will be switched to Power-on mode, and the voltage regulator and LIN transceiver module will be shut down. When the temperature drops below the overtemperature protection recovery threshold, the SIT1028Q switches from the Power-on mode to the standby mode.

7 Fail-safe feature

- A pull-up to V_{CC} on pin TXD ensures that when the pin TXD is virtual welded or the microcontroller pin is floating, it remains bus recessive level.
- The current in the transmitter output stage is limited in order to protect the transmitter against burning driver or affecting function when bus short circuits to pins V_{BAT}.

- A loss of power has no impact on the bus port and there is no reverse current on it.
- When EN or RSTN is low, the LIN driver will shut down automatically.
- After switching to normal mode, the LIN driver is enabled only if high level is detected in TXD.

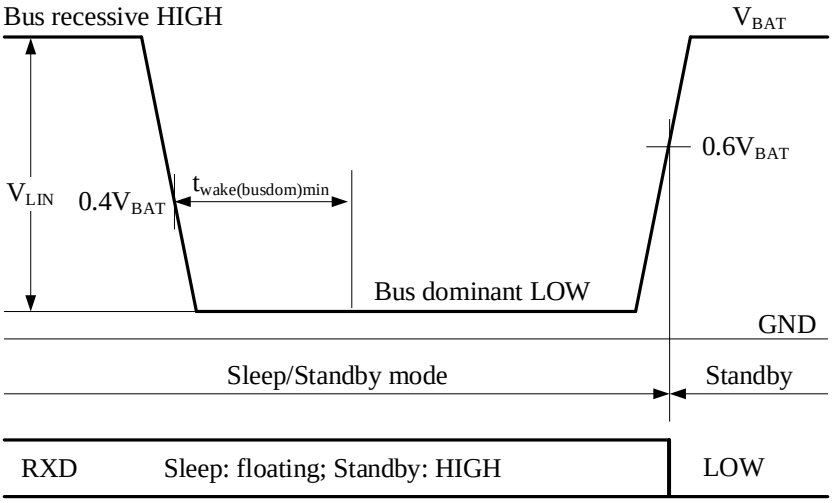


Fig. 6 Remote wake-up behavior

STATIC CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power consumption						
Battery supply current	I_{BAT}	Sleep mode ($V_{LIN} = V_{BAT}$)	-	10	-	μA
		Sleep mode ($V_{LIN} = V_{BAT}$) Only SIT1028QT/1 and SIT1028QTK/1 version		8	-	μA
		Standby mode ($V_{LIN} = V_{BAT}$)	-	40	-	μA
		Standby mode ($V_{LIN} = V_{BAT}$) Only SIT1028QT/1 and SIT1028QTK/1 version		25	-	μA
		Normal mode (recessive) ($V_{LIN} = V_{BAT}$; $V_{TXD} = V_{CC}$; V_{RSTN} = HIGH)	-	200	500	μA
		Normal mode (dominant) (V_{BAT} = 12V; V_{TXD} = 0V; V_{RSTN} = HIGH)	-	2.5	4	mA
		Normal mode (dominant) (V_{BAT} = 12V; V_{TXD} = 0V; V_{RSTN} = HIGH) Only SIT1028QT/1 and SIT1028QTK/1 version		2	3.5	mA
Power-on reset						
V_{BAT} reset threshold voltage	$V_{th(BAT)L}$		3	-	4.7	V
		Only SIT1028QT/1 and SIT1028QTK/1 version	3	3.8	4.2	V
V_{BAT} reset threshold voltage	$V_{th(BAT)H}$		-	-	5.25	V
		Only SIT1028QT/1 and SIT1028QTK/1 version		4.1	4.5	V
V_{BAT} hysteresis voltage	$V_{hys(BAT)}$		50	-	-	mV
Pin V_{CC}						
Voltage regulator output voltage	V_{CC}	$V_{CC(nom)}$ = 5V; I_{CC} = -70mA ~ 0	4.9	5	5.1	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
		$V_{CC(nom)}$ = 5V; I_{CC} = -150mA ~ 0 Only SIT1028QT/1 and SIT1028QTK/1 version	4.9	5	5.1	V
		$V_{CC(nom)}$ = 3.3V; I_{CC} = -70mA ~ 0	3.234	3.3	3.366	V
		$V_{CC(nom)}$ = 3.3V; I_{CC} = -70mA ~ 0 Only SIT1028QT/1 and SIT1028QTK/1 version	3.234	3.3	3.366	V
Current limitation for voltage regulator	I_{Olim}	V_{CC} = 0 ~ 5.5V	-250	-	-70	mA
		V_{CC} = 0 ~ 5.5V Only SIT1028QT/1 and SIT1028QTK/1 version	-500		-150	mA
Undervoltage detection voltage	V_{UVD}	$V_{CC(nom)}$ = 5V	4	-	4.7	V
		$V_{CC(nom)}$ = 5V Only SIT1028QT/1 and SIT1028QTK/1 version	4.2		4.75	V
		$V_{CC(nom)}$ = 3.3V	2.3	-	2.9	V
		$V_{CC(nom)}$ = 3.3V Only SIT1028QT/1 and SIT1028QTK/1 version	2.75		3.135	V
Undervoltage Recover voltage	V_{UVR}	$V_{CC(nom)}$ = 5V	4.2	-	4.9	V
		$V_{CC(nom)}$ = 5V Only SIT1028QT/1 and SIT1028QTK/1 version	4.35		4.9	V
		$V_{CC(nom)}$ = 3.3V	2.6	-	3.2	V
		$V_{CC(nom)}$ = 3.3V Only SIT1028QT/1 and SIT1028QTK/1 version	2.85		3.24	V
V_{BAT} to V_{CC} conduction resistance	$R_{(VBAT-VCC)}$ [1]	$V_{CC(nom)}$ = 5 V; V_{BAT} = 4.5V ~ 5.5V I_{V1} = -70 mA ~ -5mA	-	-	5	Ω
		$V_{CC(nom)}$ = 5 V; V_{BAT} = 4.5V ~ 5.5V I_{V1} = -1500 mA ~ -5Ma Only SIT1028QT/1 and SIT1028QTK/1 version			9	Ω
Output capacitance	C_O [1]	ESR < 5Ω	2.2	10	-	μF

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Pin TXD						
Input threshold voltage	$V_{th(SW)}$	V_{CC} = 2.97 V ~ 5.5 V	0.3 V_{CC}	-	0.7 V_{CC}	V
Input hysteresis voltage	$V_{hys(i)}$	V_{CC} = 2.97 V ~ 5.5 V	200	-	-	mV
Pull-up resistance	R_{pu}		5	12	25	kΩ
Pin RXD						
HIGH-level input voltage	I_{OH}	Normal mode V_{LIN} = V_{BAT}; V_{RXD} = V_{CC} - 0.4 V	-	-	-0.4	mA
LOW-level input voltage	I_{OL}	Normal mode V_{LIN} = 0; V_{RXD} = 0.4 V	0.4	-	-	mA
Pin EN						
Input threshold voltage	$V_{th(SW)}$		0.8	-	2	V
Pull-down resistance	R_{pd}		50	130	400	kΩ
Pin RSTN						
Pull-up resistance	R_{pu}	V_{RSTN} = V_{CC} - 0.4 V V_{CC} = 2.97 V ~ 5.5 V	3	-	12	kΩ
LOW-level output current	I_{OL}	V_{RSTN} = 0.4 V V_{CC} = 2.97 V ~ 5.5 V -40 °C < T_j < 195 °C	3.2	-	40	mA
LOW-level output voltage	V_{OL}	V_{CC} = 2.5 V ~ 5.5 V -40 °C < T_j < 195 °C	0	-	0.5	V
HIGH-level output voltage	V_{OH}	-40 °C < T_j < 195 °C	0.8 V_{CC}	-	V_{CC} + 0.3	V
Pin LIN						
Current limitation for driver dominant state	I_{BUS_LIM}	V_{TXD} = 0V; V_{LIN} = V_{BAT} = 18V	40	-	100	mA
Receiver recessive input leakage current	$I_{BUS\_PAS\_rec}$	V_{TXD} = V_{CC}; V_{LIN} = 18V; V_{BAT} = 5.5V	-	-	20	µA
Receiver dominant input leakage current	$I_{BUS\_PAS\_dom}$	Normal mode V_{TXD} = V_{CC}; V_{LIN} = 0V; V_{BAT} = 12V	-1000	-	-	µA
Loss-of-ground bus leakage current	$I_{L(log)}$	V_{BAT} = 18V; V_{LIN} = 0V	-1000	-	10	µA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Loss-of-power bus leakage current	$I_{L(lob)}$	V_{BAT} = 0V; V_{LIN} = 18V	-	-	20	μA
Receiver dominant reverse threshold voltage	$V_{th(dom)RX}$	V_{BAT} = 5.5 V ~ 18 V	-	-	0.4V_{BAT}	V
Receiver recessive reverse threshold voltage	$V_{th(rec)RX}$	V_{BAT} = 5.5 V ~ 18 V	0.6V_{BAT}	-	-	V
Receiver center reverse threshold voltage	$V_{th(RX)cntr}$	V_{BAT} = 5.5 V ~ 18 V $V_{th(RX)\ cntr}$ = ($V_{th(rec)RX}$+$V_{th(dom)RX}$)/2	0.475V_{BAT}	0.5 V_{BAT}	0.525V_{BAT}	V
Receiver hysteresis threshold voltage	$V_{th(hys)RX}$	V_{BAT} = 5.5 V ~ 18 V $V_{th(hys)RX}$ = $V_{th(rec)RX}$-$V_{th(dom)RX}$	-	-	0.175V_{BAT}	V
Slave resistance	R_{slave}	equivalent resistance between pins LIN and VBAT; V_{LIN} = 0V; V_{BAT} = 12V	20	30	60	kΩ
Capacitance on pin LIN	C_{LIN} [1]		-	-	30	pF
Dominant output voltage	$V_{o(dom)}$	Normal mode V_{TXD} = 0V; V_{BAT} = 7V	-	-	1.4	V
		Normal mode V_{TXD} = 0V; V_{BAT} = 18V	-	-	2.0	V
Overtemperature protection						
Overtemperature protection	$T_{th(act)otp}$ [1]		165	180	195	°C
Overtemperature recovery	$T_{th(rel)otp}$ [1]		125	140	155	°C

(Unless specified otherwise; 5.5V≤V_{BAT}≤18V, -40°C≤T_j≤150°C; typical in V_{BAT}=13V, T_{amb}=25°C.)

[1] Not tested in production; guaranteed by design.

SWITCH CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Duty cycles						
duty cycle 1	δ1 [1][2]	$V_{th(rec)(max)}$=0.744×V_{BAT}; $V_{th(dom)(max)}$=0.581×V_{BAT}; t_{bit}=50µs; V_{BAT}=7V~18V Fig. 7/9	0.396			
		$V_{th(rec)(max)}$=0.76×V_{BAT}; $V_{th(dom)(max)}$=0.593×V_{BAT}; t_{bit}=50µs; V_{BAT}=5.5V~7V Fig. 7/9	0.396			
duty cycle 1	δ2 [2][3]	$V_{th(rec)(min)}$=0.422×V_{BAT}; $V_{th(dom)(min)}$=0.284×V_{BAT}; t_{bit}=50µs; V_{BAT}=7.6V~18V Fig. 7/9			0.581	
		$V_{th(rec)(min)}$=0.41×V_{BAT}; $V_{th(dom)(min)}$=0.275×V_{BAT}; t_{bit}=50µs; V_{BAT}=6.1V~7.6V Fig. 7/9			0.581	
duty cycle 3	δ3 [1][2]	$V_{th(rec)(max)}$=0.778×V_{BAT}; $V_{th(dom)(max)}$=0.616×V_{BAT}; t_{bit}=96µs; V_{BAT}=7V~18V Fig. 7/9	0.417			
		$V_{th(rec)(max)}$=0.797×V_{BAT}; $V_{th(dom)(max)}$=0.630×V_{BAT}; t_{bit}=96µs; V_{BAT}=5.5V~7V Fig. 7/9	0.417			
duty cycle 4	δ4 [2][3]	$V_{th(rec)(min)}$=0.389×V_{BAT}; $V_{th(dom)(min)}$=0.251×V_{BAT}; t_{bit}=96µs; V_{BAT}=7.6V~18V Fig. 7/9			0.590	
		$V_{th(rec)(min)}$=0.378×V_{BAT}; $V_{th(dom)(min)}$=0.242×V_{BAT}; t_{bit}=96µs; V_{BAT}=6.1V~7.6V Fig. 7/9			0.590	
Timing characteristics						
receiver propagation delay	$t_{PD(RX)}$	C_{RXD} = 20 pF			6	µs
receiver propagation delay symmetry	$t_{PD(RX)sym}$	C_{RXD} = 20 pF	-2		2	µs

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Bus dominant wake-up time	$t_{wake(busdom)min}$	Sleep mode	30	80	150	μs
TXD dominant time-out time	$t_{to(dom)TXD}$	V_{TXD}=0V	6	-	20	ms
mode selection time	t_{msel}		3	-	30	μs
Pin RSTN						
reset time	t_{rst}		2	-	8	ms

(Unless specified otherwise; 5.5V≤V_{BAT}≤18V, -40°C≤T_j≤150°C; typical in V_{BAT}=13V, T_{amb}=25°C.)

[1] $\delta 1, \delta 3 = \frac{t_{bus(rec)(\min)}}{2 \times t_{bit}}$.

[2] Bus load conditions: (1) C_L=1nF, R_L=1kΩ; (2) C_L=6.8nF, R_L=660Ω; (3) C_L=10nF, R_L=500Ω.

[3] $\delta 2, \delta 4 = \frac{t_{bus(rec)(\max)}}{2 \times t_{bit}}$.

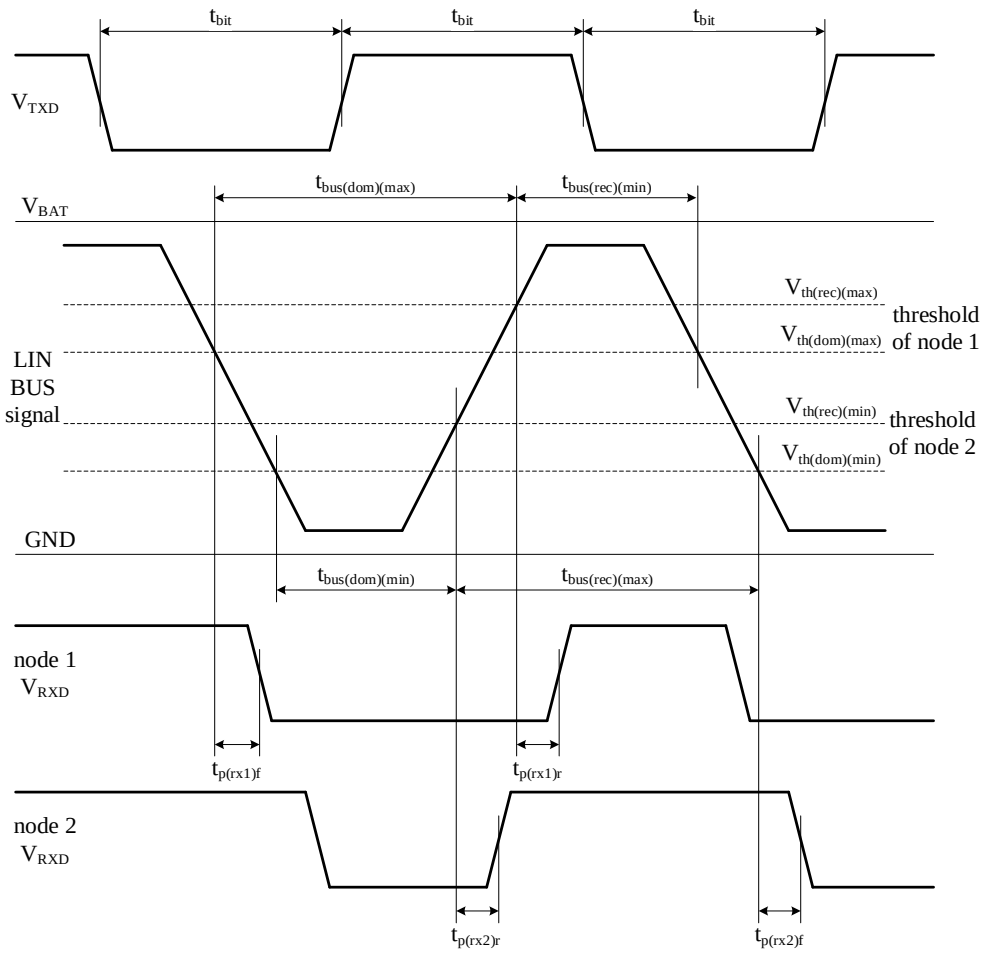


Fig. 7 Timing diagram of LIN transceiver duty cycle

TYPICAL APPLICATION

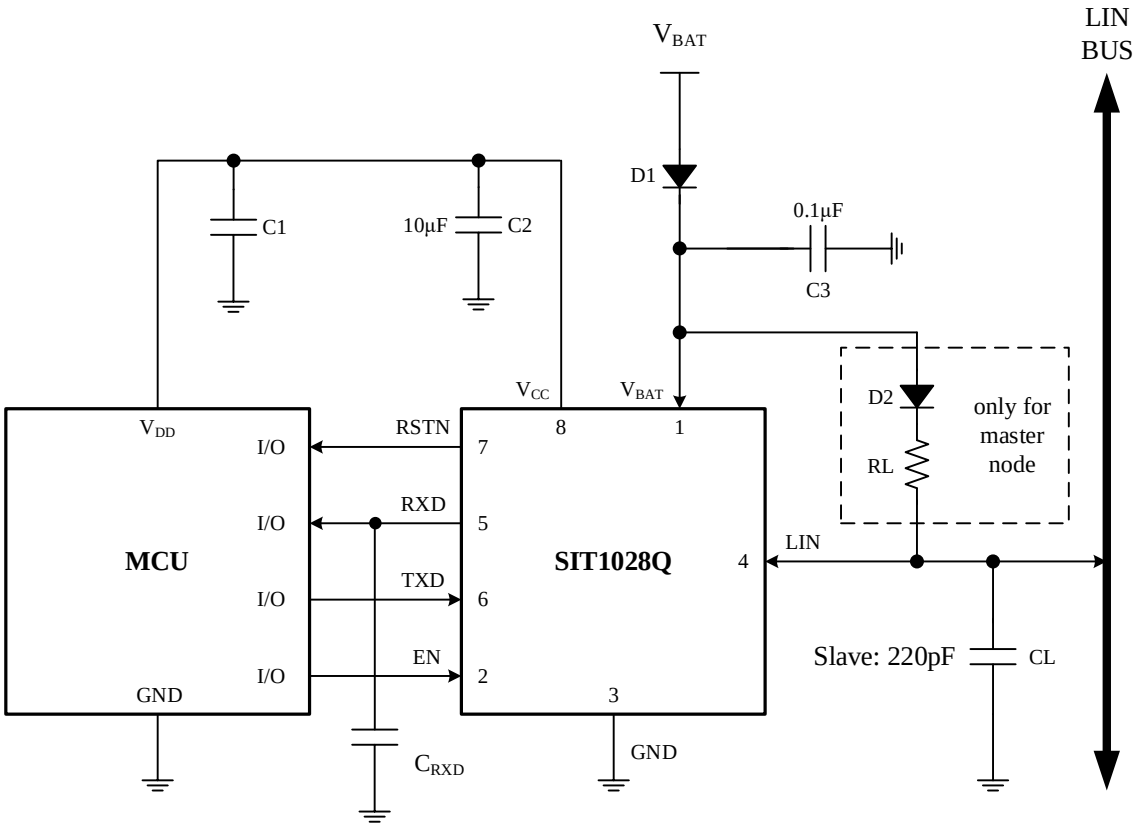


Fig. 8 Typical application of the of SIT1028Q

Note:

1) R_L/C_L combination of 660Ω/6.8nF is recommended when the master node is used to obtain a slower bus waveform slope.
2) The recommended value for C_{RXD} is 1nF. (only SIT1028QT and SIT1028QTK version)

TEST MODEL

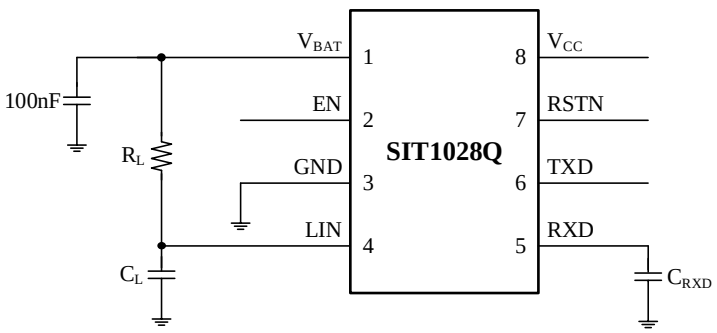
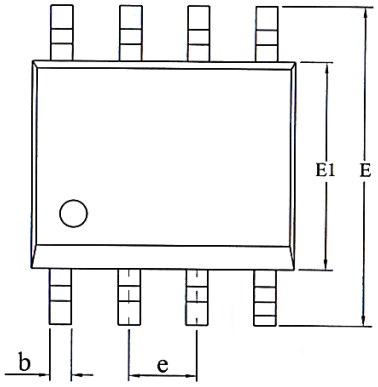


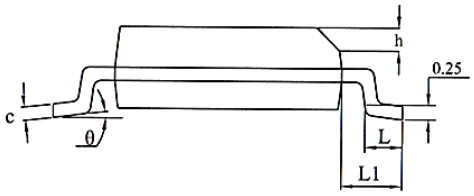
Fig. 9 Switching characteristic test circuit

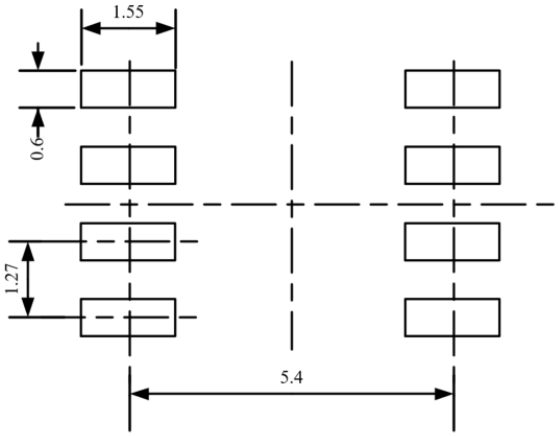
SOP8 DIMENSIONS

PACKAGE SIZE

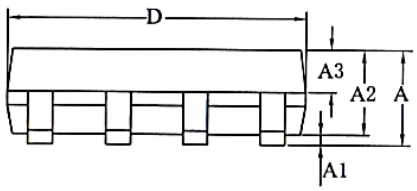
SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	1.40	-	1.80
A1	0.10	-	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.38	-	0.51
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.40	0.60	0.80
L1	1.05REF		
c	0.20	-	0.25
θ	0°	-	8°







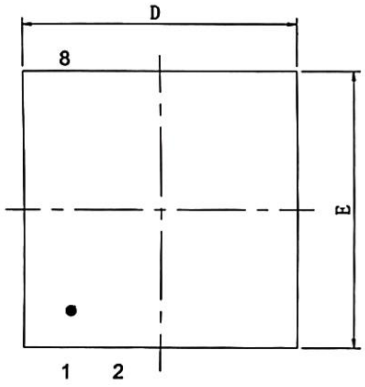
LAND PATTERN EXAMPLE (Unit: mm)

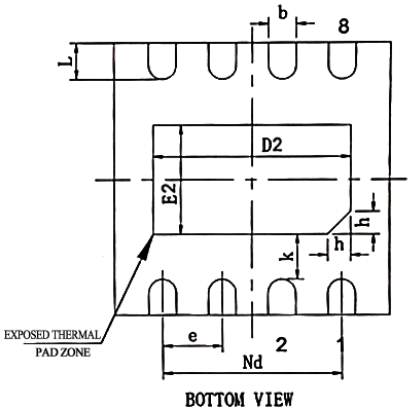


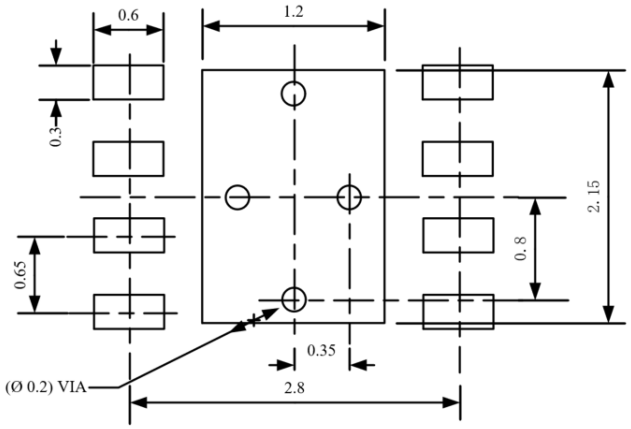
DFN3*3-8 DIMENSIONS

PACKAGE SIZE

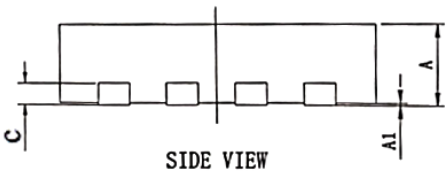
SYMBOL	MIN/mm	TYP /mm	MAX/mm
A	0.70	0.75	0.80
A1	0	0.02	0.05
c	0.203 REF		
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	2.05	2.15	2.25
Nd	1.95BSC		
E2	1.10	1.20	1.30
b	0.25	0.30	0.35
e	0.65 TYP		
k	0.50REF		
L	0.35	0.4	0.45
h	0.20	0.25	0.30



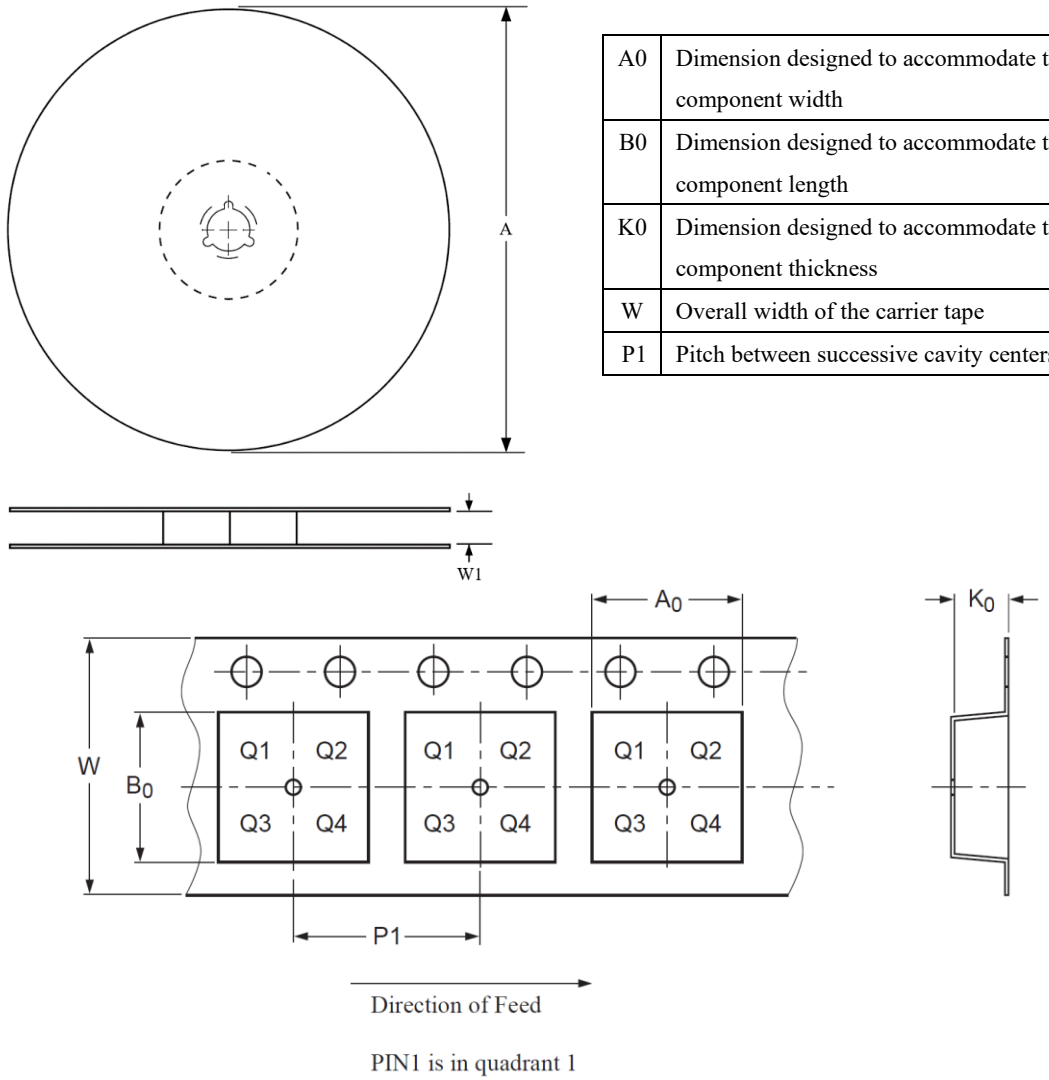




LAND PATTERN EXAMPLE (Unit: mm)



TAPE AND REEL INFORMATION



PIN1 is in quadrant 1

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Package type	Reel diameter A (mm)	Tape width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
SOP8	330±1	12.4	6.60±0.1	5.30±0.10	1.90±0.1	8.00±0.1	12.00±0.1
DFN3*3-8	329±1	12.4	3.30±0.1	3.30±0.1	1.10±0.1	8.00±0.1	12.00±0.3

ORDERING INFORMATION

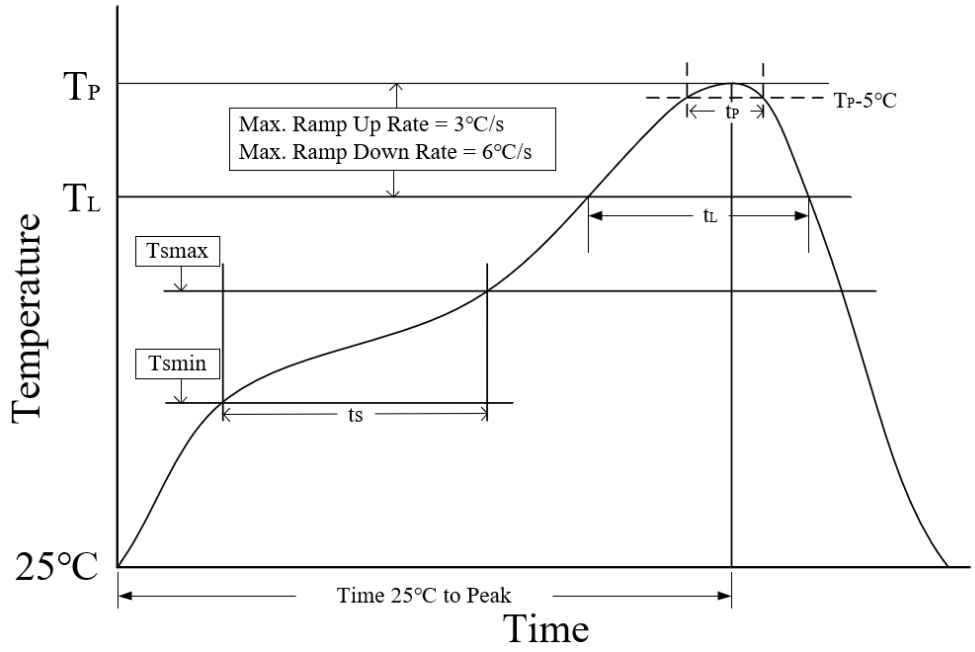
TYPE NUMBER	PACKAGE	PACKING
SIT1028QT/5V0	SOP8	Tape and reel
SIT1028QT/3V3	SOP8	Tape and reel
SIT1028QT/1/5V0	SOP8	Tape and reel
SIT1028QT/1/3V3	SOP8	Tape and reel
SIT1028QTK/5V0	DFN3*3-8, small outline, no leads	Tape and reel
SIT1028QTK/3V3	DFN3*3-8, small outline, no leads	Tape and reel
SIT1028QTK/1/5V0	DFN3*3-8, small outline, no leads	Tape and reel
SIT1028QTK/1/3V3	DFN3*3-8, small outline, no leads	Tape and reel

SOP8 is packed with 2500 pieces/disc in braided packaging. Leadless DFN3*3-8 is package with 6000 pieces/disc in braided packaging.

Note: SIT1028QT/5V0, SIT1028QTK/5V0, SIT1028QT/1/5V0 and SIT1028QTK/1/5V0 are 5V voltage regulator versions;

SIT1028QT/3V3, SIT1028QTK/3V3, SIT1028QT/1/3V3, SIT1028QTK/1/3V3 are 3.3V voltage regulator versions.

REFLOW SOLDERING



Parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	3 ℃/second max
Preheat time ts (T_{smin}=150 ℃ to T_{smax}=200 ℃)	60-120 seconds
Melting time t_L (T_L=217 ℃)	60-150 seconds
Peak temp T_P	260-265 ℃
5°C below peak temperature t_P	30 seconds
Ave cooling rate (T_P to T_L)	6 ℃/second max
Normal temperature 25℃ to peak temperature T_P time	8 minutes max

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Data sheet status	Revision date
V1.0	Initial version.	November 2022
V1.1	Added ambient temperature T_{amb} range; Updated state diagram; Updated the parameters of V_{UVD} and V_{UVR}; Deleted the parameters of thermal shutdown; Added the parameters of overtemperature protection.	March 2023
V1.2	Added AEC-Q100 qualified.	October 2023
V1.3	Updated typical application.	May 2024
V1.4	Added SIT1028QT/1 and SIT1028QTK/1 version.	December 2024