



FEATURES

- ISO 11898-2:2016, SAE J2284-1 to SAE J2284-5 and SAE J1939-14 compliant
- AEC-Q100 Grade 1 qualified
- Implements CAN Signal Improvement Capability as defined in CiA 601-4:2019 to significantly reduce signal ringing effects in a network
- Low power Sleep mode and Standby mode
- Remote wake-up function and local wake-up function
- $\pm 58\text{V}$ BUS protection
- $\pm 30\text{V}$ receiver common mode input voltage
- I/O pin supports 1.8V, 3.3V or 5V MCU
- Driver (TXD) dominant timeout function
- Undervoltage protection on VBAT, VCC and VIO pins
- High-speed CAN, support 8Mbps CAN with Flexible Data-Rate
- Sleep mode INH output pin with power disable function
- -40°C to 150°C junction temperature range with over-temperature protection
- High Electro-Magnetic Immunity (EMI) and Low Electro-Magnetic Emission (EME)
- Unpowered state disengages from the bus
- Available in SOP14 and leadless DFN4.5 \times 3-14 packages; DFN4.5 \times 3-14 with improved Automated Optical Inspection (AOI) capability

DESCRIPTION

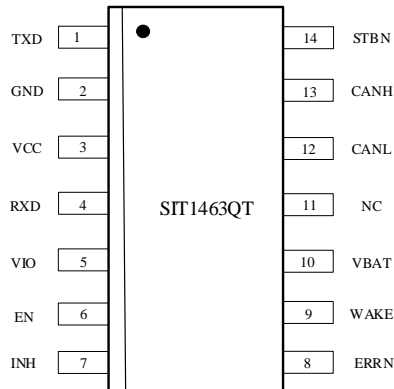
SIT1463Q is an interface chip applied between CAN protocol controller and physical bus, supports 8Mbps Flexible Data-Rate, and has the capability of differential signal transmission between bus and CAN protocol controller. SIT1463Q includes CAN Signal Improvement Capability (SIC), as defined in CiA 601-4:2019. CAN signal improvement significantly reduces signal ringing in a network, allowing reliable CAN FD communication to function in large networks with multiple unterminated stubs. The SIT1463Q features a CAN bus fault protection from -58V to $+58\text{V}$, and the receiver common mode input voltage can reach -30V to $+30\text{V}$. The SIT1463Q is powered by multiple power supplies and has multiple system protection and diagnostic functions to improve the stability of the device and CAN. In addition, SIT1463Q has five working modes: normal mode, silent mode, standby mode, sleep mode and off mode. It supports local wake-up and remote wake-up in low power mode. The provided low power mode management can greatly save the power of CAN bus application system.

Applications: Automotive and Transport

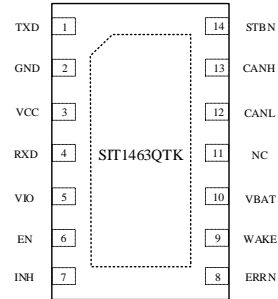
- Body Control
- Automotive Gateway
- ADAS
- Information and entertainment



PIN CONFIGURATION



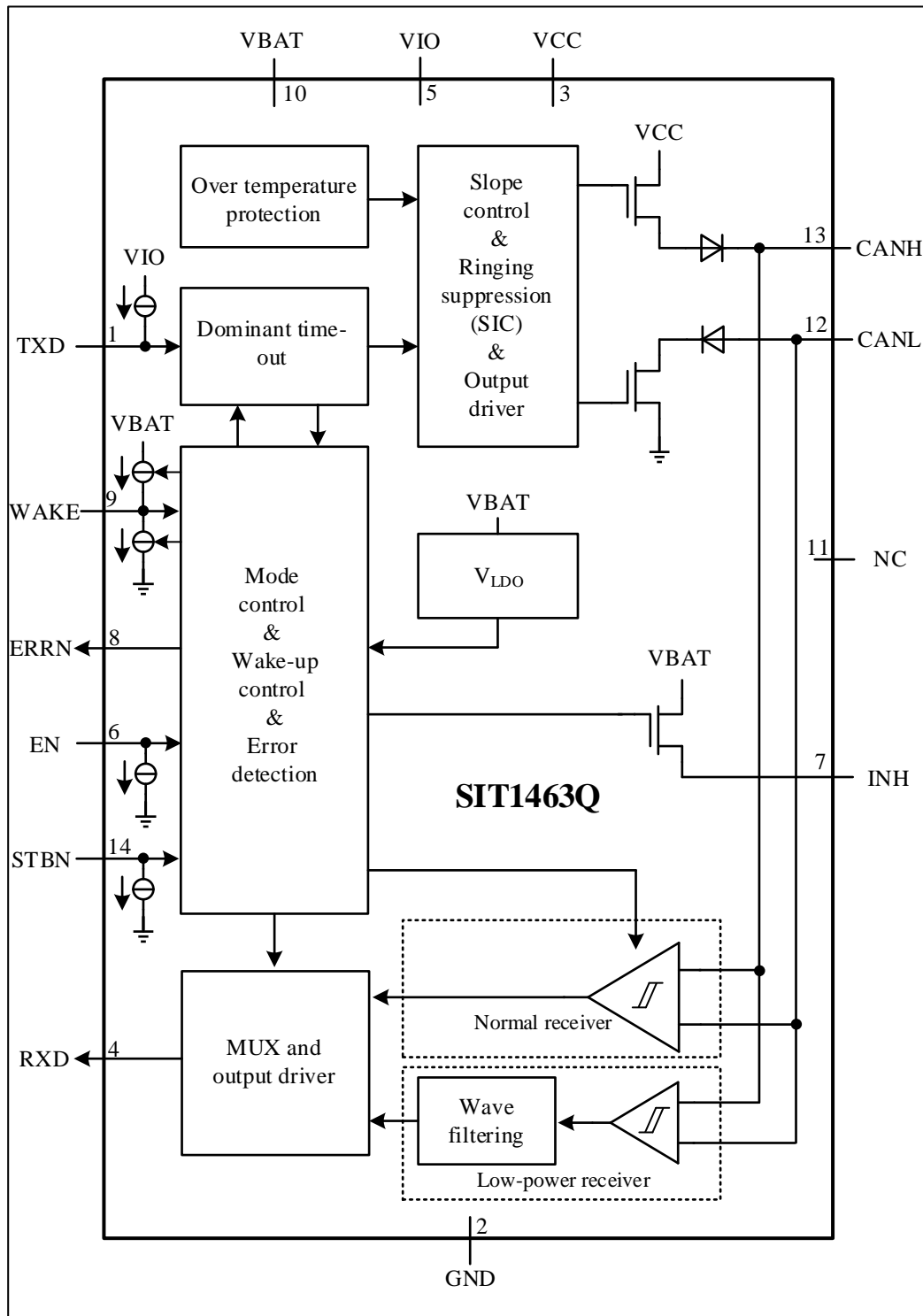
SIT1463QT: SOP14



SIT1463QTK: DFN4.5×3-14

PIN DESCRIPTION

| PIN | SYMBOL | DESCRIPTION |
|-----|--------|---|
| 1 | TXD | Transmit data input. |
| 2 | GND | Ground. |
| 3 | VCC | 5V bus power supply. |
| 4 | RXD | Receive data output; reads out data from the bus lines. |
| 5 | VIO | I/O port power supply. |
| 6 | EN | Enable control input. |
| 7 | INH | Used to control the working state of the external voltage regulator, set to high after a wake-up event. |
| 8 | ERRN | Error indication output. |
| 9 | WAKE | Local wake-up input. |
| 10 | VBAT | Battery power supply. |
| 11 | NC | No connected. |
| 12 | CANL | Low-level CAN bus input and output. |
| 13 | CANH | High-level CAN bus input and output. |
| 14 | STBN | Standby mode control input. |

INTERNAL CIRCUIT BLOCK DIAGRAM

Figure 1 SIT1463Q block diagram

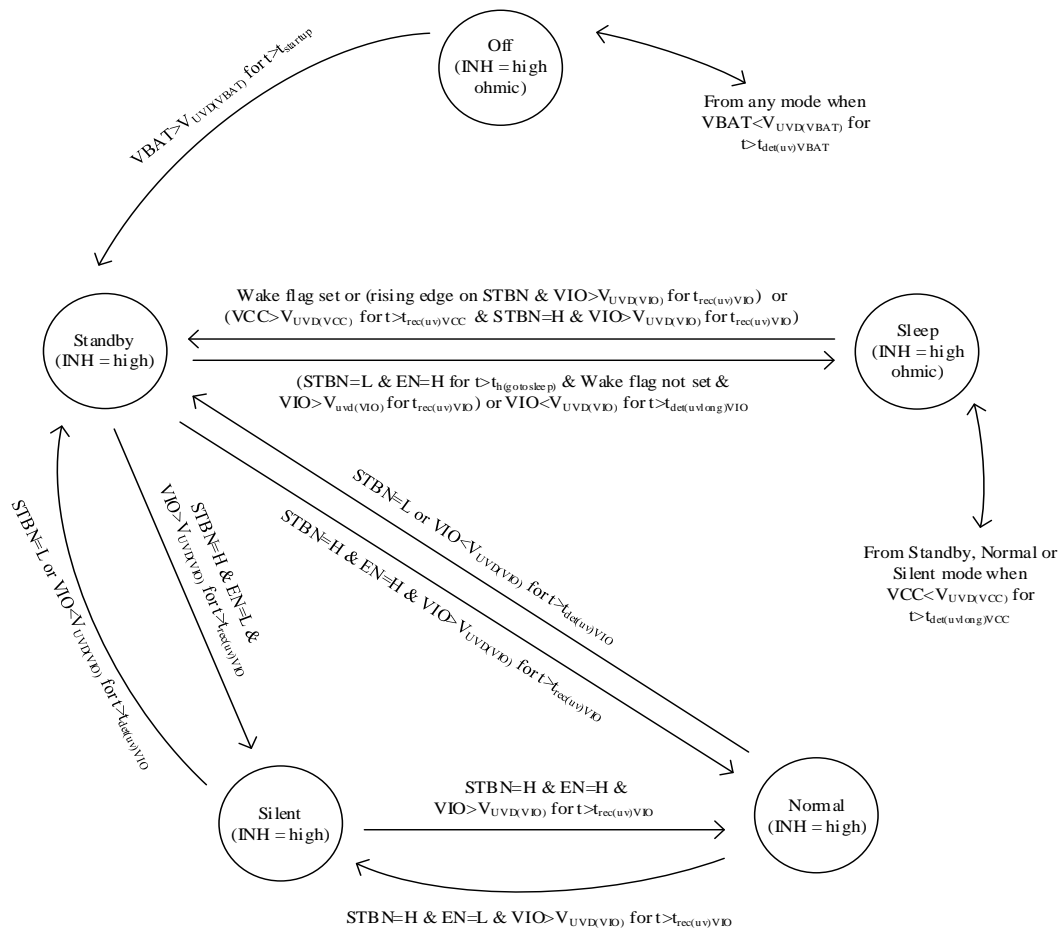
RECOMMENDED WORK STATUS

| PARAMETER | SYMBOL | VALUE | UNIT |
|--|-----------------|---------|------|
| VBAT supply voltage | VBAT | 4.5~40 | V |
| VCC supply voltage | VCC | 4.5~5.5 | V |
| VIO supply voltage | VIO | 1.7~5.5 | V |
| Logic output pin high level output current (RXD&ERRN) | $I_{OH(Logic)}$ | >-2 | mA |
| Logic output pin low level output current (RXD&ERRN) | $I_{OL(Logic)}$ | <2 | mA |
| INH output current | $I_{O(INH)}$ | <4 | mA |
| Ambient temperature | T_{amb} | -40~125 | °C |

LIMITING VALUES

| PARAMETER | SYMBOL | VALUE | UNIT |
|---|--------------------------|------------------------------|------|
| Battery power supply | VBAT | -0.3~45 | V |
| Low power supply | VCC, VIO | -0.3~7 | V |
| MCU side port | TXD, RXD, STBN, EN, ERRN | -0.3~7 | V |
| Bus side input voltage | CANH, CANL | -58~58 | V |
| Local wake-up port | WAKE | -45~45 and -45~VBAT+0.3 | V |
| Inhibit output | INH | -0.3~45 and -0.3~VBAT+0.3 | V |
| Bus differential breakdown voltage | $V_{(CANH-CANL)}$ | -58~58 | V |
| Storage temperature | T_{stg} | -55~150 | °C |
| Virtual junction temperature | T_j | -40~150 | °C |

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

MODE TRANSITIONS

Figure 2 Mode transitions

**SYSTEM OPERATING MODES****Normal mode**

Valid VCC, VIO and VBAT voltages are present, both EN and STBN are set to high level, the device will enter the normal mode. In normal mode, the driver and high-speed receiver are enabled, the driver converts the digital input signal on the TXD to the bus analog level, while the receiver monitors the bus level and reacts it to the RXD. INH will be pulled high in normal mode.

Silent mode

Valid VCC, VIO and VBAT voltages are present, setting EN to low level and STBN to high level, the device enters silent mode. In this mode, the driver is disabled, the high-speed receiver is enabled, the dominant and recessive signals of CANH and CANL are reflected to the RXD through the receiver. The bus will be biased to $1/2V_{CC}$, and INH will be pulled high.

Standby mode

The Standby mode is the first-level low-power mode in which the driver and high-speed receiver are disabled, the low-power receiver is enabled and the device can still detect local wake-up and remote wake-up events. INH will be pulled high in standby mode. When the chip is initially powered on, once VBAT rises above $V_{UVD(VBAT)}$ and the time is longer than $t_{stratup}$, the device will enter Standby and resulting in a high level on pin INH.

Sleep mode

Sleep mode is the lowest-power working mode of the device. There are three ways to enter Sleep mode:
 VCC undervoltage is longer than $t_{det(uvlong)VCC}$ and the VBAT is valid;
 VIO undervoltage is longer than $t_{det(uvlong)VIO}$ and the VBAT is valid;
 The power supply is valid, wake flag is not set, EN is set high, STBN is set low, when $t > t_{h(gotosleep)}$ can enter sleep mode.
 In sleep mode, the driver and high-speed receiver are disabled, the low-power receiver is enabled and the output port INH is in a high ohmic-state, which can instruct to turn off the external voltage regulator, and the VCC power supply of the transceiver and MCU will not be available. In this state, SIT1463Q maintains power supply through the battery pin VBAT, so as to ensure the monitoring work of local wake-up and remote wake-up, which can cause INH to be pulled high.

Off mode

With regardless of the state of the other pins (such as EN, STBN, VIO, VCC), once VBAT undervoltage time is longer than $t_{det(uv)V_{BAT}}$ the device can enter Off mode. In Off mode, the output pin INH, ERRN, RXD and BUS pins are in a high ohmic-state.

CAN MODE TRANSITIONS

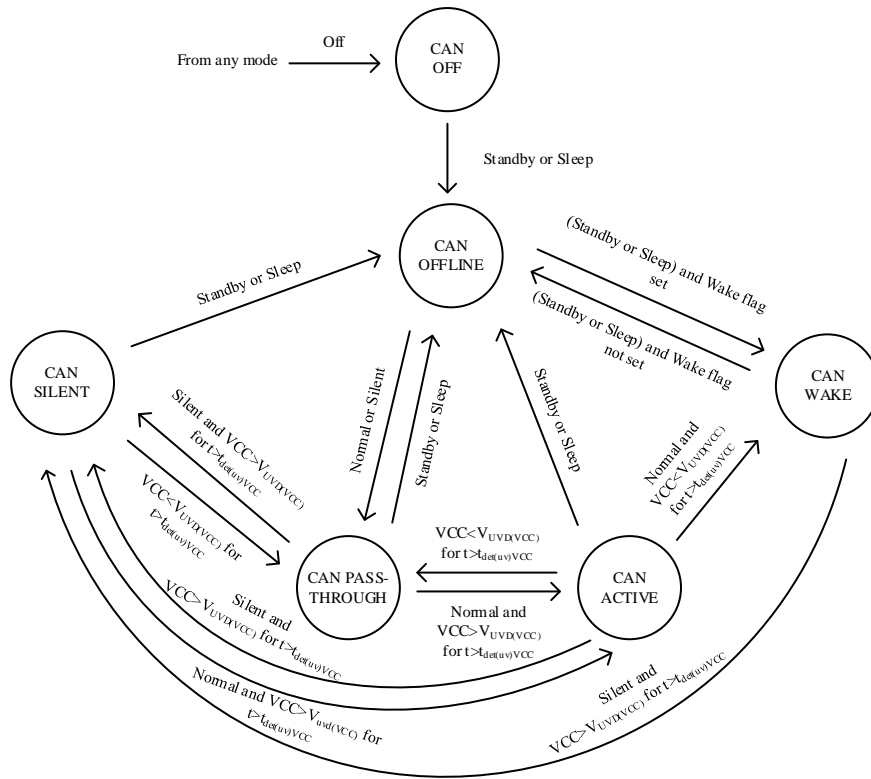


Figure 3 CAN state diagram

CAN OPERATING MODES

| |
|---|
| CAN Off |
| CAN operating mode will enter CAN Off when the device is in Off mode. The bus pins and RXD are high ohmic. The driver, low-power receiver and high-speed receiver are disabled. |
| CAN Offline |
| CAN operating mode will enter CAN Offline when the device is in Sleep or Standby mode and wake flag are not set. The bus pins are biased to GND, RXD is high. The driver and high-speed receiver are disabled. The low-power receiver is enabled. In this state, the transceiver maintains power supply through the battery pin VBAT, so as to ensure the monitoring work of local wake-up and remote wake-up. |
| CAN Wake |



CAN operating mode will enter CAN Wake when the device is in Sleep or Standby mode and wake flag is set.

The bus pins are biased to GND, RXD is low. The driver and high-speed receiver are disabled. The low-power receiver is enabled.

CAN Pass-through

CAN operating mode will enter CAN Pass-through when the device is in Normal or Silent mode and VCC undervoltage time is shorter than $t_{det(uv)VCC}$.

The bus pins are biased to GND, high-speed receiver and driver are disabled. The low-power receiver monitors the dominant and recessive signals of CANH and CANL and reflected to the RXD.

CAN Active

CAN operating mode will enter CAN Active when the device is in Normal mode and the power supply is valid.

The bus pins are biased to $VCC/2$. The driver and high-speed receiver are fully operational, the low-power receiver is off. The driver converts the digital input signal on the TXD to the bus analog level, while the receiver monitors the bus level and reacts it to the RXD. In this mode, data begin to transmit after TXD must be pulled high at least once.

CAN Silent

CAN operating mode will enter CAN Silent when the device is in Silent mode and the power supply is valid.

The bus pins are biased to $VCC/2$. The driver and low-power receiver are all off, the high-speed receiver is enabled. The dominant and recessive signals of bus are reflected to the RXD through the high-speed receiver.



FUNCTION MODE TABLE

| VCC | VIO | VBAT | EN | STBN | Wake flag | Mode | Driver | Normal Receiver | Low-power Receiver | RXD | BUS State | INH |
|---------|---------|--------|----|------|-----------|---------|---------|-----------------|--------------------|----------------|-----------|-----|
| normal | normal | normal | H | H | X | normal | enable | enable | disable | follow the bus | VCC/2 | H |
| normal | normal | normal | L | H | X | silent | disable | enable | disable | follow the bus | VCC/2 | H |
| normal | normal | normal | H | L | clear | sleep | disable | disable | enable | H | GND | Z |
| normal | normal | normal | H | L | set up | standby | disable | disable | enable | L | GND | H |
| normal | normal | normal | L | L | clear | standby | disable | disable | enable | H | GND | H |
| normal | normal | normal | L | L | set up | standby | disable | disable | enable | L | GND | H |
| UV long | normal | normal | X | X | X | sleep | disable | disable | enable | H | GND | Z |
| normal | UV long | normal | X | X | X | sleep | disable | disable | enable | Z | GND | Z |
| X | X | UV | X | X | X | off | disable | disable | disable | Z | Z | Z |

Note: H=high level; L=low level; Z=high ohmic; X=irrelevant; UV= Under Voltage

DRIVER STATUS TABLE

| MODE | TXD INPUT | BUS OUTPUT | | BUS STATE |
|--------------|-----------|------------|------|---------------------|
| | | CANH | CANL | |
| Normal mode | L | H | L | Dominate |
| | H or Open | Z | Z | Bus biased to VCC/2 |
| Silent mode | X | Z | Z | Bus biased to VCC/2 |
| Standby mode | X | Z | Z | Bus biased to GND |
| Sleep mode | X | Z | Z | Bus biased to GND |
| Off mode | X | Z | Z | High ohmic |

Note: H=high level; L=low level; Z=high ohmic; X=irrelevant

**RECEIVER FUNCTION TABLE**

| MODE | BUS DIFFERENTIAL INPUT $V_{OD}=CANH-CANL$ | BUS STATE | RXD OUTPUT |
|--------------------------------|--|-----------|--------------------------------------|
| Normal mode and Silent mode | $V_{OD} \geq 0.9V$ | Dominate | L |
| | $0.9V > V_{OD} > 0.5V$ | ? | ? |
| | $V_{OD} \leq 0.5V$ | Recessive | H |
| Standby mode and Sleep mode | $V_{OD} \geq 1.15V$ | Dominate | H, L when the wake-up flag set |
| | $1.15V > V_{OD} > 0.4V$ | ? | |
| | $V_{OD} \leq 0.4V$ | Recessive | |

Note: H=high level; L=low level; ?=uncertain; Valid VCC, VIO and VBAT voltages are present.

INTERNAL FLAG SIGNAL

| FLAG SIGNAL | REASON FOR APPEARING | EXTERNAL INDICATION | FLAG SIGNAL CLEAR | NOTE |
|------------------------------------|---|--|--|---|
| Power-on flag | VBAT power-on | Enter silent mode (from standby mode, sleep mode) ERRN=L | Enter normal mode | |
| Wake-up request flag | Remote wake-up, local wake-up, initial power-on | Enter standby mode or sleep mode ERRN=RXD=L | Enter normal mode, VCC or VIO undervoltage | |
| Wake-up source flag ⁽¹⁾ | Local wake-up, initial power-on | Enter normal mode: ERRN=L indicates local wake-up | Leaving normal mode, VCC or VIO undervoltage | The establishment of the power-up flag sets the wake-up source flag |
| Local failure flag | TXD dominant timeout | When entering silent mode from normal mode ERRN=L | RXD=L&TXD=H or enter normal mode | Once a TXD dominant timeout occurs, the drive will be disabled |
| | TXD shorted to RXD | When entering silent mode from normal mode ERRN=L | | A short circuit of TXD to RXD occurs, the driver will be disabled |
| | Bus dominant timeout | When entering silent mode from normal mode ERRN=L | RXD=H or enter normal mode | A bus timeout occurred and the drive is still enabled |
| | Over temperature protection | When entering silent mode from normal mode ERRN=L | The junction temperature returns to normal and RXD=L&TXD=H or the junction temperature returns to normal and jumps back to normal operation mode | In the event of an overtemperature condition, the driver will be disabled |

(1) The wake-up source flag will only identify the first wake-up request signal;

The device carries out system diagnosis through the above series of flag signals and indicates the cause of the failure. The MCU can judge the internal working state of the system or the cause of the fault through some mode switching and the indication of the transceiver chip ERRN and RXD pins.

Power-on flag

The power-on flag refers specifically to the power-on event of the battery power supply VBAT. The power-on flag is set when VBAT returns to normal operating voltage from a voltage lower than $V_{UVD}(VBAT)$. Once the device enters silent mode from standby or sleep mode, ERRN is pulled low to indicate that the power-on flag is set. When entering normal operating mode, the power-on flag will be cleared. The power-on flag sets the wake-up request flag and wake-up source flag.

Wake-up request flag

SIT1463Q can realize low-power wake-up function in two ways: local wake-up and remote wake-up.

Local wake-up

SIT1463Q realizes the function of local wake-up through the WAKE pin. In standby mode or sleep mode, as long as there is a valid rising or falling edge on the WAKE pin, it will be detected as a local wake-up event. A valid rising edge means that the voltage of the WAKE port jumps from a voltage lower than $V_{th}(WAKE)$ to a voltage higher than $V_{th}(WAKE)$, and the duration of this jump is longer than $t_{wake(local)}$, which can be considered as a valid rising edge, as shown in Figure 4; a valid falling edge is when the voltage at the WAKE port transitions from a voltage above $V_{th}(WAKE)$ to a voltage below $V_{th}(WAKE)$, and the duration of this transition is greater than $t_{wake(local)}$, which can be considered as a valid falling edge, as shown in Figure 5. Any transitions of duration less than $t_{wake(local)}$ and transitions that do not cross the threshold voltage $V_{th}(WAKE)$ will be filtered out.

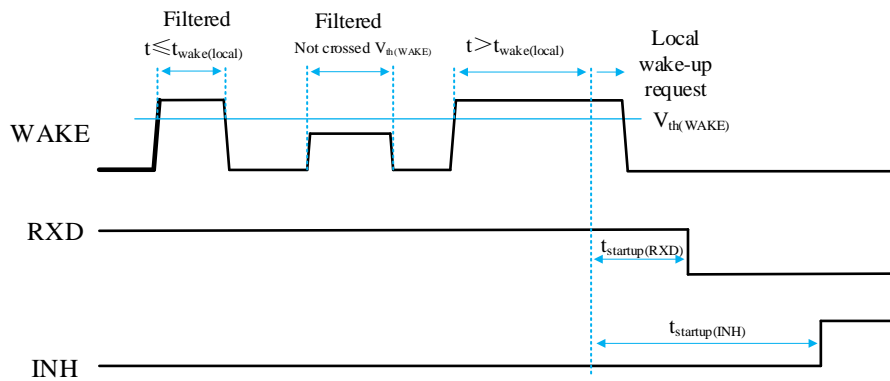


Figure 4 Local wake-up for WAKE rising edge

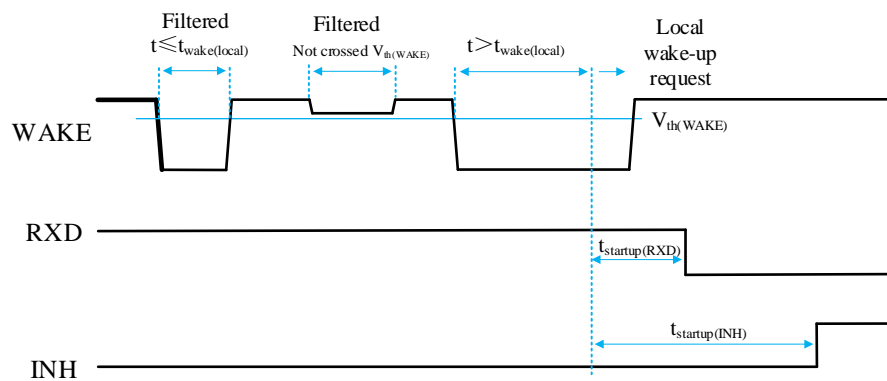


Figure 5 Local wake-up for WAKE falling edge

Remote wake-up

The SIT1463Q implements a remote wake-up function through a low-power receiver to inform the MCU that the bus has been activated and the node should resume normal operation. In sleep mode, when a valid remote wake-up pattern (WUP) appears, the device will wake up and jump to standby mode, RXD will be pulled low after $t_{startup(RXD)}$ and INH will be pulled high after $t_{startup(INH)}$.

According to ISO11898-2:2016, the complete WUP consists of: a filtered dominant level (duration greater than $t_{wake(dom)}$), a filtered recessive level (duration greater than $t_{wake(rec)}$) and another filtered dominant level flat (duration greater than $t_{wake(dom)}$). This dominant-recessive-dominant level signal must appear within $t_{wake(timeout)}$ time, otherwise the internal wake-up logic will be reset and restart the monitoring of the bus.

The RXD pin will remain high until the wake-up event is triggered. The above mentioned dominant and recessive levels will be ignored (filtered out) if the duration is lower than $t_{wake(busdom)}$ and $t_{wake(busrec)}$. A wake-up event will not be responded when any of the following events occurs while a valid wakeup pattern is received:

- (1) The device switches to the normal working mode;
- (2) The complete wake-up request frame is not received within the $t_{wake(timeout)}$;
- (3) VCC or VIO undervoltage is detected.

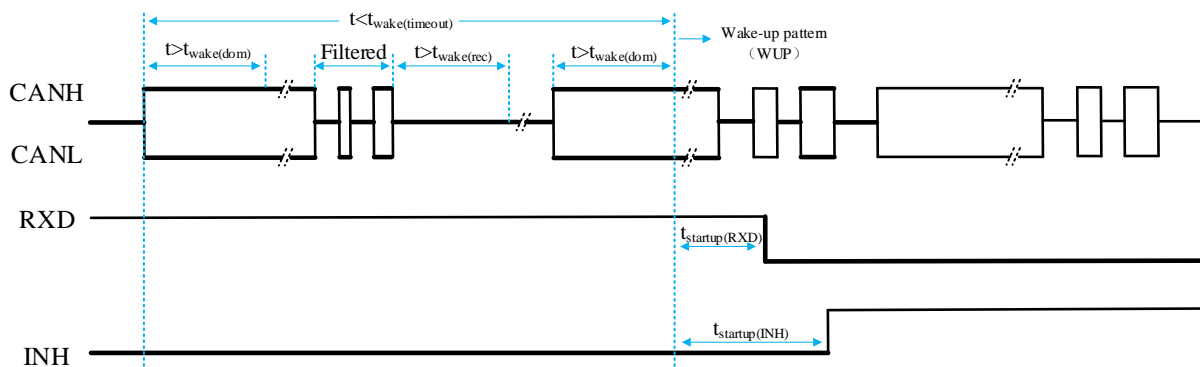


Figure 6 Remote wake-up diagram

Wake-up source flag

SIT1463Q can identify the wake-up source through the wake-up source flag, and the wake-up source flag can be represented by the level of the ERRN pin when the chip enters the normal mode. If the wake-up flag is generated by the local wake-up request given by the WAKE pin, the ERRN pin is low level after jumping to the normal operating mode. The chip leaving the normal operating mode also clears the wake-up source flag. This flag is also generated on initial power-on.

Local failure flag

SIT1463Q can detect four kinds of local failure events: TXD dominant timeout, TXD and RXD short circuit, bus dominant timeout, over temperature protection. Whenever any of these events occur, a local failure flag is generated, and when the device transitions from normal mode to silent mode, ERRN is pulled low, indicating that a local failure flag has been set.

TXD dominant timeout

In normal mode, if a low level voltage on pin TXD lasts longer than the internal timer value $t_{dom(TXD)}$, the transmitter will be disabled, driving the bus into a recessive state. This prevents the bus line from being driven to a permanent dominant state (blocking all network traffic) due to a hardware or software application failure on pin TXD being forced permanently low.

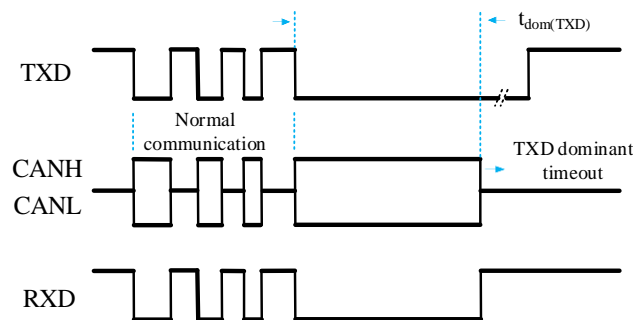


Figure 7 TXD dominant timeout diagram

TXD and RXD short circuit

SIT1463Q has the protection function of short circuit between TXD and RXD, which can avoid the periodic deadlock situation of the local device. In normal mode or silent mode, if a short circuit occurs between the TXD and RXD of the device, and the duration of the short circuit exceeds $t_{dom(TXD)}$, the device will consider that a short circuit between TXD and RXD has occurred, the local failure flag is established, and the driver will be disabled.

Bus dominant timeout

When the bus is short-circuited, if the bus has a dominant level whose duration is greater than the internal timer value $t_{dom(BUS)}$, it will be regarded as a bus dominant timeout event and a local failure flag will be established.

Over temperature protection

SIT1463Q has an over temperature protection function. If the junction temperature of the device exceeds the over temperature shutdown temperature $T_{j(sd)}$, the bus driver circuit will be shut down, thereby blocking the transmission path from TXD to the bus, so during thermal shutdown the level is biased in a recessive state while the rest of the chip remains functional. Because the driver tube is the main energy consuming component, turning off the driver tube can reduce the power consumption and thus reduce the chip temperature.

DC PARAMETERS

Tested under recommended operating conditions: VBAT=4.5V to 40V, VCC=4.5V to 5.5V, VIO=1.7V to 5.5V, T_{amb}=-40°C to 125°C. Unless otherwise stated, all typical values are measured at T_{amb}=25°C, supply voltage VBAT=12V, VCC=5V, VIO=5V, R_L=60Ω.

| PARAMETER | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT | |
|-------------------------------------|------------------------|--|------|------|------|------|----|
| VBAT supply characteristics | | | | | | | |
| VBAT supply voltage | VBAT | | 4.5 | | 40 | V | |
| VBAT supply current | I _{BAT} | Normal or Silent mode | | 60 | 100 | μA | |
| | | Standby mode | | 18 | 28 | μA | |
| | | Sleep mode | | 16 | 26 | μA | |
| VBAT undervoltage detection voltage | V _{UVD(VBAT)} | VBAT undervoltage threshold | 4 | | 4.4 | V | |
| | | VBAT undervoltage recovery threshold | 4.1 | | 4.5 | V | |
| VCC supply characteristics | | | | | | | |
| VCC supply voltage | VCC | | 4.5 | | 5.5 | V | |
| VCC supply current | I _{CC} | Normal dominant, TXD=0V | | 42 | 70 | mA | |
| | | Normal recessive, TXD=VIO | | 4.3 | 7 | mA | |
| | | Silent mode | | 4.3 | 7 | mA | |
| | | Normal dominant, TXD=0V, bus short circuit, -3V < (CANH= CANL) < 40V | | | | 125 | mA |
| | | Standby or Sleep mode | | | | 3.5 | μA |
| VCC undervoltage detection voltage | V _{UVD(VCC)} | VCC undervoltage threshold | 3.5 | 3.8 | | V | |
| | | VCC undervoltage recovery threshold | | 4 | 4.2 | V | |
| VIO supply characteristics | | | | | | | |
| VIO supply voltage | VIO | | 1.7 | | 5.5 | V | |
| VIO supply current | I _{IO} | Normal dominant, TXD=0V | | 110 | 250 | μA | |



| PARAMETER | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------------------------------|------------------|--|--------|------|---------|------------|
| VIO supply current | I_{IO} | Normal recessive or Silent mode, TXD=VIO | | | 5 | μA |
| VIO supply current | I_{IO} | Standby or Sleep mode, TXD=VIO | | | 2.5 | μA |
| VIO undervoltage detection voltage | $V_{UVD(VIO)}$ | VIO undervoltage threshold | 1.4 | | | V |
| | | VIO undervoltage recovery threshold | | | 1.65 | V |
| TXD Pin Characteristics | | | | | | |
| HIGH-level input current | $I_{IH(TXD)}$ | TXD=VIO | -1 | | 1 | μA |
| LOW-level input current | $I_{IL(TXD)}$ | TXD=0V | -150 | | -20 | μA |
| Pull-up resistance | R_{pu} | | 20 | | 80 | k Ω |
| Unpowered leakage current | $I_{O(off)}$ | VIO=0V, TXD=5.5V | -1 | | 1 | μA |
| HIGH-level input voltage | V_{IH} | | 0.7VIO | | VIO+0.3 | V |
| LOW-level input voltage | V_{IL} | | -0.3 | | 0.3VIO | V |
| Input capacitance ⁽¹⁾ | C_i | | | | 10 | pF |
| Open voltage on pin TXD | TXD _O | | H | | | logic |
| Pin RXD Characteristics | | | | | | |
| RXD HIGH-level output current | $I_{OH(RXD)}$ | RXD=VIO-0.4V | -10 | -5 | -1 | mA |
| RXD LOW-level output current | $I_{OL(RXD)}$ | RXD=0.4V | 1 | 5 | 10 | mA |
| Pin STBN Characteristics | | | | | | |
| HIGH-level input current | $I_{IH(STBN)}$ | STBN=VIO | 20 | | 110 | μA |
| LOW-level input current | $I_{IL(STBN)}$ | STB=0V | -1 | | 1 | μA |
| Pull-down resistance | R_{pd} | | 20 | | 80 | k Ω |
| Unpowered leakage current | $I_{O(off)}$ | VIO=0V, STBN=5.5V | -1 | | 1 | μA |
| HIGH-level input voltage | V_{IH} | | 0.7VIO | | VIO+0.3 | V |
| LOW-level input voltage | V_{IL} | | -0.3 | | 0.3VIO | V |



| PARAMETER | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT |
|----------------------------------|-----------------------|--|--------|------|---------|-------|
| Input capacitance ⁽¹⁾ | C _i | | | | 10 | pF |
| Open voltage on pin STBN | STBN _O | | L | | | logic |
| Pin EN Characteristics | | | | | | |
| HIGH-level input current | I _{IH(EN)} | EN=VIO | 20 | | 110 | μA |
| LOW-level input current | I _{IL(EN)} | EN=0V | -1 | | 1 | μA |
| Pull-down resistance | R _{pd} | | 20 | | 80 | kΩ |
| Unpowered leakage current | I _{O(off)} | VIO=0V EN=5.5V | -1 | | 1 | μA |
| HIGH-level input voltage | V _{IH} | | 0.7VIO | | VIO+0.3 | V |
| LOW-level input voltage | V _{IL} | | -0.3 | | 0.3VIO | V |
| Input capacitance ⁽¹⁾ | C _i | | | | 10 | pF |
| Open voltage on pin EN | EN _O | | L | | | logic |
| Pin ERRN Characteristics | | | | | | |
| ERRN HIGH-level output current | I _{OH(ERRN)} | ERRN=VIO-0.4V | -50 | | -4 | μA |
| ERRN LOW-level output current | I _{OL(ERRN)} | ERRN=0.4V | 0.1 | | 2 | mA |
| INH Pin Characteristics | | | | | | |
| INH HIGH-level voltage drop | ΔV _H | ΔV _H =V _{BAT} -INH; INH =-1mA | 0 | | 1 | V |
| | | ΔV _H =V _{BAT} -INH; INH =-2mA | 0 | | 2 | V |
| INH leakage current | I _L | Sleep mode or Off mode | -2 | 0 | 2 | μA |
| Short-circuit output current | I _{O(sc)} | V _{INH} =0V | -15 | | | mA |
| WAKE Pin Characteristics | | | | | | |
| WAKE HIGH-level input current | I _{IH(WAKE)} | WAKE>2.6V | -8 | -4 | -2 | μA |
| WAKE LOW-level input current | I _{IL(WAKE)} | WAKE<1.8V | 2 | 4 | 8 | μA |
| HIGH-level input voltage | V _{IH} | | 1.9 | 2.3 | 2.6 | V |
| LOW-level input voltage | V _{IL} | | 1.8 | 2.2 | 2.5 | V |



| PARAMETER | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|------------------------------|--|--------------------|--------------------|--------------------|------|
| Hysteresis voltage on pin WAKE | V _{hys} | | | 100 | | mV |
| Bus lines; pins CANH and CANL | | | | | | |
| CANH dominant output voltage | V _{OH(D)} | Normal mode; TXD=0V, R _L =50Ω to 65Ω | 2.75 | 3.5 | 4.5 | V |
| CANL dominant output voltage | V _{OL(D)} | | 0.5 | 1.5 | 2.25 | V |
| Bus dominant differential output voltage | V _{OD(D)} | Normal mode, TXD=0V, R _L =50Ω to 65Ω | 1.5 | | 3 | V |
| | | Normal mode, TXD=0V, R _L =45Ω to 70Ω | 1.4 | | 3.3 | V |
| | | Normal mode, TXD=0V, R _L =2240Ω | 1.5 | | 5 | V |
| Bus recessive output voltage | V _{O(R)} | Normal or Silent mode, TXD=IO, no load | 2 | 0.5V _{CC} | 3 | V |
| Bus recessive differential output voltage | V _{OD(R)} | Normal or Silent mode, TXD=IO, no load | -500 | | 50 | mV |
| Bus output voltage (bus is biased to ground) | V _{O(S)} | Sleep mode or Standby mode, no load | -0.1 | | 0.1 | V |
| Bus differential output voltage (bus is biased to ground) | V _{OD(S)} | Sleep mode or Standby mode, no load | -0.2 | | 0.2 | V |
| Dominant output voltage symmetry | V _{dom(TX) sym} | V _{dom(TX)sym} =V _{CC} - CANH-CANL | -400 | | 400 | mV |
| Transmitter voltage symmetry ⁽¹⁾ | V _{TXsym} | V _{TXsym} = CANH + CANL, R _L =60Ω, C _{SPLIT} =4.7nF, f _{TXD} =250kHz, 1MHz or 2.5MHz Figure 13 | 0.9V _{CC} | | 1.1V _{CC} | V |
| Common mode voltage step | V _{cm(step)} | Figure 10, Figure 13 | -150 | | 150 | mV |
| Peak-to-peak common mode voltage ⁽¹⁾ | V _{cm(p-p)} | Figure 10, Figure 13 | -300 | | 300 | mV |
| Dominant short-circuit output current | I _{O(SC)DOM} | Normal mode, TXD=0V, CANH=-15V to 40V | -100 | -70 | | mA |

| PARAMETER | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT |
|--|-----------------------|---|------|------|------|------------|
| Dominant short-circuit output current | $I_{O(SC)DOM}$ | Normal mode, TXD=0V, CANL=-15V to 40V | | 70 | 100 | mA |
| Recessive short-circuit output current | $I_{O(SC)REC}$ | Normal mode, $V_{TXD}=V_{IO}$, CANH=CANL= -27V to 32V | -3 | | 3 | mA |
| Differential receiver threshold voltage | $V_{th(RX)dif}$ | Normal or Silent mode, $-30V \leq V_{CM} \leq 30V$ | 0.5 | | 0.9 | V |
| | | Standby or Sleep mode, $-12V \leq V_{CM} \leq 12V$ | 0.4 | | 1.15 | V |
| Differential receiver hysteresis voltage | $V_{hys(RX)dif}$ | Normal or Silent mode, $-30V \leq V_{CM} \leq 30V$ | 50 | 120 | 400 | mV |
| Receiver recessive voltage | $V_{rec(RX)}$ | Normal or Silent mode, $-30V \leq V_{CM} \leq 30V$ | -3 | | +0.5 | V |
| | | Standby or Sleep mode, $-12V \leq V_{CM} \leq 12V$ | -3 | | +0.4 | V |
| Receiver dominant voltage | $V_{dom(RX)}$ | Normal or Silent mode, $-30V \leq V_{CM} \leq 30V$ | 0.9 | | 8 | V |
| | | Standby or Sleep mode, $-12V \leq V_{CM} \leq 12V$ | 1.15 | | 8 | V |
| Leakage current | I_L | $V_{CC}=V_{IO}=V_{BAT}=0V$ CANH=CANL=5V | -5 | | 5 | μA |
| CANH and CANL input resistance | R_{IN} | $-2V \leq CANH \leq 7V$ $-2V \leq CANL \leq 7V$ | 25 | 40 | 50 | k Ω |
| Differential input resistance | $R_{i(dif)}$ | $-2V \leq CANH \leq 7V$ $-2V \leq CANL \leq 7V$ | 50 | 80 | 100 | k Ω |
| CANH, CANL input resistance deviation | ΔR_{IN} | $0V \leq CANH \leq 5V$ $0V \leq CANL \leq 5V$ | -2 | | 2 | % |
| CANH, CANL input capacitance to ground ⁽¹⁾ | C_{IN} | TXD=VIO | | | 40 | pF |
| CANH, CANL differential input Capacitance ⁽¹⁾ | C_{ID} | TXD=VIO | | | 20 | pF |
| Differential input resistance in dominant phase ⁽¹⁾ | $R_{ID(dom)}$ | Figure 11 | | 40 | | Ω |
| Differential input resistance in active recessive drive phase ⁽¹⁾ | $R_{ID(active_rec)}$ | Figure 11 | | 60 | | Ω |



| PARAMETER | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT |
|--|-----------------------|---|------|------|------|------|
| Signal Improvement function and CAN FD device characteristics (according to CiA601-4:2019) ⁽¹⁾ | | | | | | |
| SIC time | $t_{SIC_TXD_base}$ | TXD to SIC end | | | 530 | ns |
| Transmitted recessive bit width | $\Delta t_{bit(BUS)}$ | $\Delta t_{bit(BUS)} = t_{bit(BUS)} - t_{bit(TXD)}$ | -10 | | +10 | ns |
| Bit pulse width symmetry | Δt_{rec} | | -20 | | 15 | ns |
| Received recessive bit width deviation | $\Delta t_{bit(RXD)}$ | $\Delta t_{bit(RXD)} = t_{bit(RXD)} - t_{bit(TXD)}$ | -30 | | +20 | ns |
| Temperature detection ⁽¹⁾ | | | | | | |
| Shutdown junction temperature | $T_{j(sd)}$ | Overtemperature protection | 180 | 190 | 205 | °C |
| | | Overtemperature recovery | 160 | 170 | 185 | °C |
| | | hysteresis | | 20 | | °C |

(1) Not test in product, guaranteed by design.

**AC PARAMETERS**

Unless otherwise stated, all typical values are measured at $T_{amb}=25^{\circ}\text{C}$, supply voltage $V_{BAT}=12\text{V}$, $V_{CC}=5\text{V}$, $V_{IO}=5\text{V}$, $R_L=60\Omega$, $C_{BUS}=100\text{pF}$, $C_{RXD}=15\text{pF}$.

| PARAMETER | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---------------------------------------|------------------------------|---|------|------|------|------|
| Driver AC Characteristics | | | | | | |
| Delay time from TXD to bus dominant | $t_{d(\text{TXD-busdom})}$ | Normal mode, Figure 8, Figure 12 | | | 80 | ns |
| Delay time from TXD to bus recessive | $t_{d(\text{TXD-busrec})}$ | Normal mode, Figure 8, Figure 12 | | | 80 | ns |
| Differential output rising time | $t_{r(\text{BUS})}$ | | | 35 | | ns |
| Differential output falling time | $t_{f(\text{BUS})}$ | | | 35 | | ns |
| TXD dominant time-out time | $t_{\text{dom}(\text{TXD})}$ | TXD=0, Normal mode, Figure 7 | 0.8 | 2 | 4 | ms |
| Bus dominant time-out time | $t_{\text{dom}(\text{BUS})}$ | $V_{OD}>0.9\text{V}$; Normal or Silent mode | 0.8 | 2 | 4 | ms |
| Receiver AC Characteristics | | | | | | |
| Delay time from bus dominant to RXD | $t_{d(\text{busdom-RXD})}$ | Normal or Silent mode, Figure 8, Figure 12 | | | 110 | ns |
| Delay time from bus recessive to RXD | $t_{d(\text{busrec-RXD})}$ | Normal or Silent mode, Figure 8, Figure 12 | | | 110 | ns |
| RXD signal rising time | $t_{r(\text{RXD})}$ | Normal or Silent mode | | 8 | | ns |
| RXD signal output falling time | $t_{f(\text{RXD})}$ | Normal or Silent mode | | 8 | | ns |
| TXD to RXD loop delay | | | | | | |
| Delay time from TXD LOW to RXD LOW | $t_{\text{loop}1}$ | Normal mode, Figure 8, Figure 12 | 40 | | 190 | ns |
| Delay time from TXD HIGH to RXD HIGH | $t_{\text{loop}2}$ | Normal mode, Figure 8, Figure 12 | 40 | | 190 | ns |
| CAN FD Bit time ⁽²⁾ | | | | | | |
| Bit time of BUS output pin | $t_{\text{bit}(\text{BUS})}$ | $t_{\text{bit}(\text{TXD})}=500\text{ns}$, Figure 9 | 490 | | 510 | ns |
| | | $t_{\text{bit}(\text{TXD})}=200\text{ns}$, Figure 9 | 190 | | 210 | ns |
| | | $t_{\text{bit}(\text{TXD})}=125\text{ns}$, Figure 9 | 115 | | 135 | ns |

| PARAMETER | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT |
|--|-----------------------------|--|------|------|------|---------|
| Bit time on pin RXD | $t_{bit(RXD)}$ | $t_{bit(TXD)}=500ns$, Figure 9 | 470 | | 520 | ns |
| | | $t_{bit(TXD)}=200ns$, Figure 9 | 170 | | 220 | ns |
| | | $t_{bit(TXD)}=125ns$, Figure 9 | 95 | | 145 | ns |
| Time difference between BUS and RXD output bits | Δt_{rec} | $\Delta t_{rec}= t_{bit(RXD)}- t_{bit(BUS)}$, $t_{bit(TXD)}=500ns$ | -20 | | 15 | ns |
| | | $\Delta t_{rec}= t_{bit(RXD)}- t_{bit(BUS)}$, $t_{bit(TXD)}=200ns$ | -20 | | 15 | ns |
| | | $\Delta t_{rec}= t_{bit(RXD)}- t_{bit(BUS)}$, $t_{bit(TXD)}=125ns$ | -20 | | 15 | ns |
| Device Switching Characteristics | | | | | | |
| Bus wake-up dominant time | $t_{wake(dom)}$ | Standby or Sleep mode | 0.5 | | 1.8 | μs |
| Bus wake-up recessive time | $t_{wake(rec)}$ | Standby or Sleep mode | 0.5 | | 1.8 | μs |
| Bus wake-up time-out time | $t_{wake(timeout)}$ | Standby or Sleep mode | 0.8 | | 4 | ms |
| Mode change transition time | $t_t(moch)$ | | | | 50 | μs |
| Start-up time | $t_{startup}$ | | | | 1.5 | ms |
| RXD start-up time | $t_{startup(RXD)}$ | | 4 | | 20 | μs |
| INH start-up time | $t_{startup(INH)}$ | | 4 | | 50 | μs |
| Go-to-sleep hold time | $t_h(gotosleep)$ | | 24 | | 50 | μs |
| Delay time from mode change to ERRN ⁽¹⁾ | $t_d(moch-ERRN)$ | | | | 20 | μs |
| Local wake-up time ⁽¹⁾ | t_{wake} | Standby or Sleep mode | 5 | | 50 | μs |
| STBN and EN pin filter time ⁽¹⁾ | t_{filter_IO} | | 1 | | 10 | μs |
| Undervoltage detection time | $t_{det(uv)V\text{BAT}}$ | On pin VBAT ⁽¹⁾ | | | 30 | μs |
| | $t_{det(uv)V\text{CC}}$ | On pin VCC ⁽¹⁾ | | | 30 | μs |
| | $t_{det(uv)V\text{IO}}$ | On pin VIO ⁽¹⁾ | | | 30 | μs |
| | $t_{det(uvlong)V\text{CC}}$ | On pin VCC | 100 | | 150 | ms |
| | $t_{det(uvlong)V\text{IO}}$ | On pin VIO | 100 | | 150 | ms |
| Undervoltage recovery time | $t_{rec(uv)V\text{CC}}$ | On pin VCC ⁽¹⁾ | | | 50 | μs |
| | $t_{rec(uv)V\text{IO}}$ | On pin VIO ⁽¹⁾ | | | 50 | μs |

(1) Not test in product, guaranteed by design.

(2) 8Mbit/s requires a VIO range of 2.8V to 5.5V.

**ESD RATINGS**

| PARAMETER | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT |
|--|----------------------|--|-------|------|-------|------|
| Contact discharge model (IEC) ⁽¹⁾ | V _{ESD_IEC} | Pins CANH and CANL | -6 | | +6 | kV |
| | | On VBAT pin with 10nF capacitance; On WAKE pin with 33kΩ resistor | -8 | | +8 | kV |
| Human body model (HBM) ⁽²⁾ | V _{ESD_HBM} | All ports | -8 | | +8 | kV |
| Charged device model (CDM) ⁽³⁾ | V _{ESD_CDM} | All ports | -1500 | | +1500 | V |

(1) According to IEC 61000-4-2;

(2) According to AEC-Q100-002;

(3) According to AEC-Q100-011.

TIMING WAVEFORM

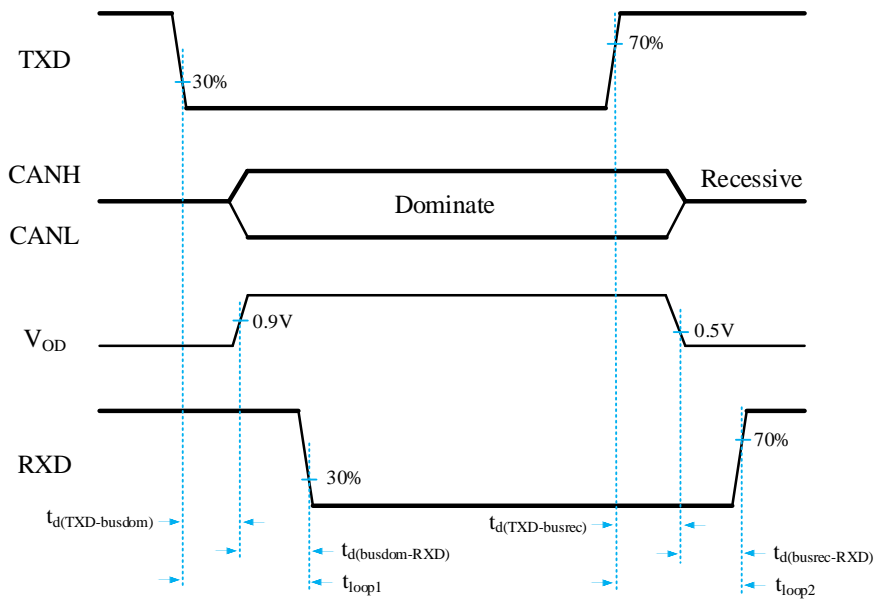


Figure 8 CAN transceiver timing diagram

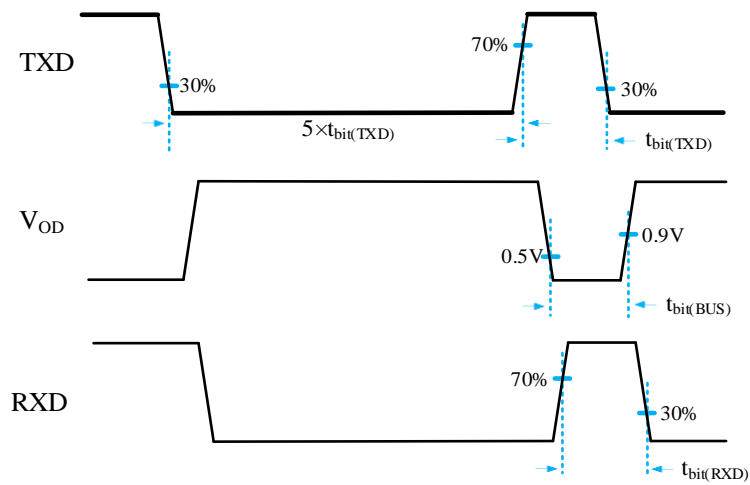


Figure 9 t_{bit} timing diagram

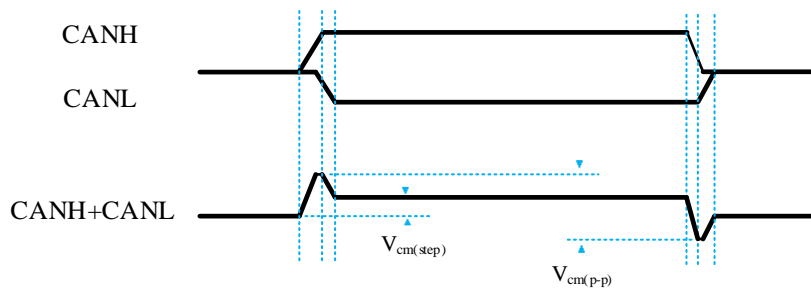


Figure 10 CAN bus common-mode voltage (according to SAE 1939-14)

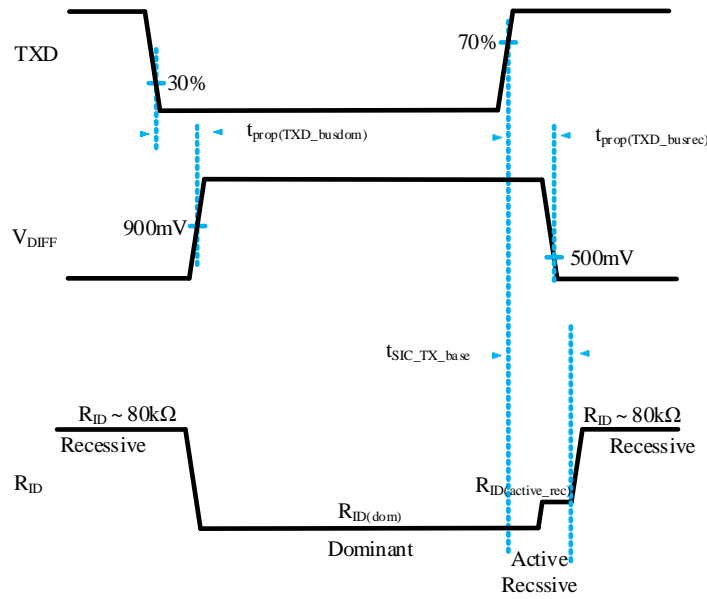


Figure 11 TXD based Signal Improvement Capability

TRANSCEIVER TEST CIRCUIT

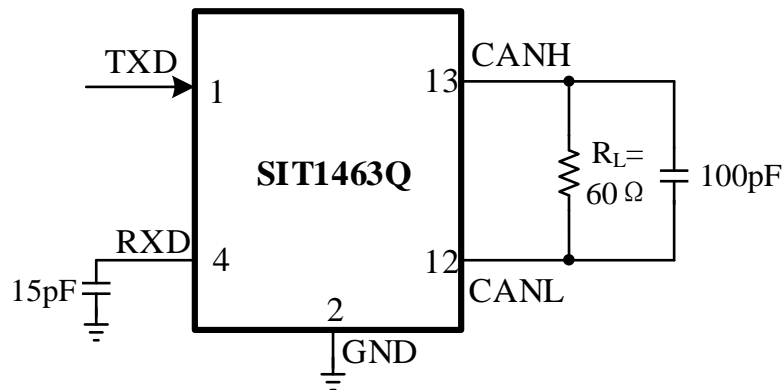


Figure 12 Transceiver timing sequence test circuit

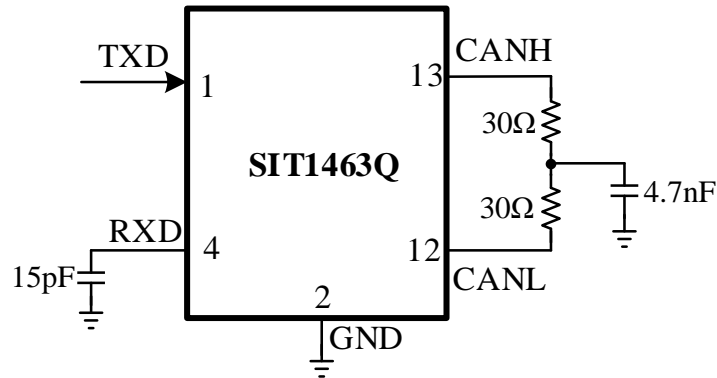
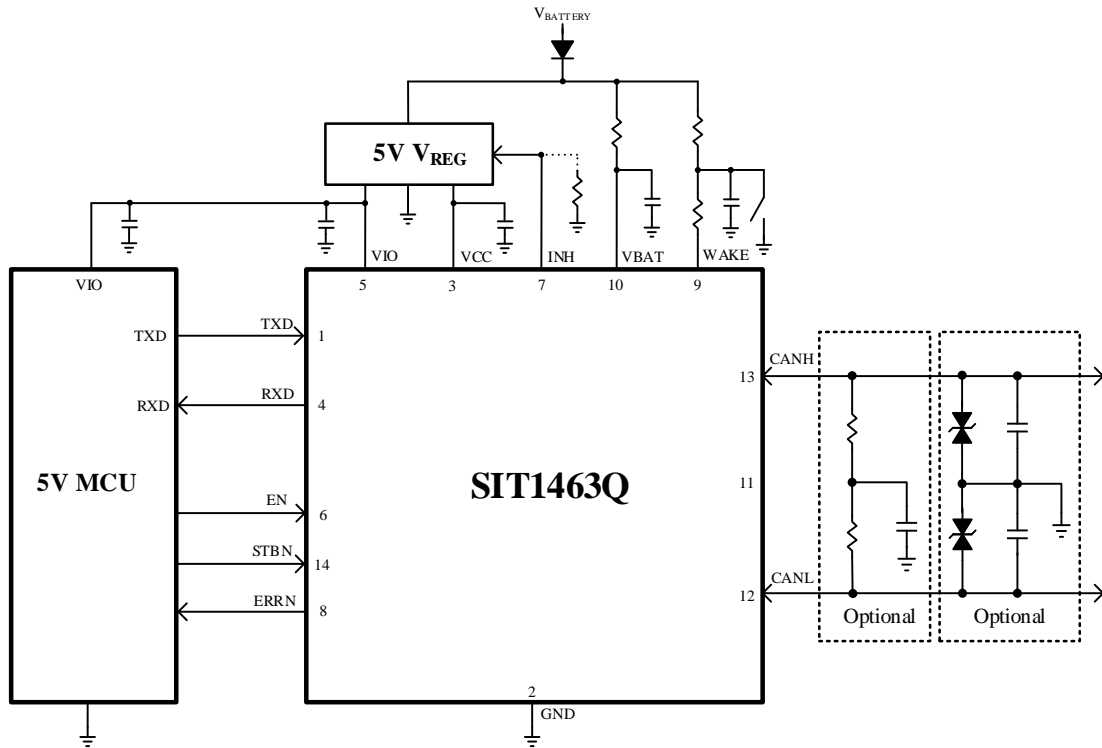
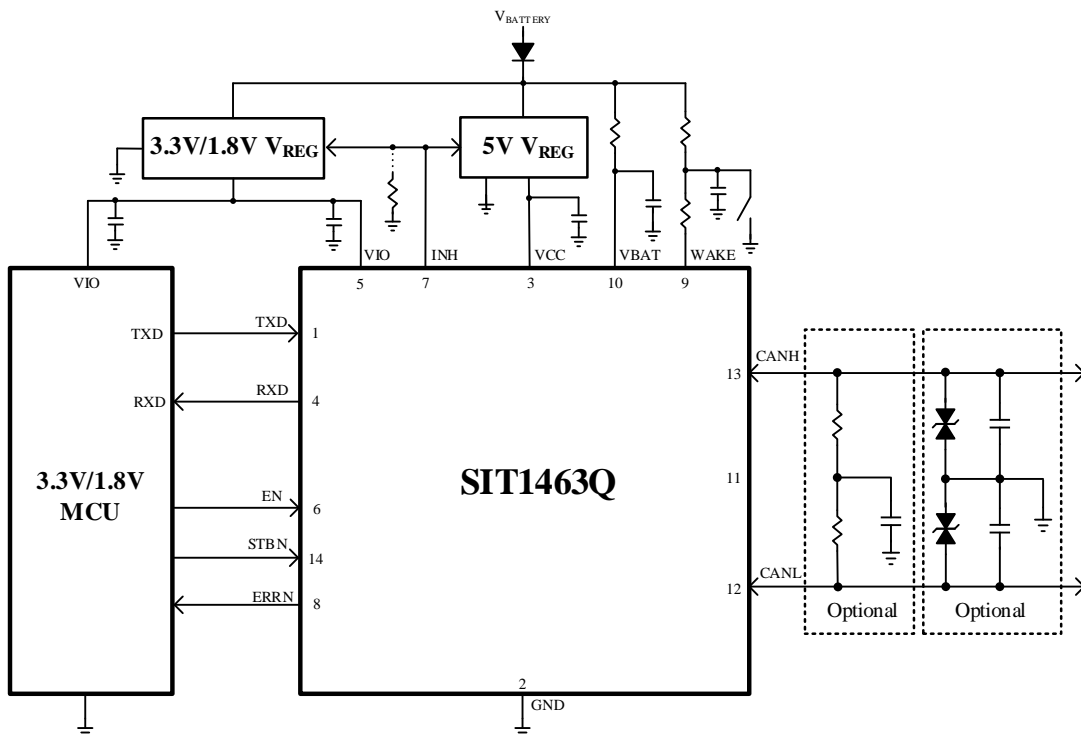


Figure 13 Transceiver bus symmetry test circuit

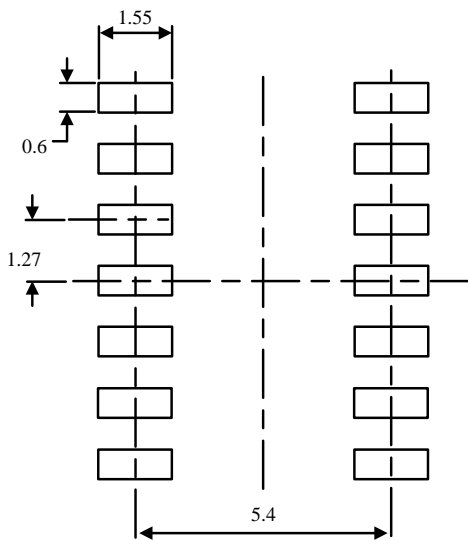
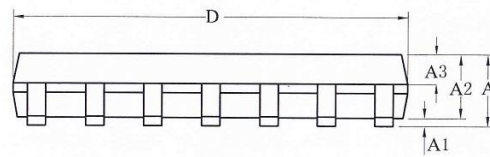
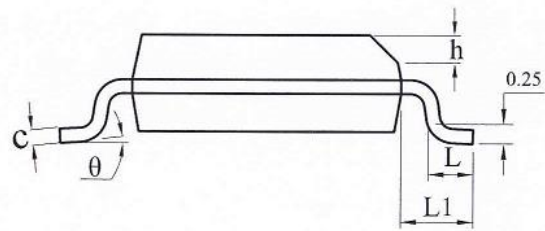
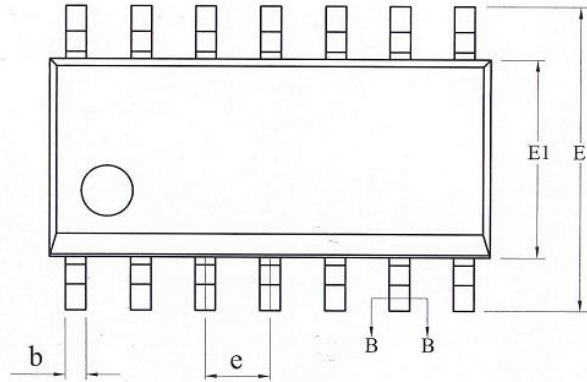
TYPICAL APPLICATION CIRCUIT

Figure 14 Typical application with 5V MCU

Figure 15 Typical application with 3.3V/1.8V MCU



SOP14 DIMENSIONS

PACKAGE SIZE

| SYMBOL | MILLIMETER | | |
|----------|------------|------|-------|
| | MIN | NOM | MAX |
| A | - | - | 1.75 |
| A1 | 0.10 | - | 0.225 |
| A2 | 1.30 | 1.40 | 1.50 |
| A3 | 0.60 | 0.65 | 0.70 |
| b | 0.39 | - | 0.47 |
| b1 | 0.38 | 0.41 | 0.44 |
| c | 0.20 | - | 0.24 |
| c1 | 0.19 | 0.20 | 0.21 |
| D | 8.55 | 8.65 | 8.75 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | 1.27BSC | | |
| h | 0.25 | - | 0.50 |
| L | 0.50 | - | 0.80 |
| L1 | 1.05REF | | |
| θ | 0 | - | 8° |



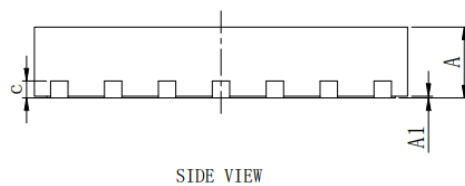
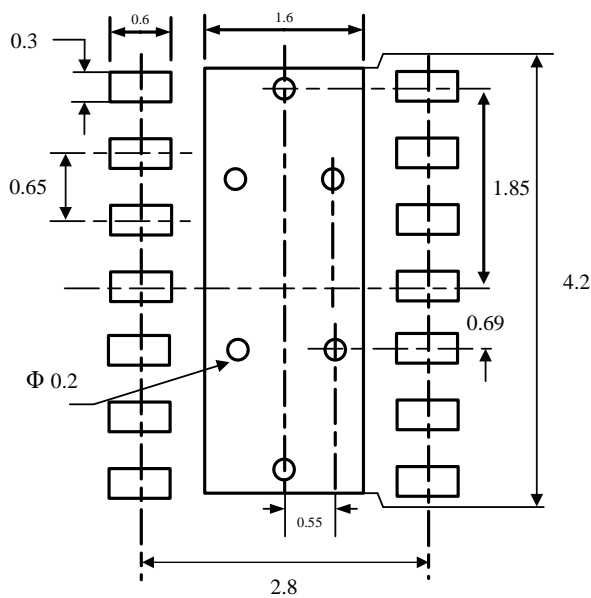
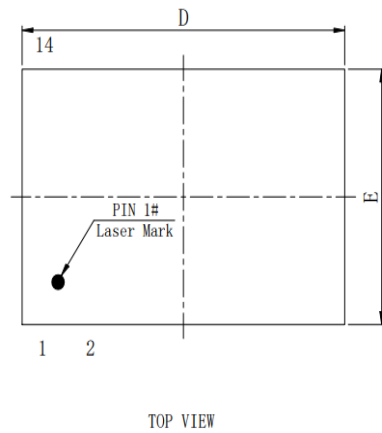
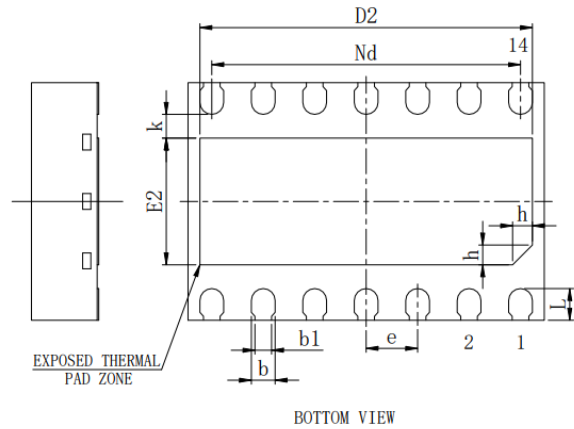
LAND PATTERN EXAMPLE (Unit: mm)



DFN4.5x3-14 DIMENSIONS

PACKAGE SIZE

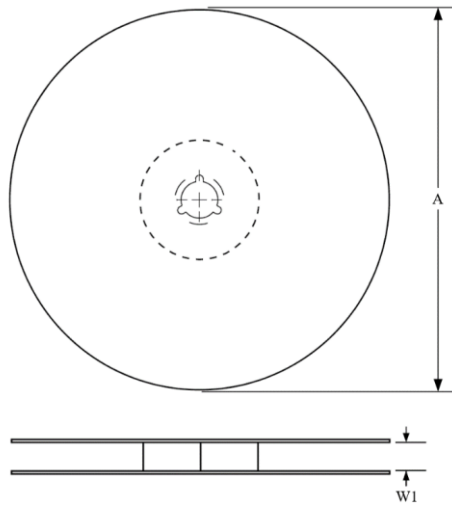
| SYMBOL | MILLIMETER | | |
|--------|------------|------|------|
| | MIN | NOM | MAX |
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.25 | 0.30 | 0.35 |
| b1 | 0.21REF | | |
| c | 0.203REF | | |
| D | 4.40 | 4.50 | 4.60 |
| D2 | 4.10 | 4.20 | 4.30 |
| e | 0.65BSC | | |
| Nd | 3.90BSC | | |
| E | 2.90 | 3.00 | 3.10 |
| E2 | 1.50 | 1.60 | 1.70 |
| L | 0.35 | 0.40 | 0.45 |
| h | 0.20 | 0.25 | 0.30 |
| K | 0.30REF | | |



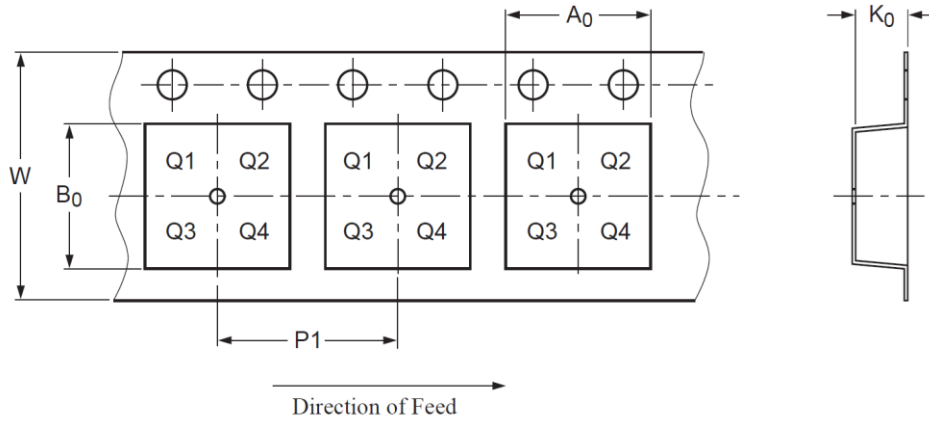
LAND PATTERN EXAMPLE (Unit: mm)



TAPE AND REEL INFORMATION



| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |



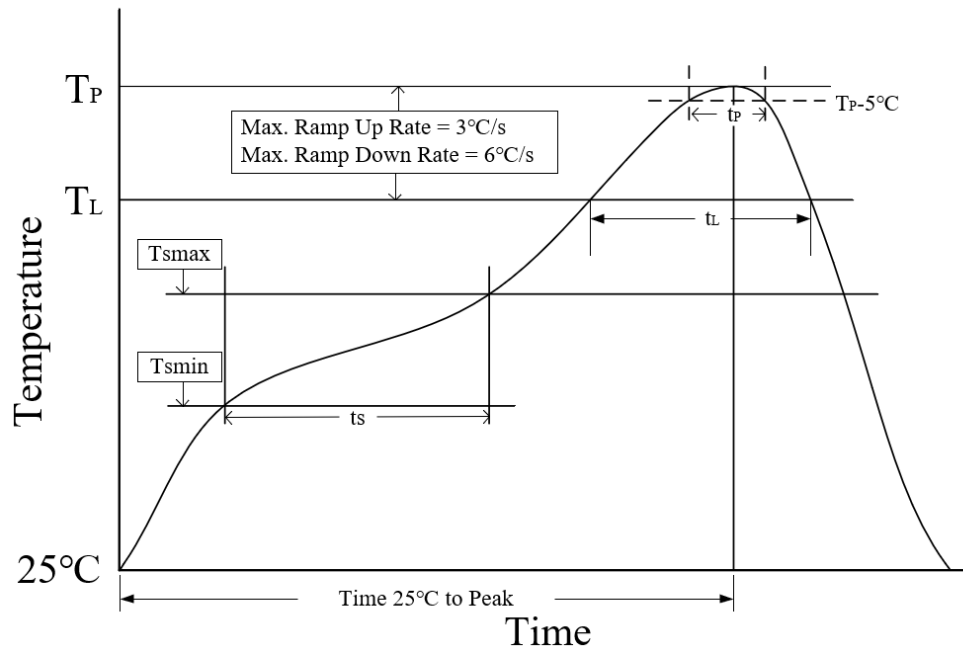
PIN1 is in quadrant 1

| Package Type | Reel Diameter A (mm) | Tape Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) |
|--------------|----------------------|--------------------|---------------------------------------|---------------------------------------|----------|----------|------------|
| SOP14 | 330±1 | 12.4 | 6.50 ^{+0.20} _{-0.1} | 9.30 ^{+0.20} _{-0.1} | 2.0±0.10 | 8.00±0.1 | 16.00±0.10 |
| DFN4.5×3-14 | 329±1 | 12.4 | 3.75±0.1 | 4.25±0.1 | 1.00±0.1 | 8.00±0.1 | 12.00±0.3 |

ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | MSL | PACKING |
|-------------|-------------|------|---------------|
| SIT1463QT | SOP14 | MSL3 | Tape and reel |
| SIT1463QTK | DFN4.5×3-14 | MSL1 | Tape and reel |

SOP14 is packed with 2500 pieces/disc in braided packaging; Leadless DFN4.5×3-14 is packed with 3000 pieces/disc in braided packaging.

REFLOW SOLDERING


| Parameter | Lead-free soldering conditions |
|---|--------------------------------|
| Ave ramp up rate (T_L to T_P) | 3 °C/second max |
| Preheat time t_s ($T_{smin}=150\text{ °C}$ to $T_{smax}=200\text{ °C}$) | 60-120 seconds |
| Melting time t_L ($T_L=217\text{ °C}$) | 60-150 seconds |
| Peak temp T_P | 260-265 °C |
| 5 °C below peak temperature t_p | 30 seconds |
| Ave cooling rate (T_P to T_L) | 6 °C/second max |
| Normal temperature 25°C to peak temperature T_P time | 8 minutes max |

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.



REVISION HISTORY

| Version number | Data sheet status | Revision date |
|----------------|---|---------------|
| V1.0 | Initial version | June 2024 |
| V1.1 | Added AEC-Q100 Grade 1 qualified; Added ESD ratings. | December 2024 |