FEATURES

- Compliant with ISO 11898-2:2016
- Supports CAN FD communication up to 5 Mbps
- Autonomous bus biasing function
- Very low supply current sleep/standby mode with bus remote wake-up capability
- Integrated BAT input regulator V1 for 5V/3.3V microcontroller supply, ±2% output voltage accuracy, current limiting >250mA, programmable undervoltage reset thresholds (60%/70%/80%/90%, 5V variants only)
- Integrated on-board 5V CAN supply (V2; SIT1169QTK, SIT1169QTK/F, SIT1169QTK/3 and SIT1169QTK/F/3 only), output voltage accuracy ±2%, current limiting >100mA
- Integrated off-board 5V sensor supply (VEXT; SIT1169QTK/X and SIT1169QTK/X/F only), ±2% output voltage accuracy, current limiting >100mA, short-circuit protected against BAT, GND and negative voltages (down to -18V)
- Overtemperature warning and shutdown
- BAT pin supports power-on and power-off detection
- Transmit data (TXD) dominant time-out function
- Mode control via the Serial Peripheral Interface (SPI)
- Multiple integrated fail-safe and reset functions (status registers accessible via SPI)
- Non-volatile memory (NVM) for user-customizable initialization
- Watchdog timer with Window, Timeout and Autonomous modes
- Integrated local wake-up via WAKE pin
- Selective wake-up support at 50 kbps, 100 kbps, 125 kbps, 250 kbps, 500 kbps, and 1 Mbps
- LIMP output pin with configurable activation threshold
- ±58V short-circuit protection on CANH/CANL pins
- Excellent Electromagnetic Immunity (EMI) performance
- Available in DFN20 package (with enhanced AOI capability)

DESCRIPTION

The SIT1169Q is a highly integrated System Basis Chip (SBC) that combines a high-speed CAN transceiver with power management functionality in a compact package. Fully compliant with ISO 11898-2:2016 and SAE J2284 standards, this device features an integrated voltage regulator capable of 250mA at 5V/3.3V for microcontroller power supply.

Key features include:

- Seven configurable operating modes (Normal, Standby, Sleep, Reset, Forced Normal, Overtemp, and Off)
- Ultra-low power consumption in standby and sleep modes
- Dual wake-up capability (CAN bus and local wake-up)
- Integrated watchdog timer and SPI interface
- Autonomous CAN bus biasing

The SIT1169Q is designed for reliable operation in automotive and industrial applications, offering robust performance while optimizing power efficiency. Its comprehensive feature set provides a solution for CAN-based systems requiring integrated power management and network connectivity.

PINNING INFORMATION

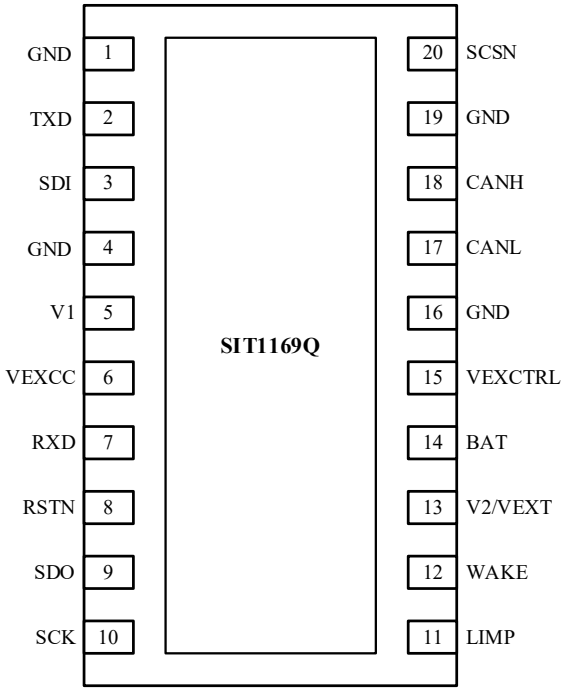


Figure 1 Pin configuration diagram

PIN DESCRIPTION

Pin	Symbol	Description
1	GND	Ground
2	TXD	Transmit data input
3	SDI	SPI data input
4	GND	Ground
5	V1	5V/3.3V microcontroller supply voltage
6	VEXCC	Current measurement for external PNP transistor; this pin is connected to the collector of the external PNP transistor
7	RXD	Receive data output; reflects data on bus lines and wake-up conditions
8	RSTN	Reset input/output; active-LOW
9	SDO	SPI data output
10	SCK	SPI clock input
11	LIMP	Limp home output, open-drain; active-LOW
12	WAKE	Local wake-up input
13	V2	5V CAN supply (SIT1169QTK, SIT1169QTK/3, SIT1169QTK/F and SIT1169QTK/F/3 only)
13	VEXT	5V sensor supply (SIT1169QTK/X and SIT1169QTK/X/F only)
14	BAT	Battery supply voltage
15	VEXCTRL	Control pin of the external PNP transistor; this pin is connected to the base of the external PNP transistor
16	GND	Ground
17	CANL	LOW-level CAN-bus line
18	CANH	HIGH-level CAN-bus line
19	GND	Ground
20	SCSN	SPI chip select input; active-LOW

Note: The metal pad on the back of the DFN20 package is recommended to be grounded.

LIMITING VALUES

Symbol	Parameter	Conditions	SPEC	Unit
V_X	Voltage on pin x	Pin V1, V2 (SIT1169QTK, SIT1169QTK/3, SIT1169QTK/F and SIT1169QTK/F/3)	-0.3 ~ +6	V
		Pins TXD, RXD, SDI, SDO, SCK, SCSN, RSTN	-0.3 ~ V_{V1}+0.3	V
		Pin VEXT (SIT1169QTK/X, SIT1169QTK/X/F)	-18~40	V
		Pin VEXCC	-0.3~6	V
		Pins WAKE	-18 ~ +40	V
		Pin LIMP, BAT, VEXCTRL	-0.3 ~ +40	V
		Pins CANH and CANL with respect to any other pin	-58 ~ +58	V
$I_{I(LIMP)}$	Input current on pin LIMP	LHC=1	0 ~ +20	mA
$V_{(CANH-CANL)}$	Voltage between pins CANH and CANL		-40 ~ +40	V
T_j	Virtual junction temperature		-40 ~ 150	℃
		when programming the MTPNV cells	0 ~ +125	℃
T_{stg}	Storage temperature		-55 ~ +150	℃

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

THERMAL CHARACTERISTICS

Symbol	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	DFN20	35	℃/W
$R_{\theta JC}$	Junction-to-case thermal resistance	DFN20	29	℃/W

BLOCK DIAGRAM

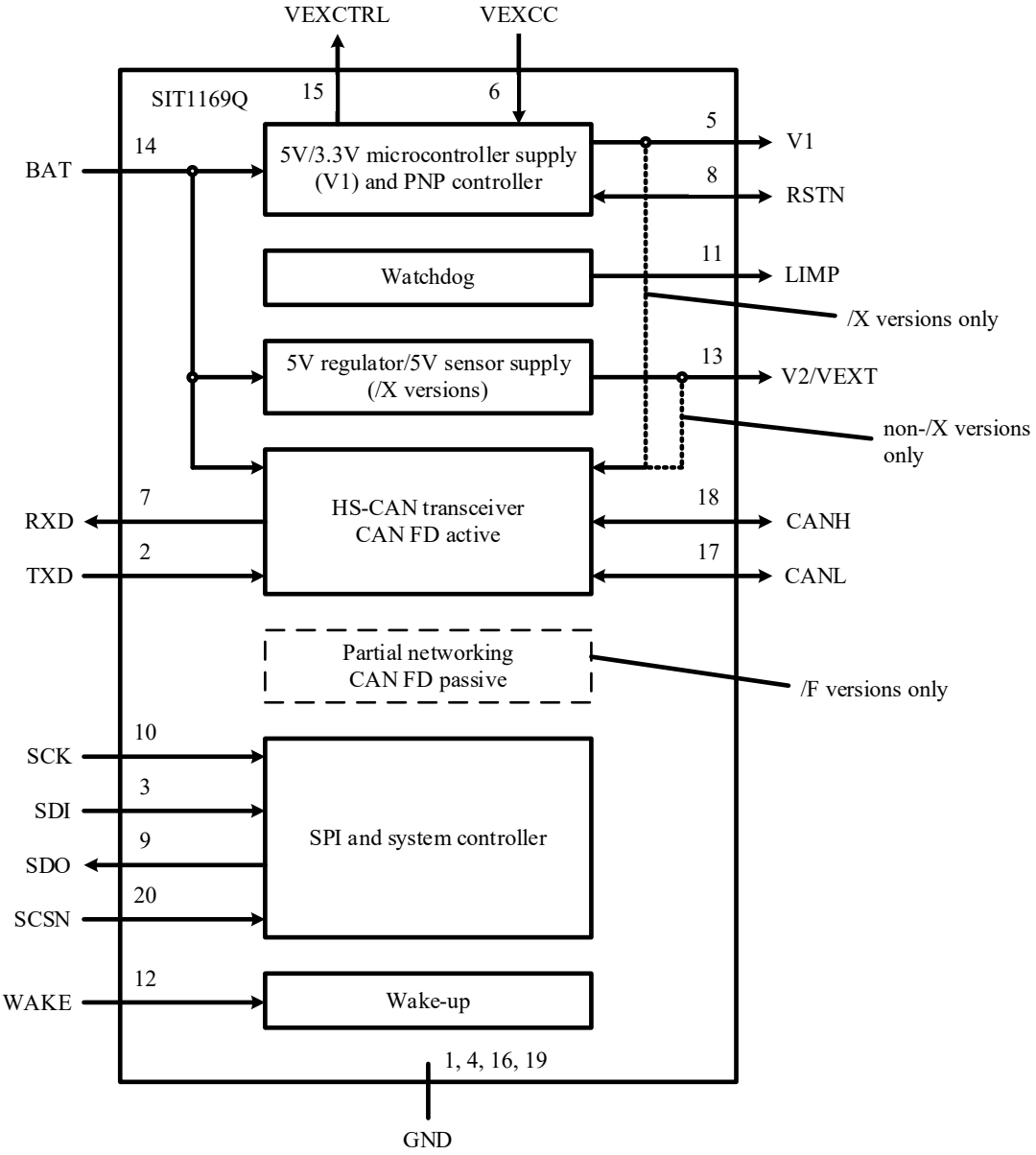


Figure 2 SIT1169Q Block diagram

FUNCTIONAL DESCRIPTION

1 System mode

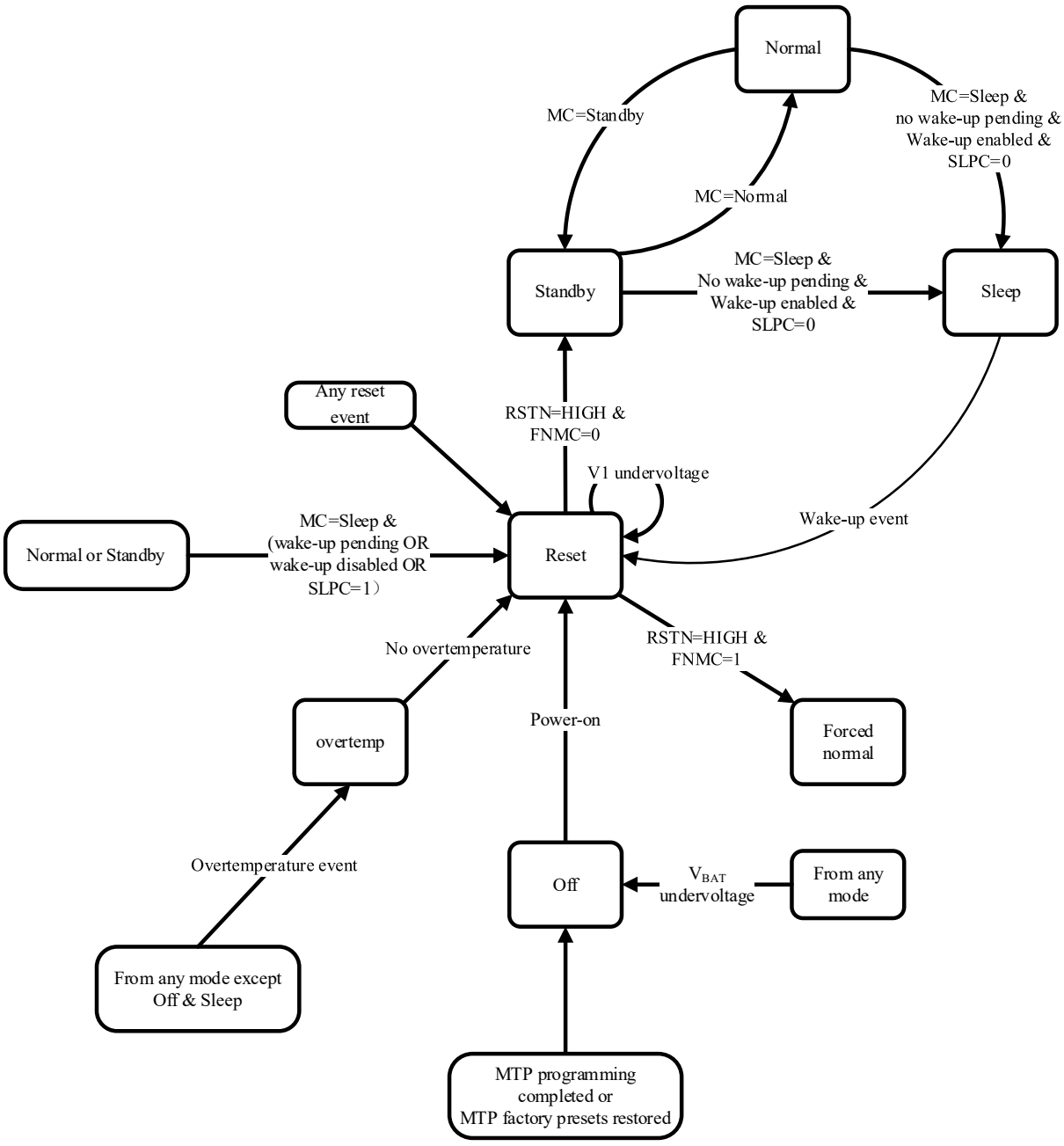


Figure 3 SIT1169Q system controller state diagram

1.1 Off mode

The SIT1169Q switches to Off mode when the battery is first connected, from any mode when $V_{BAT} < V_{th(det)poff}$, MTP programming completed or MTP factory presets restored. Only power-on detection is enabled; all other modules are inactive. The SIT1169Q starts to boot up when the battery voltage rises above the power-on

detection threshold $V_{th(det)pon}$ and switches to Reset mode after $t_{startup}$. In Off mode, the CAN pins disengage from the bus (zero load; high-ohmic).

1.2 Reset mode

Reset mode is the reset state of the SBC. In Reset mode, Pin RSTN is pulled down for a defined time to allow the microcontroller to start up in a controlled manner.

The SPI is inactive; the watchdog is disabled; V1 and overtemperature detection are active. The transceiver is unable to transmit or receive data in Reset mode. The behavior of V2/VEXT is determined by the settings of bits V2C/VEXTC and V2SUC/VEXTSUC.

The SIT1169Q switches to Reset mode from any mode in response to a reset event: (see Table 3):

- power-on（left Off mode）
- CAN wake-up in Sleep mode
- wake-up via WAKE pin in Sleep mode
- watchdog overflow in Sleep mode (Timeout mode)
- diagnostic wake-up in Sleep mode
- watchdog triggered too early (Window mode)
- watchdog overflow (Window mode or Timeout mode with WDF = 1)
- illegal watchdog mode control access
- RSTN pulled down externally
- exited Overtemp mode
- V1 undervoltage
- illegal Sleep mode command received
- wake-up from Sleep mode due to a frame detect error

If a V1 undervoltage event forced the transition to Reset mode, the SIT1169Q will remain in Reset mode until the voltage on pin V1 has recovered.

The SIT1169Q exits Reset mode:

- switches to Standby mode if pin RSTN is released HIGH
- switches to Forced Normal mode if bit FNMC = 1
- if the SBC is forced into Off or Overtemp mode

1.3 Overtemp mode

Overtemp mode is provided to prevent the SIT1169Q being damaged by excessive temperatures. The

SIT1169Q switches to Overtemp mode from any mode except Off mode or Sleep mode when the global chip temperature rises above the overtemperature protection activation threshold $T_{th(act)otp}$.

To help prevent the loss of data due to overheating, the SIT1169Q issues a warning when the IC temperature rises above the overtemperature warning threshold $T_{th(warn)otp}$. When this happens, status bit OTWS is set and an overtemperature warning event is captured (OTW = 1), if enabled (OTWE = 1).

In Overtemp mode, the CAN transmitter and receiver are disabled and the CAN pins are in a high-ohmic state. No wake-up event will be detected, but a pending wake-up will still be signaled by a LOW level on pin RXD, which will persist after the overtemperature event has been cleared. when the SBC enters Overtemp mode, V1 is off, pin RSTN is driven LOW and V2/VEXT is off.

The SIT1169Q exits Overtemp mode:

- switches to Reset mode if the chip temperature falls below the overtemperature protection release threshold $T_{th(rel)otp}$
- if the device is forced to switch to Off mode ($V_{BAT} < V_{th(det)poff}$)

1.4 Force Normal mode

Forced Normal mode is SBC testing mode and is useful for initial prototyping and failure detection, as well as first flashing of the microcontroller. In Forced Normal mode, the watchdog is disabled, the low-drop voltage regulator V1 is active, the CAN transceiver is active.

Bit FNMC is factory preset to 1, the SIT1169Q initially boots up in Forced Normal mode. This allows a newly installed device to be run in Normal mode without a watchdog. So the microcontroller can be flashed via the CAN bus in the knowledge that a watchdog timer overflow will not trigger a system reset. The non-volatile memory is store bit FNMC (address 74h). So once bit FNMC is programmed to 0, the SBC will no longer boot up in Forced Normal mode, allowing the watchdog to be enabled (see Table 8).

Even in Forced Normal mode, a reset event will trigger a transition to Reset mode with normal Reset mode behavior except that the transmitter remains active if there is no V_{CAN} undervoltage. However, the SIT1169Q will return to Forced Normal mode instead of switching to Standby mode when it exits Reset mode.

The SIT1169Q exits Force Normal mode:

- switches to Overtemp mode if the chip temperature rises above the overtemperature protection activation threshold $T_{th(act)otp}$
- switches to Reset mode if RSTN pulled down externally, exited Overtemp mode or V1 undervoltage
- if the device is forced to switch to Off mode ($V_{BAT} < V_{th(det)poff}$)

In Forced Normal mode, only the Main status register, the Watchdog status register, the Identification register and registers stored in non-volatile memory can be read. The non-volatile memory area is fully accessible for writing as long as the SIT1169Q is in the factory preset state.

1.5 Standby mode

Standby mode is the first-level power-saving mode of the SIT1169Q, offering reduced current consumption. In Standby mode, the transceiver is unable to transmit or receive data, the V1 is still active and the SPI remains enabled; the watchdog is active in Timeout mode if enabled. The behavior of V2/VEXT is determined by the SPI setting.

If remote CAN wake-up is enabled (CWE = 1), the receiver monitors bus activity for a wake-up request. Pin RXD is forced LOW when any enabled wake-up event is detected. This can be either a regular wake-up or a diagnostic wake-up such as an overtemperature event. The bus pins are biased to GND (via $R_{i(cm)}$) when the bus is inactive for $t > t_{to(silence)}$ and at approximately 2.5 V when there is activity on the bus (autonomous biasing). CAN wake-up can occur via a standard wake-up pattern or via a selective wake-up frame (selective wake-up is enabled when CPNC = PNCOK = 1, otherwise standard wake-up is enabled; see Table 4).

The SIT1169Q switches to Standby mode via Reset mode:

- from Off mode if the battery voltage rises above the power-on detection threshold ($V_{th(det)pon}$)
- from Overtemp mode if the chip temperature falls below the overtemperature protection release threshold $T_{th(rel)otp}$
- from Sleep mode on the occurrence of a regular or diagnostic wake-up event Standby mode can also be selected from Normal mode via an SPI command (MC = 100).

1.6 Normal mode

Normal mode is the active operating mode. In Normal mode, all the hardware on the device is available and can be activated (see Table 1). Voltage regulator V1 is enabled to supply the microcontroller.

Depending on the SPI register settings, the watchdog may be running in Window or Timeout mode and the V2/VEXT output may be active. The CAN interface can be configured to be active and thus to support normal CAN communication.
Normal mode can be selected from Standby mode via an SPI command (MC=111).

1.7 Sleep mode

Sleep mode is the second-level power-saving mode of the SIT1169Q. The difference between Sleep and Standby modes is that V1 is off in Sleep mode and temperature protection is inactive. Any enabled regular wake-up via CAN or WAKE or any diagnostic wake-up event will cause the SIT1169Q to wake up from Sleep mode.

The behavior of V2/VEXT is determined by the SPI settings. The SPI is disabled. Autonomous bus biasing is active. In Sleep mode, watchdog behavior determined by WMC setting (address 00h) and SDMC (See Table 7), The SIT1169Q will switch to Sleep mode when Sleep mode can be selected from Normal or Standby mode via an SPI command (MC = 001), provided there are no pending wake-up events and at least one regular wake-up source is enabled. Any attempt to enter Sleep mode while one of these conditions has not been met will

cause the SIT1169Q to switch to Reset mode and set the reset source status bits (RSS = 10100, 'illegal Sleep mode command received'; see Table 6).

Since V1 is off in Sleep mode, the only way the SBC can exit Sleep mode is via a wake-up event. Sleep mode can be permanently disabled in applications where, for safety reasons, the supply voltage to the host controller must never be cut off.

Sleep mode can be permanently disabled in applications where, for safety reasons, the supply voltage to the host controller must never be cut off. Sleep mode is permanently disabled by setting the Sleep control bit SLPC set in the SBC configuration register to 1(see Table 8). This register is located in the non-volatile memory area of the device. When SLPC set, a Sleep mode SPI command (MC = 001) triggers an SPI failure event instead of a transition to Sleep mode.

Table 1 Hardware characterization by function block

Block	Operating mode						
	Off	**Force Normal**	**Standby**	**Normal**	**Sleep**	**Reset**	**Overtempt**
V1	Off (1)	On	On	On	Off	On	Off
VEXT/V2	Off	On	Determined by bits V2C/VEXTC and V2SUC/VEXTSUC	Determined by bits V2C/VEXTC and V2SUC/VEXTSUC	Determined by bits V2C/VEXTC and V2SUC/VEXTSUC	Determined by bits V2C/VEXTC and V2SUC/VEXTSUC	VEXT/V2 off
RSTN	LOW	HIGH	HIGH	HIGH	LOW	LOW	LOW
SPI	Disabled	Active (2)	Active	Active	Disabled	Disabled	Disabled
Watchdog	Off	Off	Determined by bit WMC (3)	Determined by bit WMC	Determined by bit WMC (3)	Off	Off
CAN	Off	Active	Offline	Active/Offline/Listen-only (determined by bit CMC)	Offline	Offline	Off
RXD	V1 level	CAN bit stream	V1 level/LOW if wake-up detected	CAN bit stream if CMC=01/10/11; otherwise, same as Standby/Sleep	V1 level/LOW if wake-up detected	V1 level/LOW if wake-up detected	V1 level/LOW if wake-up detected

(1) When the SBC switches from Reset, Standby or Normal mode to Off mode in the 5 V variants, V1 behaves as a current source during power down while VBAT is falling from Vth(det)pof down to 2 V (RAM retention feature; see Section 10.1).
(2) Limited register access: Main status register, Watchdog status register, Identification register and non-volatile memory only.
(3) Window mode is only active in Normal mode.

2 System mode control

The operating mode is selected via bits MC in the Mode control register. The Mode control register is accessed via SPI address 0x01.

Table 2 Mode control register (address 01h)

Bit	Symbol	Access	Value	Description
7:3	Reserved	R	-	
2:0	MC	R/W		Mode control:
			001	Sleep mode
			100	Standby mode
			111	Normal mode

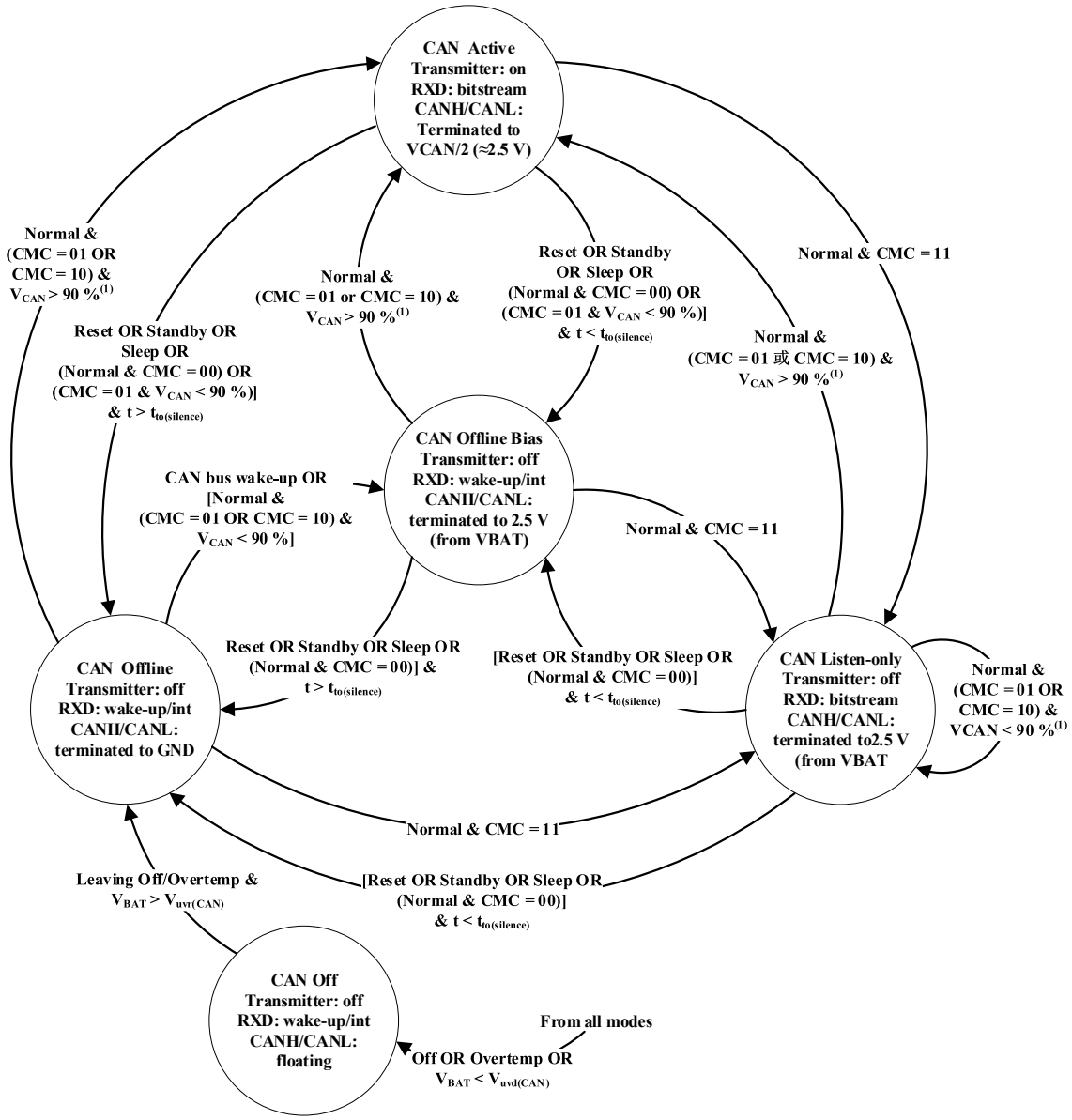
3 System mode state

In Main status register, the OTWS can be accessed to monitor the status of the overtemperature warning flag. The NMS to determine whether the SIT1169Q has entered Normal mode after initial power-up. The RSS also indicates the source of the most recent reset event.

Table 3 Main status registers (address 03h)

Bit	Symbol	Access	Value	Description
7	Reserved	R		
6	OTWS	R		Overtemperature warning status:
			0	IC temperature below overtemperature warning threshold
			1	IC temperature above overtemperature warning threshold
5	NMS	R		Normal mode status:
			0	SIT1169Q has entered Normal mode (after power-up)
			1	SIT1169Q has powered up but has not yet switched to Normal mode
4:0	RSS	R		Reset source status:
			00000	Left Off mode (power-on)
			00001	CAN wake-up in Sleep mode
			00100	Wake-up via WAKE pin in Sleep mode
			01100	Watchdog overflow in Sleep mode (Timeout mode)
			01101	Diagnostic wake-up in Sleep mode
			01110	Watchdog triggered too early (Window mode)
			01111	Watchdog overflow (Window mode or Timeout mode with WDF=1)
			10000	Illegal watchdog mode control access
			10001	RSTN pulled down externally
			10010	Left Overtemp mode
			10011	V1 undervoltage
			10100	Illegal Sleep mode command received
			10110	Wake-up from Sleep mode due to a frame detect error

4 CAN operating modes



(1) To prevent the bus lines being driven to a permanent dominant state, the transceiver will not switch to CAN Active mode or CAN Listen-only mode if pin TXD is held LOW (e.g. by a short-circuit to GND)

Figure 4 CAN transceiver state machine (with FNMC = 0)

The integrated CAN transceiver supports 5 operating modes: Off, Offline and Offline Bias, Listen-only, Active (see Figure 4). The CAN transceiver operating mode depends on the SIT1169Q operating mode and on the setting of bits CMC in the CAN control register (Table 4).

4.1 CAN Off mode

If one of the following conditions is met, the CAN transceiver will switch to CAN Off:

- V_{BAT} is lower than undervoltage detection threshold, $V_{uvd(CAN)}$ or
- The system mode is Off or Overtemp

If V_{BAT} rises above the undervoltage recovery threshold ($V_{uvr(CAN)}$), the CAN transceiver will switch to CAN Offline mode. The battery supply to the SBC is lost so that the CAN transceiver prevents reverse currents flowing from the bus in CAN Off mode.

4.2 CAN Offline and Offline Bias mode

In CAN offline mode, CANH and CANL are bias to GND, and the transceiver monitors wake-up events on the CAN bus, provided that CAN wake-up detection is enabled (CWE=1).

The CAN Offline Bias mode is the same as CAN Offline mode, but the CAN bus bias is 2.5V.

When the transceiver is in CAN Offline mode and activity is detected on the CAN bus, this is automatically activated. The transceiver will return to CAN Offline mode when the CAN bus is silent (no CAN bus edges) for longer than $t_{to(silence)}$.

There are four ways to CAN Offline mode or CAN Offline Bias mode:

- If one of the following conditions is met, the CAN transceiver switches to CAN Offline/Offline Bias mode from CAN Active mode:

  CMC = 01 and V_{CAN} drops lower than the 90 % undervoltage threshold or

  V1 drops lower than the V1 reset threshold.

- If one of the following conditions is met, the CAN transceiver will switch from CAN Offline mode to CAN Offline Bias mode:

  a standard wake-up pattern is detected on the CAN bus or

  the system mode is Normal, CMC = 01 or 10 and V_{CAN} < 90 %

- If one of the following conditions is met, the CAN transceiver switches to CAN Offline mode:

  the system mode is from Off or Overtemp mode to Reset mode or

  from CAN Offline Bias mode if no activity is detected on the bus (no CAN edges) for $t > t_{to(silence)}$

- If one of the following conditions is met, the CAN transceiver will switch from CAN Active mode or CAN Listen-only mode to CAN Offline mode:

  CAN transceiver is in Normal and CMC = 00 or

  the system mode is Reset or Standby or Sleep

The premise is that the CAN-bus has been inactive for at least $t_{to(silence)}$. The CAN transceiver will switch first to CAN Offline Bias mode and then to CAN Offline mode once the bus has been silent for $t_{to(silence)}$ when the CAN-bus has been inactive for less than $t_{to(silence)}$.

4.3 CAN Listen-only mode

CAN Listen-only mode allows the SIT1169Q to monitor bus activity while the transceiver is inactive, without

influencing bus levels. This facility could be used by development tools that need to listen to the bus but do not need to transmit or receive data or for software-driven selective wake-up. Dedicated microcontrollers could be used for selective wake-up, providing an embedded low-power CAN engine designed to monitor the bus for potential wake-up events.

In Listen-only mode the CAN transmitter is disabled, reducing current consumption. The CAN receiver and CAN biasing remain active. This enables the host microcontroller to switch to a low-power mode in which an embedded CAN protocol controller remains active, waiting for a signal to wake up the microcontroller.

The CAN transceiver is in Listen-only mode when:

- the system mode is in Normal mode and CMC = 11
- the CAN transceiver will not leave Listen-only mode while TXD is LOW or CAN Active mode is selected with CMC = 01 while the voltage on V_{CAN} is below the 90 % undervoltage threshold.

4.4 CAN Active mode

In CAN Active mode, the transceiver can transmit and receive data via CANH and CANL. The differential receiver converts the analog data on the bus lines into digital data, which is output on pin RXD. The transmitter converts digital data generated by the CAN controller (input on pin TXD) into analog signals suitable for transmission over the CANH and CANL bus lines. CAN Active mode is selected when MC = 111 and CMC = 01 or 10. When CMC = 01, V_{CAN} undervoltage detection is enabled and the transceiver will go to CAN Offline or CAN Offline Bias mode when the voltage on V_{CAN} drops below the 90 % threshold. When CMC = 10, V_{CAN} undervoltage detection is disabled. The transmitter will remain active until the voltage on V1 drops below the V1 reset threshold (selected via bits V1RTC). The SBC will then switch to Reset mode and the transceiver will switch to CAN Offline or CAN Offline Bias mode.

The CAN transceiver is in Active mode when:

- the system mode is in Normal mode (MC = 111) and the CAN transceiver has been enabled by setting bits CMC in the CAN control register to 01 or 10

  if CMC = 01, the voltage on pin V_{CAN} is above the 90 % undervoltage threshold

  if CMC = 10, the voltage on pin V1 is above the V1 reset threshold

If pin TXD is held LOW when CAN Active mode is selected via bits CMC, the transceiver will not enter CAN Active mode but will switch to or remain in CAN Listen-only mode. It will remain in Listen-only mode until pin TXD goes HIGH in order to prevent a hardware and/or software application failure from driving the bus lines to an unwanted dominant state.

In CAN Active mode, the CAN bias voltage is the CAN supply voltage divided by two (depending on the derivative, the bias voltage is either V1 divided by two or V2 divided by two).

The application can determine whether the CAN transceiver is ready to transmit/receive data or is disabled by reading the CAN Transceiver Status (CTS) bit in the Transceiver Status Register (see Table 5).

5 CAN mode control

When the SIT1169Q is in Normal mode, the CAN transceiver operating mode (Active, Listen-only or Offline) can be selected via bits CMC in the CAN control register. When the SIT1169Q is in Standby or Sleep modes, the transceiver is forced to Offline or Offline Bias mode (depending on bus activity).

Table 4 CAN control register (address 20h)

Bit	Symbol	Access	Value	Description
7	Reserved	R	-	
6	CFDC (1)	R/W		CAN FD control:
			0	CAN FD tolerance disabled
			1	CAN FD tolerance enabled
5	PNCOK (1)	R/W		CAN partial networking configuration OK:
			0	Partial networking register configuration invalid (wake-up via standard wake-up pattern only)
			1	Partial networking registers configured successfully
4	CPNC (1)	R/W		CAN partial networking control:
			0	Disable CAN selective wake-up
			1	Enable CAN selective wake-up
3:2	Reserved	R	-	
1:0	CMC	R/W		CAN transceiver operating mode selection (available when STI1169Q is in Normal mode; MC=111)
			00	Offline mode
			01	Active mode; see Section 4.4 (V_{CAN} undervoltage detection is enabled)
			10	Active mode; see Section 4.4 (V_{CAN} undervoltage detection is disabled)
			11	Listen-only mode

(1) SIT1169QTK/F and SIT1169QTK/X/F only.

6 Transceiver status

Table 5 Transceiver status register (address 22h)

Bit	Symbol	Access	Value	Description
7	CTS	R		CAN transceiver status:
			0	CAN transceiver not in Active mode
			1	CAN transceiver in Active mode
6	CPNERR (1)	R		CAN partial networking error:
			0	no CAN partial networking error detected (PNFDE=0 AND PNCOK=1)

Bit	Symbol	Access	Value	Description
			1	CAN partial networking error detected (PNFDE=1 OR PNCOK=0; wake-up via standard wake-up pattern only)
5	CPNS (1)	R		CAN partial networking status:
			0	CAN partial networking configuration error detected (PNCOK=0)
			1	CAN partial networking configuration ok (PNCOK=1)
4	COSCS (1)	R		CAN oscillator status:
			0	CAN partial networking oscillator not running at target frequency
			1	CAN partial networking oscillator running at target frequency
3	CBSS	R		CAN bus silence status:
			0	CAN bus active (communication detected on bus)
			-	CAN bus inactive (for longer than $t_{to(silence)}$)
2	Reserved	R	-	
1	VCS (2)	R		V_{CAN} status:
			0	CAN supply voltage is above the undervoltage threshold, $V_{uvd(CAN)}$
			1	CAN supply voltage is below the undervoltage threshold, $V_{uvd(CAN)}$
0	CFS	R		CAN failure status:
			0	no TXD dominant time-out event detected
			1	CAN transmitter disabled due to a TXD dominant time-out event

(1) SIT1169QTK/F and SIT1169QTK/X/F only.

(2) Only active when CMC = 01.

7 Watchdog

The SIT1169Q contains a watchdog that supports three operating modes: Window, Timeout and Autonomous. Eight watchdog periods are supported, from 8ms to 4096ms. The watchdog period is programmed via bits NWP. The selected period is valid for both Window and Timeout modes. The default watchdog period is 128ms. A watchdog trigger event resets the watchdog timer. A watchdog trigger event is any valid write access to the Watchdog control register. If the watchdog mode or the watchdog period have changed as a result of the write access, the new values are immediately valid.

The watchdog mode is selected via bits WMC in the Watchdog control register (see Table 7).

The SBC must be in Standby mode when the watchdog mode or period is changed. If Window mode is selected

(WMC = 100), the watchdog will remain or switch Timeout mode until the SBC enters Normal mode.

Any attempt to change the watchdog operating mode or period (via WMC or NWP) while the SBC is in Normal mode will cause the SIT1169Q to switch to Reset mode. The reset source status bits (RSS = 10000, 'illegal watchdog mode control access' see Table 6) and a SPI failure (SPIF) event triggered, if enabled (SPIFE).

In Window mode when available only in SBC Normal mode, the watchdog can only be triggered during the second half of the watchdog period.

In Timeout mode, the watchdog runs continuously and can be reset at any time within the timeout time by a watchdog trigger. Watchdog timeout mode can also be used for cyclic wake-up of the microcontroller.

In Autonomous mode, the watchdog can be off or in Timeout mode.

Table 6 Watchdog configuration

Operating/watchdog mode						
FNMC (Forced Normal mode control)		0	0	0	0	1
SDMC (Software Development mode control)		x	x	0	1	x
WMC (watchdog mode control)		100 (Window)	010 (Timeout)	001 (Autonomous)	001 (Autonomous)	n.a.
SBC operating mode	Normal mode	Window	Timeout	Timeout	Off	Off
	Standby mode (RXD HIGH) (1)	Timeout	Timeout	Off	Off	Off
	Standby mode (RXD LOW) (1)	Timeout	Timeout	Timeout	Off	Off
	Sleep mode	Timeout	Timeout	Off	Off	Off
	Other modes	Off	Off	Off	Off	Off

(1) RXD LOW signals a pending wake-up.

Table 7 Watchdog control register (address 00h)

Bit	Symbol	Access	Value	Description
7:5	WMC	R/W		Watchdog mode control:
			001 (1)	Autonomous mode
			010 (2)	Timeout mode
			100 (3)	Window mode
4	Reserved	R	-	
3:0	NWP	R/W		Nominal watchdog period:
			1000	8ms
			0001	16ms
			0010	32ms

Bit	Symbol	Access	Value	Description
			1011	64ms
			0100(2)	128ms
			1101	256ms
			1110	1024ms
			0111	4096ms

(1) Default value if SDMC = 1.

(2) Default value.

(3) Selected in Standby mode but only activated when the SBC switches to Normal mode.

Two operating modes have a major impact on the operation of watchdog: Forced Normal mode and Software Development mode (Software Development mode is provided for test and development purposes only and is not a dedicated SBC operating mode; the SIT1169Q can be in any functional operating mode with Software Development mode enabled; see Section 7.2.2). These modes are enabled and disabled via bits FNMC and SDMC respectively in the non-volatile memory area. The watchdog is disabled in Forced Normal mode (FNM). In Software Development mode (SDM), the watchdog can be disabled or activated for test and software debugging purposes.

Table 8 SBC configuration control register (address 74h)

Bit	Symbol	Access	Value	Description
7:6	Reserved	R	-	
5:4	V1RTSUC (1)	R/W		V1 reset threshold (defined by bit V1RTC) at start-up:
			00 (2)	V1 undervoltage detection at 90% of nominal value at start-up (V1RTC=00)
			01	V1 undervoltage detection at 80% of nominal value at start-up (V1RTC=01)
			10	V1 undervoltage detection at 70% of nominal value at start-up (V1RTC=10)
			11	V1 undervoltage detection at 60% of nominal value at start-up (V1RTC=11)
3	FNMC (3)	R/W	-	Forced Normal mode control:
			0	Forced Normal mode disabled
			1 (2)	Forced Normal mode enabled
2	SDMC	R/W		Software Development mode control:
			0 (2)	Software Development mode disabled
			1	Software Development mode enabled
1	Reserved	R	-	
0	SLPC	R/W		Sleep mode:

Bit	Symbol	Access	Value	Description
			0 (2)	Sleep mode commands accepted
			1	Sleep mode commands ignored

(1) The V1 undervoltage threshold is fixed at 90 % in the SIT1169QTK/3 and SIT1169QTK/F/3, regardless of the setting of bit V1RTSUC.

(2) Factory preset value.

(3) FNMC settings overrule SDMC.

Information on the status of the watchdog is available from the Watchdog status register (Table 9). This register also indicates whether Forced Normal and Software Development modes are active.

Table 9 Watchdog status register (address 05h)

Bit	Symbol	Access	Value	Description
7:4	Reserved	R	-	
3	FNMS	R		Forced Normal mode status:
			0	SBC is not in Forced Normal mode
			1	SBC is in Forced Normal mode
2	SDMS	R		Software Development mode status:
			0	SBC is not in Software Development mode
			1	SBC is in Software Development mode
1:0	WDS	R		Watchdog status:
			00	Watchdog is off
			01	Watchdog is in first half of the nominal period
			10	Watchdog is in second half of the nominal period
			11	Reserved

7.1 Software Development mode

Software Development mode is provided to simplify the software design process. When Software Development mode is enabled, the watchdog starts up in Autonomous mode (WMC=001) and is inactive after a system reset, overriding the default value (see Table 7). The watchdog is always off in Autonomous mode if Software Development mode is enabled (SDMC=1; see Table 6).

Software can be run without a watchdog in Software Development mode. However, it is possible to activate and deactivate the watchdog for test purposes by selecting Window or Timeout mode via bits WMC while the SBC is in Standby mode (note that Window mode will only be activated when the SBC switches to Normal mode). Software Development mode is activated via bits SDMC in non-volatile memory (see Table 8).

7.2 Window mode

The watchdog runs continuously in Window mode. The watchdog will be in Window mode if WMC = 100 and the SIT1169Q is in Normal mode. In Window mode, the watchdog can only be triggered during the second

half of the watchdog period.

If the watchdog overflows, or is triggered in the first half of the watchdog period (before $t_{trig(wd)1}$), a system reset is performed. After the system reset, the reset source (either 'watchdog triggered too early' or 'watchdog overflow') can be read via the reset source status bits (RSS) in the Main Status register.

If the watchdog is triggered in the second half of the watchdog period (after $t_{trig(wd)1}$ but before $t_{trig(wd)2}$), the watchdog timer is restarted.

7.3 Timeout mode

The watchdog runs continuously in Timeout mode. The watchdog will be in Timeout mode if WMC=010 and the SIT1169Q is in Normal, Standby or Sleep mode. The watchdog will also be in Timeout mode if WMC=100 and the SIT1169Q is in Standby or Sleep mode. If Autonomous mode is selected (WMC=001), the watchdog will be in Timeout mode if one of the conditions for Timeout mode has been satisfied (see Table 10).

In Timeout mode, the watchdog timer can be reset at any time by a watchdog trigger. If the watchdog overflows, a watchdog failure event (WDF) is captured. If a WDF is already pending when the watchdog overflows, a system reset is performed. In Timeout mode, the watchdog can be used as a cyclic wake-up source for the microcontroller when the SIT1169Q is in Standby or Sleep mode. In Sleep mode, a watchdog overflow generates a wake-up event.

When the SBC is in Sleep mode with watchdog Timeout mode selected, a wake-up event s generated after the nominal watchdog period (NWP). If bit WDF is set, RXD is forced LOW and V1 is turned on. The application software can then clear the WDF bit and trigger the watchdog before it overflows.

7.4 Autonomous mode

Autonomous mode is selected when WMC=001. When Autonomous mode is selected, the watchdog will be in Timeout mode if the SBC is in Normal mode or Standby mode with RXD LOW, provided Software Development mode has been disabled (SDMC=0). Otherwise, the watchdog will be off.

In Autonomous mode, the watchdog will not be running when the SBC is in Standby (RXD HIGH) or Sleep mode. If a wake-up event is captured, pin RXD is forced LOW to signal the event and the watchdog is automatically restarted in Timeout mode. If the SBC was in Sleep mode when the wake-up event was captured, it switches to Standby mode.

Table 10 Watchdog status in Autonomous mode

SIT1169Q operating mode	Watchdog status	
	SDMC=0	SDMC=1
Normal mode	Timeout mode	Off
Standby: RXD HIGH	Off	Off
Sleep	Off	Off
Any other mode	Off	Off
Standby: RXD LOW	Timeout mode	Off

8 System reset

When a system reset occurs, the SBC switches to Reset mode and initiates a process that generates a low-level pulse on pin RSTN. The SIT1169Q can distinguish up to 13 different reset sources, as detailed in Table 3.

8.1 Characteristics of pin RSTN

Pin RSTN is a bidirectional open drain low side driver with integrated pull-up resistance, as shown in Figure 5. The input reset pulse width must be at least tw(rst) to guarantee that external reset events are detected correctly. With this configuration, the SBC can detect the pin being pulled down externally, e.g. by the microcontroller.

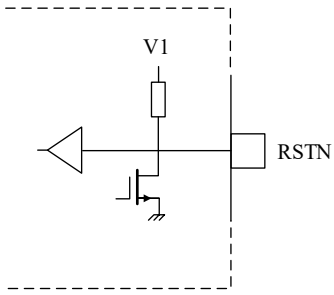


Figure 5 RSTN internal pin configuration

8.2 Selecting the output reset pulse width

The duration of the output reset pulse is selected via bits RLC in the Start-up control register (Table 11). The SBC distinguishes between a cold start and a warm start. A cold start is performed if the reset event was combined with a V1 undervoltage event (power-on reset, reset during Sleep mode, over-temperature reset, V1 undervoltage before entering or while in Reset mode). The output reset pulse width for a cold start is

determined by the setting of bits RLC.

If any other reset event occurs without a V1 undervoltage (external reset, watchdog failure, watchdog change attempt in Normal mode, illegal Sleep mode command) the SBC uses the shortest reset length ($t_{w(rst)}$ = 1 ms to 1.5 ms). This is called a warm start of the microcontroller.

Table 11 Start-up control register (address: 73h)

Bit	Symbol	Access	Value	Description
7:6	Reserved	R	-	
5:4	RLC	R/W		RSTN output reset pulse width:
			00(1)	$t_{w(rst)}$=20ms to 25ms
			01	$t_{w(rst)}$=10ms to 12.5ms
			10	$t_{w(rst)}$=3.6ms to 5ms
			11	$t_{w(rst)}$=1ms to 1.5ms
3	V2SUC (2) VEXTSUC (3)	R/W		V2/VEXT start-up control:
			0(1)	Bits V2C/VEXTC set to 00 at power-up

Bit	Symbol	Access	Value	Description
			1	Bits V2C/VEXTC set to 11 at power-up
2:0	Reserved	R	-	

(1) Factory preset value.

(2) SIT1169QTK, SIT1169QTK/3, SIT1169QTK/F and SIT1169QTK/F/3 only.

(3) SIT1169QTK/X and SIT1169QTK/X/F only.

8.3 Reset sources

The following events will cause the SIT1169Q to switch to Reset mode:

- V_{V1} drops below the selected V1 undervoltage threshold defined by bits V1RTC (except in Sleep mode or Overtemp mode)
- via Off mode after an MTPNV programming cycle has been completed
- pin RSTN is pulled down externally
- the watchdog overflows in Window mode
- the watchdog is triggered too early in Window mode (before $t_{trig(wd)1}$)
- the watchdog overflows in Timeout mode with WDF = 1 (watchdog failure pending)
- an attempt is made to reconfigure the Watchdog control register while the SBC is in Normal mode
- the SBC leaves Off mode
- local or CAN bus wake-up in Sleep mode
- diagnostic wake-up in Sleep mode
- the SBC leaves Overtemp mode
- illegal Sleep mode command received
- wake-up from Sleep mode due to a frame detect error

9 Global temperature protection

The temperature of the SIT1169Q is monitored continuously, except in Sleep and Off modes. The SBC switches to Overtemp mode if the temperature exceeds the overtemperature protection activation threshold, $T_{th(act)otp}$. In addition, pin RSTN is driven LOW and V1, V2/VEXT and the CAN transceiver are switched off. When the temperature drops below the overtemperature protection release threshold, $T_{th(rel)otp}$, the SBC switches to Standby mode via Reset mode.

In addition, the SIT1169Q provides an overtemperature warning. When the IC temperature rises about the overtemperature warning threshold ($T_{th(warn)otp}$), status bit OTWS is set and an overtemperature warning event is captured (OTW = 1) if overtemperature warning enable (OTWE = 1).

10 Power supplies

10.1 Battery supply voltage (VBAT)

The internal circuitry is supplied from the battery via pin BAT. The device needs to be protected against negative supply voltages, e.g. by using an external series diode. If VBAT falls below the power-off detection threshold, $V_{th(det)poff}$, the SBC switches to Off mode. However, the microcontroller supply voltage (V1) remains active until VBAT falls below 2 V. The SBC switches from Off mode to Reset mode $t_{startup}$ after the battery voltage rises above the power-on detection threshold, $V_{th(det)pon}$. Power-on event status bit PO is set to 1 to indicate the SIT1169Q has powered up and left Off mode (see Table 24).

10.2 Voltage regulator V1

The SIT1169Q provides a 5 V or 3.3 V supply (V1), depending on the variant. V1 can deliver up to 250 mA load current. In the SIT1169QTK/X and SIT1169QTK/X/F variants, the CAN transceiver is supplied internally via V1, reducing the output current available for external components. When V1 is turned off, the voltage of V1(CAN transceiver supply) will drop rapidly to GND through the internal pull-down circuits.

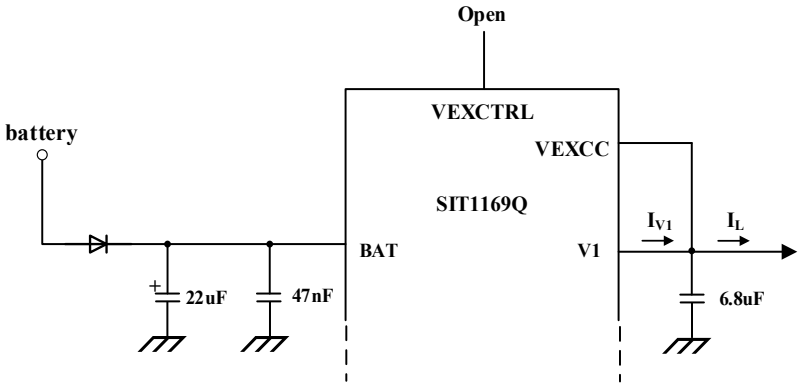


Figure 6 typical application without external PNP (showing example component values)

To prevent the device overheating at high ambient temperatures or high average currents, an external PNP transistor can be connected as illustrated in Figure 8. In this configuration, the power dissipation is distributed between the SBC (I_{V1}) and the PNP transistor (I_{PNP}).

The PNP transistor is activated when the load current reaches the PNP activation threshold, $I_{th(act)PNP}$. Bit PDC in the Regulator control register (Table 12) is used to regulate how power dissipation is distributed.

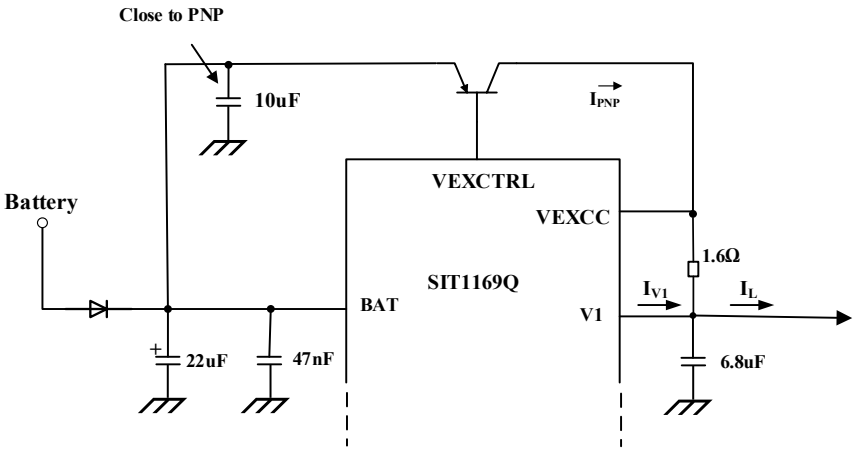


Figure 7 Typical application with external PNP (showing example component values)

For short-circuit protection, a resistor must be connected between pins V1 and VEXCC to allow the current to be monitored. This resistor limits the current delivered by the external transistor. If the voltage difference between pins VEXCC and V1 reaches $V_{th(act)Ilim}$, the PNP current limiting activation threshold voltage, the transistor current will not increase further. In general, any PNP transistor with a current amplification factor (β) of between 50 and 500 can be used. The output voltage on V1 is monitored. A system reset is generated if the voltage on V1 drops below the selected undervoltage threshold (60 %, 70 %, 80 % or 90 % of the nominal V1 output voltage for the 5 V variants, selected via V1RTC in the Regulator control register; fixed at 90 % for the 3.3 V variants; see Table 12).

The default value of the undervoltage threshold at power-up is determined by the value of bits V1RTSUC in the SBC configuration control register (Table 8). The SBC configuration control register is in non-volatile memory, allowing the user to define the undervoltage threshold (V1RTC) at start-up.

In addition, an undervoltage warning (a V1U event) is generated if the voltage on V1 falls below 90 % of the nominal value (and V1U event detection is enabled, V1UE=1; see Table 29). This information can be used as a warning, when the 60 %, 70 % or 80 % threshold is selected, to indicate that the level on V1 is outside the nominal supply range. The status of V1, whether it is above or below the 90 % undervoltage threshold, can be read via bit V1S in the Supply voltage status register (Table 13).

10.3 Voltage regulator V2

In the SIT1169QTK, SIT1169QTK/3, SIT1169QTK/F and SIT1169QTK/F/3, pin 13 is a voltage regulator output (V2) delivering up to 100 mA.

The CAN transceiver is supplied internally from V2, consuming a portion of the available current. V2 is not protected against shorts to the battery or to negative voltages and should not be used to supply off-board components. V2 is software controlled and must be turned on (via bit V2C in the Regulator control register; see Table 12) to activate the supply voltage for the internal CAN transceiver. V2 is not required for wake-up detection via the CAN interface. When V2 is turned off, the voltage of V2(CAN transceiver supply) will drop rapidly to gnd through the internal pull-down circuits.

The default value of V2C at power-on is defined by bits V2SUC in non-volatile memory. The status of V2 can be polled from the Supply voltage status register (Table 13).

10.4 Voltage regulator VEXT

In the SIT1169QTK/X and SIT1169QTK/X/F, pin 13 is a voltage regulator output (VEXT) that can be used to supply off-board components, delivering up to 100 mA. VEXT is protected against short-circuits to the battery and negative voltages. Since the CAN controller is supplied internally via V1, the full 100 mA supply current is available for off-board loads connected to VEXT (provided the thermal limits of the PCB are not exceeded).

VEXT is software controlled and must be turned on (via bit VEXTC in the Regulator control register; see Table 12) to activate the supply voltage for off-board components. The default value of VEXTC at power-on is defined by bits VEXTSUC in non-volatile memory. The status of VEXT can be read from the Supply voltage status register (Table 13).

Table 12 Regulator control register (address 10h)

Bit	Symbol	Access	Value	Description
7	Reserved	R	-	
6	PDC	R/W		Power distribution control:
			0	V1 threshold current for activating the external PNP transistor, load current rising; $I_{th(act)PNP}$ (higher value) V1 threshold current for deactivating the external PNP transistor, load current falling; $I_{th(act)PNP}$ (higher value)
			1	V1 threshold current for activating the external PNP transistor; load current rising; $I_{th(act)PNP}$ (lower value) V1 threshold current for deactivating the external PNP transistor; load current falling; $I_{th(act)PNP}$ (lower value)
5:4	Reserved	R	-	
3:2	V2C (1) VEXTC (2)	R/W		V2C/VEXTC configuration:
			00	V2/VEXT off in all modes
			01	V2/VEXT on in Normal mode
			10	V2/VEXT on in Normal, Standby and Reset modes
			11	V2/VEXT on in Normal, Standby, Sleep and Reset modes
1:0	V1RTC (3)	R/W		Set V1 reset threshold:
			00	Reset threshold set to 90% of V1 nominal output voltage
			01	Reset threshold set to 80% of V1 nominal output voltage
			10	Reset threshold set to 70% of V1 nominal output voltage
			11	Reset threshold set to 60% of V1 nominal output voltage

(1) SIT1169QTK, SIT1169QTK/3, SIT1169QTK/F and SIT1169QTK/F/3: default value at power-up defined by V2SUC bit setting (see Table 11).

(2) SIT1169QTK/X and SIT1169QTK/X/F: default value at power-up defined by VEXTSUC bit setting (see Table 11).

(3) 5 V variants only; default value at power-up defined by setting of bits V1RTSUC (see Table 8). The threshold is fixed at 90 % in the 3.3 V variants and V1RTC always reads 00 (regardless of the value written to V1RTC or the start-up threshold defined by V1RTSUC).

Table 13 Supply voltage status register (address 1Bh)

Bit	Symbol	Access	Value	Description
7:3	Reserved	R	-	
2:1	V2S (1) VEXTS (2)	R		V2/VEXT status:
			00 (3)	V2/VEXT voltage ok
			01	V2/VEXT output voltage below undervoltage threshold
			10	V2/VEXT output voltage above overvoltage threshold
			11	V2/VEXT disabled
0	V1S	R		V1 status:
			0 (3)	V1 output voltage above 90% undervoltage threshold
			1	V1 output voltage below 90% undervoltage threshold

(1) SIT1169QTK, SIT1169QTK/3, SIT1169QTK/F and SIT1169QTK/F/3 only.

(2) SIT1169QTK/X and SIT1169QTK/X/F only.

(3) Default value at power-up

10.5 LIMP output

The dedicated LIMP pin can be used to enable so called ‘limp home’ hardware in the event of a serious ECU failure. Detectable failure conditions include SBC overtemperature events, loss of watchdog service, short-circuits on pins RSTN or V1 and user-initiated or external reset events (see Figure 8). The LIMP pin is a battery-robust, active-LOW, open-drain output. The LIMP pin can also be forced LOW by setting bit LHC in the Fail-safe control register (Table 14).

10.5.1 Reset counter

The SIT1169Q uses a reset counter to detect serious failures. The reset counter is incremented (bits RCC=RCC+1; see Table 14) every time the SBC enters Reset mode. When the system is running correctly, it is expected that the system software will reset this counter (RCC = 00) periodically to ensure that routinely expected reset events do not cause it to overflow.

If RCC is equal to 3 when the SBC enters Reset mode, the SBC assumes that a serious failure has occurred and sets the limp-home control bit, LHC. This action forces the external LIMP pin LOW with RCC overflowing to RCC = 0. Bit LHC can also be set via the SPI interface. The LIMP pin is set floating again if LHC is reset to 0 through software control or at power-up when the SBC leaves Off mode. The application software can preset the counter value to define how many reset events are tolerated before the limp-home function is activated. If RCC is initialized to 3, for example, the next reset event will immediately trigger the

limp-home function. The default counter setting at power-up is RCC = 00. Besides a reset counter (RCC) overflow, the following events cause bit LHC to be set and immediately trigger the limp-home function:

• overtemperature lasting longer than $t_{d(limp)}$

• SBC remaining in Reset mode for longer than $t_{d(limp)}$ (e.g. because of a clamped RSTN pin or a permanent V1 undervoltage).

10.5.2 LIMP state diagram

Note that the SBC always switches to Reset mode after leaving Sleep mode, since the SBC powers up V1 in response to a wake-up event. So RCC is incremented after each Sleep mode cycle. The application software needs to monitor RCC and update the value as necessary to ensure that multiple Sleep mode cycles do not cause the reset counter to overflow.

The limp-home function and the reset counter are disabled in Forced Normal mode. The LIMP pin is floating, RCC remains unchanged and bit LHC=0.

SBC modes are derived from the SBC state diagram (see Figure 3). The reset counter overflows from 3 to 0; t is the time the SBC remains continuously in Reset or Overtemp mode; time t is reset at mode entry; time t is not reset on a transition between Reset and Overtemp modes.

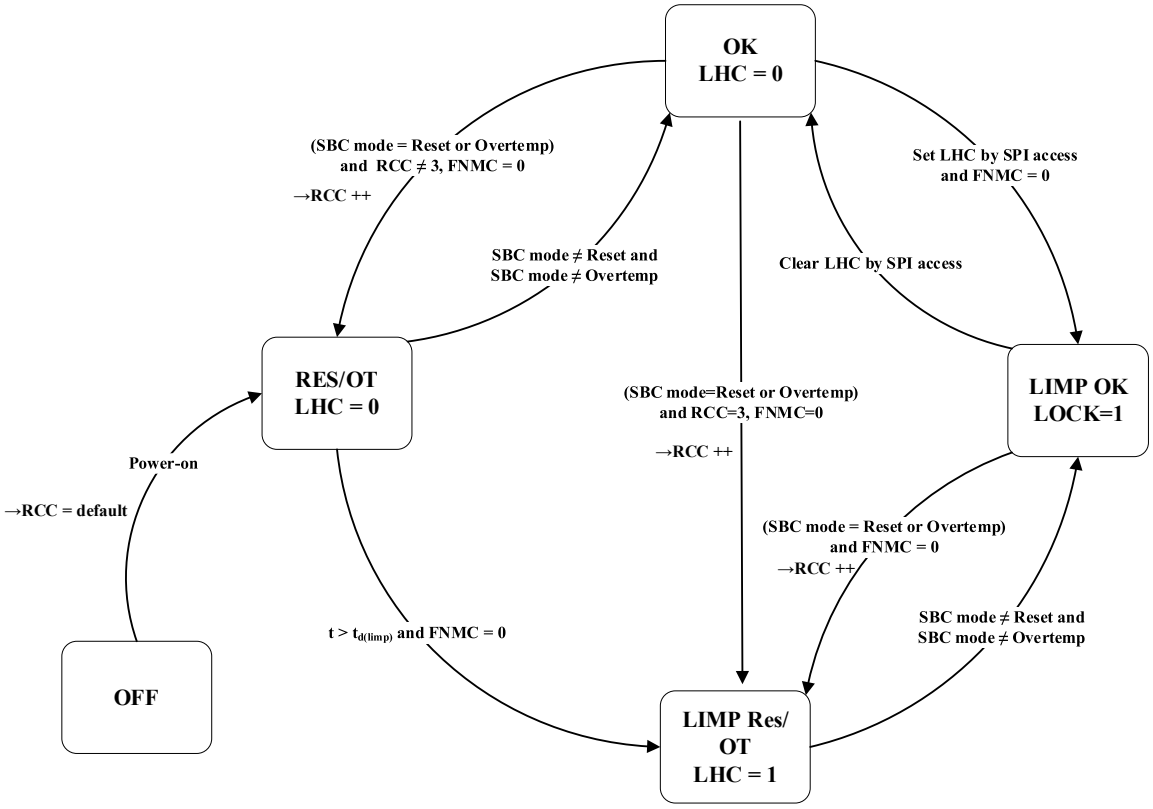


Figure 8 Limp function state diagram

10.5.2.1 Fail-safe control register

The Fail-safe control register contains the reset counter along with limp home control settings.

Table 14 Fail-safe control register (address 02h)

Bit	Symbol	Access	Value	Description
7:3	Reserved	R	-	
2	LHC	R/W		LIMP home Control:
			0	LIMP pin is floating
			1	LIMP pin is driven LOW
1:0	RCC	R/W		Reset counter control:
			xx	Incremented every time the SBC enters Reset mode while FNMC=0; RCC overflows from 11 to 00; default at power-on is 00

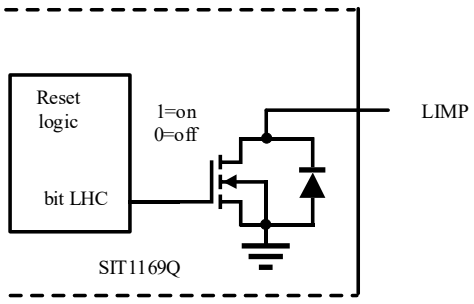


Figure 9 LIMP pin function diagram

11 CAN standard wake-up

If the CAN transceiver is in Offline mode and CAN wake-up is enabled (CWE = 1), but CAN selective wake-up is disabled (CPNC = 0 or PNCOK = 0), the SIT1169Q will monitor the bus for a wake-up pattern. A filter at the receiver input prevents unwanted wake-up events occurring due to automotive transients or EMI. A dominant-recessive-dominant wake-up pattern must be transmitted on the CAN bus within the wake-up timeout time ($t_{to(wake)bus}$) to pass the wake-up filter and trigger a wake-up event (see

Figure **10**; note that additional pulses may occur between the recessive/dominant phases). The recessive and dominant phases must last at least $t_{wake(busrec)}$ and $t_{wake(busdom)}$, respectively.

When a valid CAN wake-up pattern is detected on the bus, wake-up bit CW in the Transceiver event status register is set (see Table 26) and pin RXD is driven LOW. If the SBC was in Sleep mode when the wake-up pattern was detected, V1 is enabled to supply the microcontroller and the SBC switches to Standby mode via Reset mode.

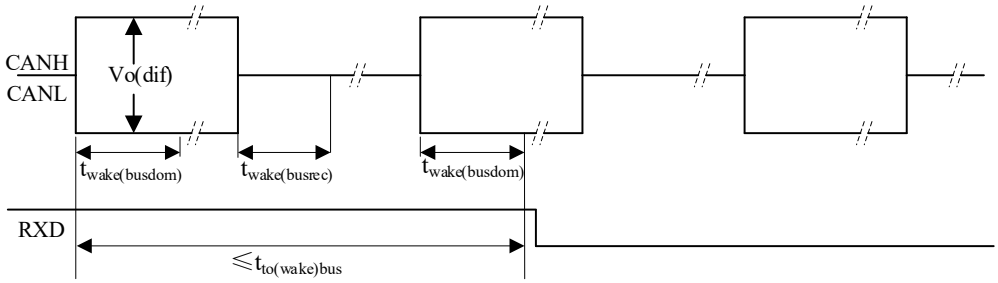


Figure 10 CAN wake-up timing

12 CAN partial networking (SIT1169Q /F variants only)

Partial networking allows nodes in a CAN network to be selectively activated in response to dedicated wake-up frames (WUF). Only nodes that are functionally required are active on the bus while the other nodes remain in a low-power mode until needed.

If both CAN wake-up (CWE = 1) and CAN selective wake-up (CPNC = 1) are enabled, and the partial networking registers are configured correctly (PNCOK = 1), the transceiver monitors the bus for dedicated CAN wake-up frames.

12.1 Wake-up frame (WUF)

A wake-up frame is a CAN frame according to ISO11898-1:2015, consisting of an identifier field (ID), a Data Length Code (DLC), a data field and a Cyclic Redundancy Check (CRC) code including the CRC delimiter.

The wake-up frame format, standard (11-bit) or extended (29-bit) identifier, is selected via bit IDE in the Frame control register (Table 18).

A valid WUF identifier is defined and stored in the ID registers (Table 16). An ID mask can be defined to allow a group of identifiers to be recognized as valid by an individual node. The identifier mask is defined in the ID mask registers (Table 17), where a 1 means ‘don’t care’.

In the example illustrated in Figure 11, based on the standard frame format, the 11-bit identifier is defined as 1A0h. The identifier is stored in ID registers 2 (29h) and 3 (2Ah). The three least significant bits of the ID mask, bits 2 to 4 of Mask register 2 (2Dh), are ‘don’t care’. This means that any of eight different identifiers will be recognized as valid in the received WUF (from 1A0h to 1A7h).

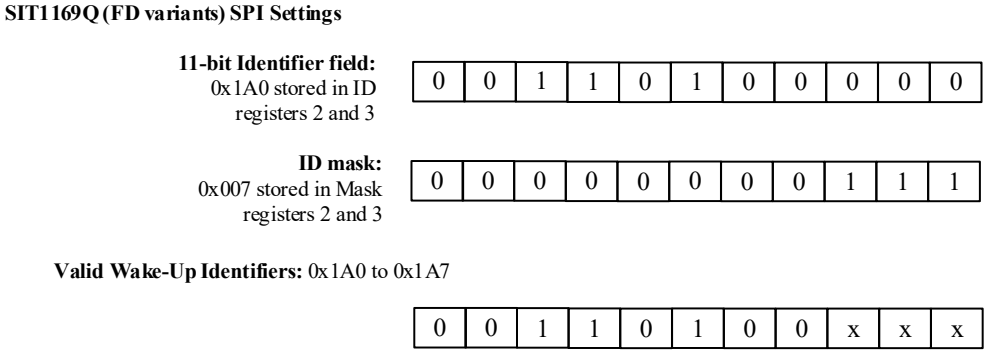


Figure 11 Evaluating the ID field in a selective wake-up frame

The data field indicates the nodes to be woken up. Within the data field, groups of nodes can be predefined and associated with bits in a data mask. By comparing the incoming data field with the data mask, multiple groups of nodes can be woken up simultaneously with a single wake-up message.

The data length code (bits DLC in the Frame control register; Table 18) determines the number of data bytes (between 0 and 8) expected in the data field of a CAN wake-up frame. If one or more data bytes are expected (DLC ≠ 0000), at least one bit in the data field of the received wake-up frame must be set to 1 and at least one equivalent bit in the associated data mask register in the transceiver (see Table 19) must also be set to 1 for a successful wake-up. Each matching pair of 1s indicates a group of nodes to be activated (since the data field is up to 8 bytes long, up to 64 groups of nodes can be defined). If DLC=0, a data field is not expected.

In the example illustrated in Figure 12, the data field consists of a single byte (DLC=1). This means that the data field in the incoming wake-up frame is evaluated against data mask 7 (stored at address 6Fh; see Table 19 and Figure 13). Data mask 7 is defined as 10101000 in the example, indicating that the node is assigned to three groups (Group1, Group 3 and Group 5).

The received message shown in Figure 12 could, potentially, wake up four groups of nodes: groups 2, 3, 4 and 5. Two matches are found (groups 3 and 5) when the message data bits are compared with the configured data mask (DM7).

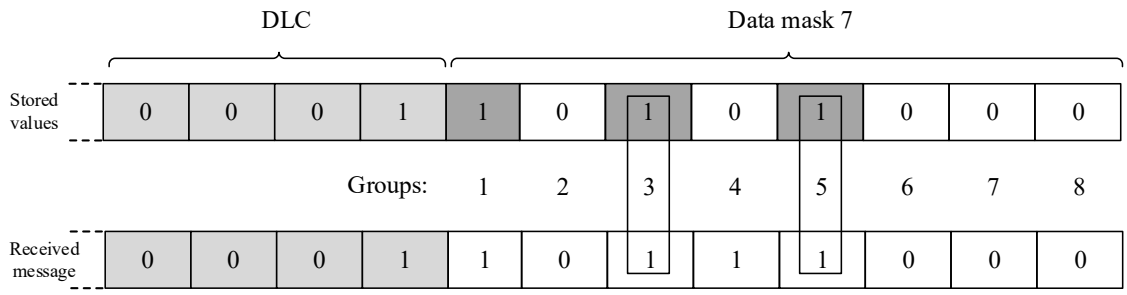


Figure 12 Evaluating the Data field in a selective wake-up frame

Optionally, the data length code and the data field can be excluded from the evaluation of the wake-up frame. If bit PNDM = 0, only the identifier field is evaluated to determine if the frame contains a valid wake-up message. If PNDM = 1 (the default value), the data field is included for wake-up filtering.

When PNDM = 0, a valid wake-up message is detected and a wake-up event is captured (and CW is set to 1) when:

• the identifier field in the received wake-up frame matches the pattern in the ID registers after filtering AND

• the CRC field in the received frame (including a recessive CRC delimiter) was received without error

When PNDM = 1, a valid wake-up message is detected when:

• the identifier field in the received wake-up frame matches the pattern in the ID registers after filtering AND

• the frame is not a Remote frame AND

• the data length code in the received message matches the configured data length code (bits DLC) AND

• if the data length code is greater than 0, at least one bit in the data field of the received frame is set and the corresponding bit in the associated data mask register is also set AND

• the CRC field in the received frame (including a recessive CRC delimiter) was received without error

If the SIT1169Q receives a CAN message containing errors (e.g. a 'stuffing' error) that are transmitted in advance of the ACK field, an internal error counter is incremented. If a CAN message is received without any errors appearing in front of the ACK field, the counter is decremented. Data received after the CRC delimiter and before the next Start of Frame (SOF) is ignored by the partial networking module. If the counter overflows (counter > 31), a frame detect error is captured (PNFDE = 1) and the device wakes up; the counter is reset to zero when the bias is switched off and partial networking is re-enabled.

Partial networking is assumed to be configured correctly when PNCOK is set to 1 by the application software. The SIT1169Q clears PNCOK after a write access to any of the CAN partial networking configuration registers.

If selective wake-up is disabled (CPNC = 0) or partial networking is not configured correctly (PNCOK = 0), and the CAN transceiver is in Offline mode with wake-up enabled (CWE = 1), then any valid wake-up pattern according to ISO 11898-2:2016 will trigger a wake-up event.

If the CAN transceiver is not in Offline mode (CMC ≠ 00) or CAN wake-up is disabled (CWE = 0), all wake-up patterns on the bus are ignored.

CAN bit rates of 50 kbit/s, 100 kbit/s, 125 kbit/s, 250 kbit/s, 500 kbit/s and 1Mbit/s are supported during selective wake-up. The bit rate is selected via bits CDR (see Table 15).

12.2 CAN FD frames

CAN FD stands for 'CAN with Flexible Data-Rate'. It is based on the CAN protocol as defined in ISO 11898-1:2015.

CAN FD is being gradually introduced into automotive market. In time, all CAN controllers will be required to comply with the new standard (enabling 'FD-active' nodes) or at least to tolerate CAN FD communication (enabling 'FD-passive' nodes). The SIT1169QTK/F, SIT1169QTK/F/3 and SIT1169QTK/X/F support FD-passive features by means of a dedicated implementation of the partial networking protocol.

The /F variants can be configured to recognize CAN FD frames as valid CAN frames. When CFDC = 1, the error counter is decremented every time the control field of a CAN FD frame is received. The SIT1169Qxx/F remains in low-power mode (CAN FD-passive) with partial networking enabled. CAN FD frames are never recognized as valid wake-up frames, even if PNDM = 0 and the frame contains a valid ID. After receiving the control field of a CAN FD frame, the SIT1169Qxx/F ignores further bus signals until idle is again detected.

CAN FD passive is supported up to a ratio of one-to-eight between arbitration and data bit rates, without unwanted wake-ups. The CAN FD filter parameter defined in ISO 11898-2:2016 and SAE J2284 is supported up to a ratio of one-to-four, with a maximum supported bit data bit rate of 2 Mbit/s and a maximum arbitration speed of 500 kbit/s.

CAN FD frames are interpreted as frames with errors by the partial networking module when CFDC = 0. So the error counter is incremented when a CAN FD frame is received. If the ratio of CAN FD frames to valid CAN frames exceeds the threshold that triggers error counter overflow, bit PNFDE is set to 1 and the device wakes up.

12.3 CAN partial networking configuration registers

Dedicated registers are provided for configuring CAN partial networking.

12.3.1 Data rate register

Table 15 Data rate register (addresses 26h)

Bit	Symbol	Access	Value	Description
7:3	Reserved	R	-	
2:0	CDR	R/W		CAN data rate selection:
			000	50 kbit/s
			001	100 kbit/s
			010	125 kbit/s
			011	250 kbit/s
			100	Reserved (intended for future use; currently selects 500 kbit/s)
			101	500 kbit/s
			110	Reserved (intended for future use; currently selects 500 kbit/s)
			111	1000 kbit/s

12.3.2 ID registers

Table 16 ID registers 0 to 3 (addresses 27h to 2Ah)

Addr.	Bit	Symbol	Access	Value	Description
27h	7:0	ID07:ID00	R/W	-	Bits ID07 to ID00 of the extended frame format
28h	7:0	ID15:ID08	R/W	-	Bits ID15 to ID08 of the extended frame format
29h	7:2	ID23:ID18	R/W	-	Bits ID23 to ID18 of the extended frame format Bits ID05 to ID00 of the standard frame format
	1:0	ID17:ID16	R/W	-	Bits ID17 to ID16 of the extended frame format
2Ah	7:5	Reserved	R	-	
	4:0	ID28:ID24	R/W	-	Bits ID28 to ID24 of the extended frame format Bits ID10 to ID06 of the standard frame format

12.3.3 ID mask registers

Table 17 ID mask registers 0 to 3 (addresses 2Bh to 2Eh)

Addr.	Bit	Symbol	Access	Value	Description
2Bh	7:0	M07:M00	R/W	-	Mask bits ID07 to ID00 of extended frame format
2Ch	7:0	M15:M08	R/W	-	Mask bits ID15 to ID08 of extended frame format
2Dh	7:2	M23:M18	R/W	-	Mask bits ID23 to ID18 of the extended frame format Mask bits ID05 to ID00 of the standard frame format
	1:0	ID17:ID16	R/W	-	Mask bits ID17 to ID16 of the extended frame format
2Eh	7:5	Reserved	R	-	
	4:0	ID28:ID24	R/W	-	Mask bits ID28 to ID24 of the extended frame format Mask. bits ID10 to ID06 of the standard frame format

12.3.4 Frame control register

Table 18 Frame control register (address 2Fh)

Bit	Symbol	Access	Value	Description
7	IDE	R/W	-	Identifier format:
			0	Standard frame format (11-bit)
			1	Extended frame format (29-bit)
6	PNDM	R/W	-	Partial networking data mask:
			0	Data length code and data field are ‘don’t care’ for wake-up
			1	Data length code and data field are evaluated at wake-up
5:4	Reserved	R	-	
3:0	DLC	R/W		Number of data bytes expected in a CAN frame:
			0000	0
			0001	1
			0010	2
			0011	3

Bit	Symbol	Access	Value	Description
			0100	4
			0101	5
			0110	6
			0111	7
			1000	8
			1001 to 1111	Tolerated, 8 bytes expected

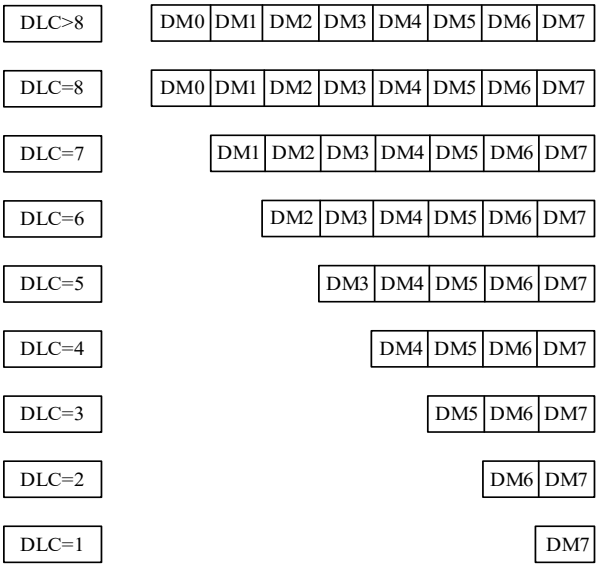


Figure 13 Data mask register usage for different values of DLC

12.3.5 Data mask registers

Table 19 Data mask registers (addresses 68h to 6Fh)

Addr.	Bit	Symbol	Access	Value	Description
68h	7:0	DM0	R/W	-	Data mask 0 configuration
69h	7:0	DM1	R/W	-	Data mask 1 configuration
6Ah	7:0	DM2	R/W	-	Data mask 2 configuration
6Bh	7:0	DM3	R/W	-	Data mask 3 configuration
6Ch	7:0	DM4	R/W	-	Data mask 4 configuration
6Dh	7:0	DM5	R/W	-	Data mask 5 configuration
6Eh	7:0	DM6	R/W	-	Data mask 6 configuration
6Fh	7:0	DM7	R/W	-	Data mask 7 configuration

13 Local wake-up via WAKE pin

Local wake-up is enabled via bits WPRE and WPFE in the WAKE pin event capture enable register (see Table 31). A wake-up event is triggered by a LOW-to-HIGH (if WPRE=1) and/or a HIGH-to-LOW (if WPFE=1) transition on the WAKE pin. This arrangement allows for maximum flexibility when designing a local wake-up circuit. In applications that don't make use of the local wake-up facility, local wake-up should be disabled and the WAKE pin connected to GND to ensure optimal EMI performance. While the SBC is in Normal mode, the status of the voltage on pin WAKE can always be read via bit WPVS. Otherwise, WPVS is only valid if local wake-up is enabled (WPRE=1 and/or WPFE=1).

Table 20 WAKE pin status register (address 4Bh)

Bit	Symbol	Access	Value	Description
7:2	Reserved	R	-	
1	WPVS	R		WAKE pin status:
			0	voltage on WAKE pin below switching threshold WAKE ($V_{th(sw)}$)
			1	voltage on WAKE pin above switching threshold ($V_{th(sw)}$)
0	Reserved	R	-	

14 CAN fail-safe features

14.1 TXD dominant timeout

A TXD dominant time-out timer is started when pin TXD is forced LOW while the transceiver is in CAN Active Mode. If the LOW state on pin TXD persists for longer than the TXD dominant time-out time ($t_{to(dom)TXD}$), the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD goes HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 4.4 kbit/s.

When the TXD dominant time-out time is exceeded, a CAN failure event is captured (CF=1; see Table 26), if enabled (CFE=1; see Table 30). In addition, the status of the TXD dominant timeout can be read via the CFS bit in the Transceiver status register (Table 5) and bit CTS is cleared.

14.2 Pull-up on TXD pin

Pin TXD has an internal pull-up towards V1 to ensure a safe defined recessive driver state in case the pin is left floating.

14.3 V_{CAN} undervoltage event

When CMC = 01, a CAN failure event is captured (CF = 1), if enabled (CFE=1), when the supply to the CAN transceiver falls below the undervoltage detection threshold, Vuvd(CAN). In addition, status bit VCS is set to 1.

14.4 Loss of power at pin BAT

A loss of power at pin BAT has no influence on the bus lines or on the microcontroller. No reverse currents will flow from the bus. This ensures that a loss of power at BAT does not affect ongoing communication between nodes on the network.

15 Wake-up and interrupt event diagnosis via pin RXD

Wake-up and interrupt event diagnosis in the SIT1169Q is intended to provide the microcontroller with information on the status of a range of features and functions. This information is stored in the event status registers (Table 24 to Table 26) and is signaled on pin RXD, if enabled. A distinction is made between regular wake-up events and interrupt events (at least one regular wake-up source must be enabled to allow the SIT1169Q to switch to Sleep mode.

Table 21 Regular events

Symbol	Event	Power-on	Description
CW	CAN wake-up	Disabled	see Transceiver event status register (Table 26)
WPR	Rising edge on WAKE pin	Disabled	see WAKE pin event capture status register (Table 27)
WPF	Falling edge on WAKE pin	Disabled	

Table 22 Diagnostic events

Symbol	Event	Power-on	Description
PO	Power-on	Always enabled	see System event status register (Table 24)
OTW	Overtemperature warning	Disabled	
SPIF	SPI failure	Disabled	
WDF	Watchdog failure	Always enabled	
V2O (1)	V2 overvoltage	Disabled	see Supply event status register (Table 25)
VEXTO (2)	VEXT overvoltage	Disabled	
V2U (1)	V2 undervoltage	Disabled	
VEXTU (2)	VEXT undervoltage	Disabled	see Supply event status register (Table 25)
V1U	V1 undervoltage	Disabled	
PNFDE (3)	PN frame detection error	Always enabled	see Transceiver event status register (Table 30)
CBS	CAN-bus silence	Disabled	
CF	CAN failure	Disabled	

(1) SIT1169QTK, SIT1169QTK/3, SIT1169QTK/F and SIT1169QTK/F/3 only.

(2) SIT1169QTK/X and SIT1169QTK/X/F only.

(3) SIT1169QTK/F, SIT1169QTK/F/3 and SIT1169QTK/X/F only; otherwise reserved.

PO, WDF and PNFDE interrupts are always enabled and thus captured. Wake-up and interrupt detection can be enabled/disabled for the remaining events individually via the event capture enable registers (Table 28 to Table 30).

If an event occurs while the associated event capture function is enabled, the relevant event status bit is set. If the transceiver is in CAN Offline mode with V1 active (SBC Normal or Standby mode), pin RXD is forced LOW to indicate that a wake-up or interrupt event has been detected. If the SIT1169Q is in sleep mode when the event occurs, the microcontroller supply, V1, is activated and the SBC switches to Standby mode (via Reset mode).

The microcontroller can monitor events via the event status registers. An extra status register, the Global event status register (Table 23), is provided to help speed up software polling routines. By polling the Global event status register, the microcontroller can quickly determine the type of event captured (system, supply, transceiver or WAKE pin) and then query the relevant event status register (Table 24, Table 25, Table 26 or Table 27 respectively).

After the event source has been identified, the status flag should be cleared (set to 0) by writing 1 to the relevant bit (writing 0 will have no effect). A number of status bits can be cleared in a single write operation by writing 1 to all relevant bits.

It is strongly recommended to clear only the status bits that were set to 1 when the status registers were last read. This precaution ensures that events triggered just before the write access are not lost.

15.1 Interrupt/wake-up delay

If interrupt or wake-up events occur very frequently while the transceiver is in CAN Offline mode, they can have a significant impact on the software processing time (because pin RXD is repeatedly driven LOW, requiring a response from the microcontroller each time an interrupt/wake-up is generated). The SIT1169Q incorporates an event delay timer to limit the disturbance to the software.

When one of the event capture status bits is cleared, pin RXD is released (HIGH) and a timer is started. If further events occur while the timer is running, the relevant status bits are set. If one or more events are pending when the timer expires after $t_{d(event)}$, pin RXD goes LOW again to alert the microcontroller. In this way, the microcontroller is interrupted once to process a number of events rather than several times to process individual events.

If all events are cleared while the timer is running, RXD remains HIGH after the timer expires, since there are no pending events. The event capture registers can be read at any time.

The event capture delay timer is stopped immediately when pin RSTN goes low (triggered by a HIGH-to-LOW transition on the pin). RSTN is driven LOW when the SBC enters Reset, Sleep, Overtemp and Off modes. A pending event is signaled on pin RXD when the SBC enters Sleep mode.

15.2 Sleep mode protection

The wake-up event capture function is critical when the SIT1169Q is in Sleep mode, because the SBC will only leave Sleep mode in response to a captured wake-up event. To avoid potential system deadlocks, the SBC distinguishes between regular and diagnostic events. Wake-up events (via the CAN bus or the WAKE pin) are classified as regular events; diagnostic events signal failure/error conditions or state changes. At least one regular wake-up event must be enabled before the SIT1169Q can switch to Sleep mode. Any attempt to enter Sleep mode while all regular wake-up events are disabled will trigger a system reset.

Another condition that must be satisfied before the SIT1169Q can switch to Sleep mode is that all event status bits must be cleared. If an event is pending when the SBC receives a Sleep mode command (MC=001), it will immediately switch to Reset mode. This condition applies to both regular and diagnostic events.

Sleep mode can be permanently disabled in applications where, for safety reasons, the supply voltage to the host controller must never be cut off. Sleep mode is permanently disabled by setting the Sleep control bit (SLPC) in the SBC configuration register (see Table 8) to 1. This register is located in the non-volatile memory area of the device. When SLPC = 1, a Sleep mode SPI command (MC = 001) will trigger an SPI failure event instead of a transition to Sleep mode.

15.3 Event status and event capture registers

After an event source has been identified, the status flag should be cleared (set to 0) by writing 1 to the relevant status bit (writing 0 will have no effect).

Table 23 Global event status register (address 60h)

Bit	Symbol	Access	Value	Description
7:4	Reserved	R	-	
3	WPE	R		WAKE pin event:
			0	no pending WAKE pin event
			1	WAKE pin event pending at address 64h
2	TRXE	R		transceiver event:
			0	no pending transceiver event
			1	transceiver event pending at address 63h
1	SUPE	R		supply event:
			0	no pending supply event
			1	supply event pending at address 62h
0	SYSE	R		system event:

Bit	Symbol	Access	Value	Description
			0	no pending system event
			1	system event pending at address 61h

Table 24 System event status register (address 61h)

Bit	Symbol	Access	Value	Description
7:5	Reserved	R	-	
4	PO	R/W		Power-on:
			0	No recent battery power-on
			1	The SIT1169Q has left off mode after battery power-on
3	Reserved	R	-	
2	OTW	R/W		overtemperature warning:
			0	overtemperature not detected
			1	The global chip temperature has exceeded the overtemperature warning threshold, $T_{th(warn)otp}$ (not in Sleep mode
1	SPIF	R/W		SPI failure:
			0	no SPI failure detected
			1	SPI clock count error (only 16-, 24- and 32-bit commands are valid), illegal WMC, NWP or MC code or attempted write access to locked register (not in Sleep mode)
0	WDF	R/W		watchdog failure:
			0	no watchdog failure event captured
			1	watchdog overflow in Timeout mode; when the watchdog overflows in Timeout mode, a system reset is only performed if a WDF is already pending (WDF = 1)

Table 25 Supply event status register (address 62h)

Bit	Symbol	Access	Value	Description
7:3	Reserved	R	-	
2	V2O [1]/ VEXTO [2]	R/W		V2/VEXT overvoltage:
			0	no V2/VEXT overvoltage event captured
			1	V2/VEXT overvoltage event captured
1	V2U [1]/ VEXTU [2]	R/W		V2/VEXT undervoltage:
			0	no V2/VEXT undervoltage event captured
			1	V2/VEXT undervoltage event captured
0	V1U	R/W		V1 undervoltage:
			0	No V1 undervoltage event capture
			1	Voltage on V1 has dropped below the 90% undervoltage

Bit	Symbol	Access	Value	Description
				threshold while V1 is active (event is not captured in Sleep mode because V1 is off); V1U event capture is independent of the setting of bits V1RTC

(1) SIT1169QTK, SIT1169QTK/3, SIT1169QTK/F and SIT1169QTK/F/3 only.

(2) SIT1169QTK/X and SIT1169QTK/X/F only.

Table 26 Transceiver event status register (address 63h)

Bit	Symbol	Access	Value	Description
7:6	Reserved	R	-	
5	PNFDE	R/W		partial networking frame detection error:
			0	No partial networking frame detection error detected
			1	Partial networking frame detection error detected
4	CBS	R/W		CAN bus status:
			0	CAN bus active
			1	No activity on CAN bus for $t_{to(silence)}$ (detected only when CBSE=1 while bus active)
3:2	Reserved	R	-	
1	CF	R/W		CAN failure:
			0	No CAN failure detected
			1	(CMC = 01 & CAN transceiver deactivated due to V_{CAN} undervoltage) OR dominant clamped TXD (not in Sleep mode)
0	CW	R/W		CAN wake-up:
			0	no CAN wake-up event detected
			1	CAN wake-up event detected while the transceiver is in CAN Offline Mode

Table 27 WAKE pin event status register (address 64h)

Bit	Symbol	Access	Value	Description
7:2	Reserved	R	-	
1	WPR	R/W		WAKE pin rising edge:
			0	No rising edge detected on WAKE pin
			1	Rising edge detected on WAKE pin
0	WPF	R/W		WAKE pin falling edge:
			0	No falling edge detected on WAKE pin
			1	Falling edge detected on WAKE pin

Table 28 System event capture enable register (address 04h)

Bit	Symbol	Access	Value	Description
7:3	Reserved	R	-	
2	OTWE	R/W		Overtemperature warning enable:
			0	Overtemperature warning disabled
			1	Overtemperature warning enabled
1	SPIFE	R/W		SPI failure enable:
			0	SPI failure detection disabled
			1	SPI failure detection enabled
0	Reserved	R	-	

Table 29 Supply event capture enable register (address 1Ch)

Bit	Symbol	Access	Value	Description
7:3	Reserved	R	-	
2	V2OE (1) VEXTOE (2)	R/W		V2/VEXT overvoltage enable:
			0	V2/VEXT overvoltage detection disabled
			1	V2/VEXT overvoltage detection enabled
1	V2UE (1) VEXTUE (2)	R/W		V2/VEXT undervoltage enable:
			0	V2/VEXT undervoltage detection disabled
			1	V2/VEXT undervoltage detection enabled
0	V1UE	R/W		V1 undervoltage enable:
			0	V1 undervoltage detection disabled
			1	V1 undervoltage detection enabled

(1) SIT1169QTK, SIT1169QTK/3, SIT1169QTK/F and SIT1169QTK/F/3 only.

(2) SIT1169QTK/X and SIT1169QTK/X/F only.

Table 30 Transceiver event capture enable register (address 23h)

Bit	Symbol	Access	Value	Description
7:5	Reserved	R	-	
4	CBSE	R/W		CAN bus silence enable:
			0	CAN bus silence detection disabled
			1	CAN bus silence detection enabled
3:2	Reserved	R	-	
1	CFE	R/W		CAN failure enable:
			0	CAN failure detection disabled
			1	CAN failure detection enabled
0	CWE	R/W		CAN wake-up enable:
			0	CAN wake-up detection disabled

Bit	Symbol	Access	Value	Description
			1	CAN wake-up detection enabled

Table 31 WAKE pin event capture enable register (address 4Ch)

Bit	Symbol	Access	Value	Description
7:2	Reserved	R	-	
1	WPRE	R/W		WAKE pin rising-edge enable:
			0	Rising-edge detection on WAKE pin disabled
			1	Rising-edge detection on WAKE pin enabled
0	WPFE	R/W		WAKE pin falling-edge enable:
			0	Falling-edge detection on WAKE pin disabled
			1	Falling-edge detection on WAKE pin enabled

16 Non-volatile SBC configuration

The SIT1169Q contains Multiple Time Programmable Non-Volatile (MTPNV) memory cells that allow some of the default device settings to be reconfigured. The MTPNV memory address range is from 0x73 to 0x74. An overview of the MTPNV registers is given in Table 8 and Table 11.

16.1 Programming MTPNV cells

The SIT1169Q must be in Forced Normal mode and the MTPNV cells must contain the factory preset values before the non-volatile memory can be reprogrammed (FNMC = 1 and NVMPS = 1). The SIT1169Q will switch to Forced Normal mode after a reset event (e.g. pin RSTN LOW) when the MTPNV cells contain the factory preset values (since FNMC = 1). The factory presets may need to be restored before reprogramming can begin. When the factory presets have been restored, a system reset is generated automatically and SIT1169Q switches to Forced Normal mode.

Programming of the non-volatile memory registers is performed in two steps. First, the required values are written to addresses 0x73 and 0x74. In the second step, reprogramming is confirmed by writing the correct CRC value to the MTPNV CRC control register. The SBC starts reprogramming the MTPNV cells as soon as the CRC value has been validated. If the CRC value is not correct, reprogramming is aborted. On completion, a system reset is generated to indicate that the MTPNV cells have been reprogrammed successfully. Note that the MTPNV cells cannot be read while they are being reprogrammed.

After an MTPNV programming cycle has been completed, the non-volatile memory is protected from being overwritten via a standard SPI write operation.

The MTPNV cells can be reprogrammed a maximum of 200 times ($N_{cy(W)MTP}$). Bit NVMPS in the MTPNV status register (Table 32) indicates whether the on-volatile cells can be reprogrammed. This register also contains a write counter, WRCNTS, that is incremented each time the MTPNV cells are reprogrammed (up to a maximum value of 111111.There is overflow. Performing a factory reset also increments the counter). This counter is provided for information purposes only; reprogramming will not be rejected when it reaches its maximum value.

An error correction code status bit, ECCS, is set to indicate that the CRC check mechanism in the SBC has detected a single bit failure in non-volatile memory. If more than one bit failure is detected, the SBC will not restart after MTPNV reprogramming. Check the ECCS flag at the end of the production cycle to verify the content of non-volatile memory. When this flag is set, it indicates a device or ECU failure.

Table 32 MTPNV status register (address 70h)

Bit	Symbol	Access	Value	Description
7:2	WRCNTS	R	-	Write counter status:
			xxxxxx	Contains the number of times the MTPNV cells were reprogrammed
1	ECCS	R		Error correction code status:
			0	No bit failure detected in non-volatile memory
			1	Bit failure detected and corrected in non-volatile memory
0	NVMPS	R		Non-volatile memory programming status:
			0	MTPNV memory cannot be overwritten
			1(1)	MTPNV memory is ready to be reprogrammed

(1) Factory preset value.

Calculating the CRC value for MTP programming

The cyclic redundancy check value stored in bits CRCC in the MTPNV CRC control register is calculated using the data written to registers 0x73 and 0x74.

Table 33 MTPNV CRC control register (address 75h)

Bit	Symbol	Access	Value	Description
7:0	CRCC	W		Cyclic redundancy check control:
			-	CRC control data

The CRC value is calculated using the data representation show in Figure 14 and the modulo-2 division with the generator polynomial: $x^8+x^5+x^3+x^2+x+1$. The result of this operation must be bitwise inverted.

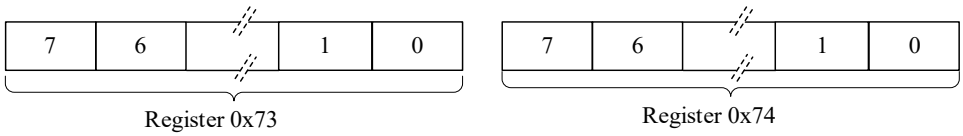


Figure 14 Data representation for CRC calculation

The following parameters can be used to calculate the CRC value (e.g. via the AUTOSAR method):

Table 34 Parameter for CRC coding

Parameter	Value
CRC result width	8 bits
Polynomial	2Fh

Parameter	Value
Initial value	FFh
Input data reflected	no
Result data reflected	no
XOR value	FFh

Alternatively, the following algorithm can be used:

```
data = 0 // unsigned byte
crc = FFh
for i = 0 to 1
    data = content_of_address (73h+i) EXOR crc
    for j = 0 to 7
        if data ≥ 128
            data = data * 2 // shift left by 1
            data = data EXOR 2Fh
        else
            data = data * 2 // shift left by 1
    next j
    crc = data
next i
crc = crc EXOR FFh
```

16.2 Restoring factory preset values

Factory preset values are restored if the following conditions apply for at least $t_{d(MTPNV)}$ during power-up:

• RSTN is held LOW

• CANH is pulled up to VBAT

• CANL is pulled down to GND

After the factory preset values have been restored, the SBC performs a system reset and enters Forced normal Mode. Since the CAN bus is clamped dominant, pin RXD is forced LOW. During the factory preset restore process, this pin is forced HIGH; a falling edge on this pin caused by bit PO being set after power-on then clearly indicates that the process has been completed.

Note that the write counter, WRCNTS, in the MTPNV status register is incremented every time the factory presets are restored.

17 Device ID

A byte is reserved at address 0x7E for a SIT1169Q identification code.

Table 35 Identification register (address 7Eh)

Bit	Symbol	Access	Value	Description
7:0	IDS [7:0]	R		Identification status:
			CFh	SIT1169QTK
			C9h	SIT1169QTK/3
			EFh	SIT1169QTK/F
			E9h	SIT1169QTK/F/3
			CEh	SIT1169QTK/X
			EEh	SIT1169QTK/X/F

18 Lock control register

Sections of the register address area can be write-protected to protect against unintended modifications. Note that this facility only protects locked bits from being modified via the SPI and will not prevent the SIT1169Q updating status registers etc.

Table 36 Lock control register (address 0Ah)

Bit	Symbol	Access	Value	Description
7	Reserved	R	-	
6	LK6C	R/W		lock control 6: address area 68h to 6Fh - data mask (/F version only)
			0	SPI write access enabled
			1	SPI write access disabled
5	LK5C	R/W		lock control 5: address area 50h to 5Fh - unused register range
			0	SPI write access enabled
			1	SPI write access disabled
4	LK4C	R/W		lock control 4: address area 40h to 4Fh - WAKE pin control
			0	SPI write access enabled
			1	SPI write access disabled
3	LK3C	R/W		lock control 3: address area 30h to 3Fh - unused register range
			0	SPI write access enabled
			1	SPI write access disabled
2	LK2C	R/W		lock control 2: address area 20h to 2Fh - transceiver control
			0	SPI write access enabled
			1	SPI write access disabled
1	LK1C	R/W		lock control 1: address area 10h to 1Fh - regulator control
			0	SPI write access enabled

Bit	Symbol	Access	Value	Description
			1	SPI write access disabled
0	LK0C	R/W		lock control 0: address area 06h to 09h - general-purpose memory
			0	SPI write access enabled
			1	SPI write access disabled

19 SPI

The Serial Peripheral Interface (SPI) provides the communication link with the microcontroller, supporting multi-slave operations. The SPI is configured for full duplex data transfer, so status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing registers to be read back by the application without changing the register content.

The SPI uses four interface signals for synchronization and data transfer:

• SCSN: SPI chip select; active LOW

• SCK: SPI clock; default level is LOW due to low-power concept (pull-down)

• SDI: SPI data input

• SDO: SPI data output; floating when pin SCSN is HIGH

Bit sampling is performed on the falling edge of the clock and data is shifted in/out on the rising edge, as illustrated in Figure 15.

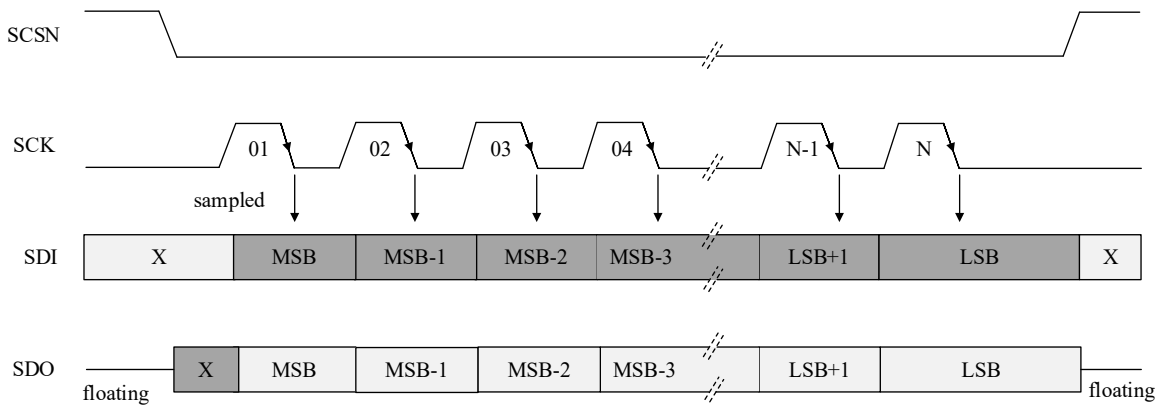


Figure 15 SPI timing overview

The SPI data in the SIT1169Q is stored in a number of dedicated 8-bit registers. Each register is assigned a unique 7-bit address. Two bytes must be transmitted to the SBC for a single register write operation. The first byte contains the 7-bit address along with a ‘read-only’ bit (the LSB). The read-only bit must be 0 to indicate a write operation (if this bit is 1, a read operation is assumed and any data on the SDI pin is ignored). The second byte contains the data to be written to the register.

24- and 32-bit read and write operations are also supported. The register address is automatically incremented, once for a 24-bit operation and twice for a 32-bit operation, as illustrated in Figure 16.

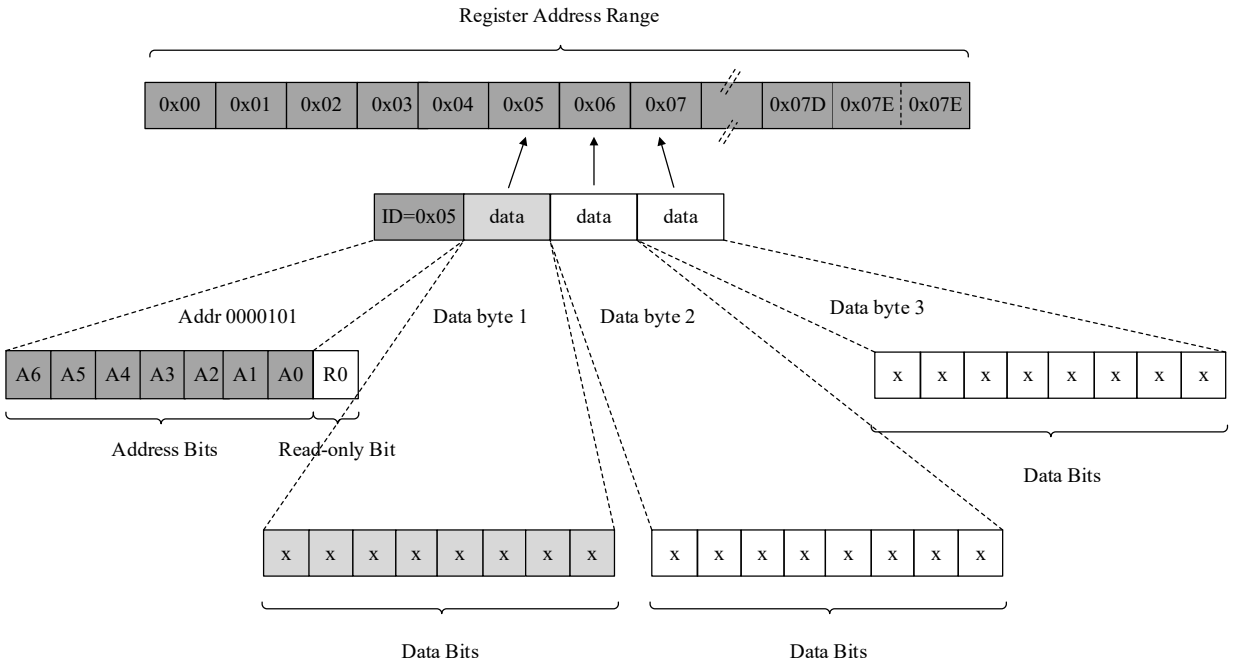


Figure 16 SPI data structure for a write operation (16-, 24- or 32-bit)

During an SPI data read or write operation, the contents of the addressed register(s) is returned via pin SDO. The SIT1169Q tolerates attempts to write to registers that don't exist. If the available address space is exceeded during a write operation, the data above the valid address range is ignored (without generating an SPI failure event).

During a write operation, the SIT1169Q monitors the number of SPI bits transmitted. If the number recorded is not 16, 24 or 32, then the write operation is aborted and an SPI failure event is captured (SPIF=1).

If more than 32 bits are clocked in on pin SDI during a read operation, the data stream on SDI is reflected on SDO from bit 33 onwards.

20 Register map

Table 37 Overview of primary control registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x00	Watchdog control	WMC			Reserved	NWP			
0x01	Mode control	Reserved					MC		
0x02	Fail-safe control	Reserved					LHC	RCC	
0x03	Main status	Reserved	OTWS	NMS	RSS				
0x04	System event enable	Reserved					OTWE	SPIFE	Reserved
0x05	Watchdog status	Reserved				FNMS	SDMS	WDS	

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x06	Memory 0	GPM [7:0]							
0x07	Memory 1	GPM [15:8]							
0x08	Memory 2	GPM [23:16]							
0x09	Memory 3	GPM [31:24]							
0x0A	Lock control	Reserved	LK6C	LK5C	LK4C	LK3C	LK2C	LK1C	LK0C

Table 38 Overview of regulator control register

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x10	Regulator control	Reserved (1)	PDC	Reserved		V2C (2)/VEXTC (3)		V1RTC (4)	
0x1B	Supply status	Reserved				V2S (2)/VEXTS (3)			V1S
0x1C	Supply event enable	Reserved				V2OE (2)/ VEXTOE (3)		V2UE (2)/ VEXTUE (3)	V1UE

(1) Reserved bits can be read and overwritten without affecting device functionality; default value at power-up is 00 (other reserved bits always return 0).

(2) SIT1169QTK, SIT1169QTK/3, SITQTK/F and SIT1169QTK/F/3 only.

(3) SIT1169QTK/X and SIT1169QTK/X/F only.

(4) Fixed at 00 in SIT1169QTK/3 and SIT1169QTK/F/3.

Table 39 Overview of transceiver control and partial networking registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x20	CAN control	Reserved	CFDC (1)	PNCOK (1)	CPNC (1)	Reserved		CMC	
0x22	Transceiver status	CTS	CPNERR (1)	CPNS (1)	COSCS (1)	CBSS	Reserved	VCS	CFS
0x23	Transceiver event enable	Reserved			CBSE	Reserved		CFE	CWE
0x26	Data rate	Reserved					CDR (1)		
0x27	Identifier 0	ID [7:0] (1)							
0x28	Identifier 1	ID [15:8] (1)							
0x29	Identifier 2	ID [23:16] (1)							
0x2A	Identifier 3	Reserved			ID [28:24] (1)				
0x2B	Mask 0	M [7:0] (1)							
0x2C	Mask 1	M [15:8] (1)							
0x2D	Mask 2	M [23:16] (1)							

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x2E	Mask 3	Reserved			M [28:24] (1)				
0x2F	Frame control	IDE (1)	PNDM (1)	Reserved		DLC (1)			
0x68	Data mask 0	DM0[7:0] (1)							
0x69	Data mask 1	DM1[7:0] (1)							
0x6A	Data mask 2	DM2[7:0] (1)							
0x6B	Data mask 3	DM3[7:0] (1)							
0x6C	Data mask 4	DM4[7:0] (1)							
0x6D	Data mask 5	DM5[7:0] (1)							
0x6E	Data mask 6	DM6[7:0] (1)							
0x6F	Data mask 7	DM7[7:0] (1)							

(1) SIT1169QTK/F, SIT1169QTK/F/3 and SIT1169QTK/X/F only.

Table 40 Overview of WAKE pin control and status registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x4B	WAKE pin status	Reserved						WPVS	Reserved
0x4C	WAKE pin enable	Reserved						WPRE	WPFE

Table 41 Overview of event capture registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x60	Global event status	Reserved				WPE	TRXE	SUPE	SYSE
0x61	System event status	Reserved			PO	Reserved	OTW	SPIF	WDF
0x62	Supply event status	Reserved					V2O (1)/ VEXTO (2)	V2U (1)/ VEXTU (2)	V1U
0x63	Transceiver event status	Reserved	PNFDE (3)		CBS	Reserved		CF	CW
0x64	WAKE pin event status	Reserved						WPR	WPF

(1) SIT1169QTK, SIT1169QTK/3, SIT1169QTK/F and SIT1169QTK/F/3 only.

(2) SIT1169QTK/X and SIT1169QTK/X/F only.

(3) SIT1169QTK/F, SIT1169QTK/F/3 and SIT1169QTK/X/F only.

Table 42 Overview of MTPNV status register

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x70	MTPNV status	WRCNTS						ECCS	NVMPS

Table 43 Overview of Start-up control register

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x73	Start-up control	Reserved		RLC		V2SUC (1)/ VEXTSUC (2)	Reserved		

(1) SIT1169QTK, SIT1169QTK/3, SIT1169QTK/F and SIT1169QTK/F/3 only.

(2) SIT1169QTK/X and SIT1169QTK/X/F only.

Table 44 Overview of SBC configuration control register

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x74	SBC configuration control	Reserved		V1RTSUC		FNMC	SDMC	Reserved	SLPC

Table 45 Overview of CRC control register

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x75	MTPNV CRC control	CRCC [7:0]							

Table 46 Overview of Identification register

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x7E	Identification	IDS [7:0]							

20.1 Register configuration in SIT1169Q operating modes

A number of register bits may change state automatically when the SIT1169Q switches from one operating mode to another. This is particularly evident when the SIT1169Q switches to Off mode. These changes are summarized in Table 47. If an SPI transmission is in progress when the SIT1169Q changes state, the transmission is ignored (automatic state changes have priority).

Table 47 Register bit settings in SIT1169Q operating modes

Symbol	Off (power-on default)	Standby	Normal (1)	Sleep	Overtempt	Reset
CBS	0	No change	No change	No change	No change	No change
CBSE	0	No change	No change	No change	No change	No change
CBSS	1	Actual state	Actual state	No change	Actual state	Actual state
CDR (2)	101	No change	No change	No change	No change	No change
CF	0	No change	No change	No change	No change	No change
CFDC (2)	0	No change	No change	No change	No change	No change
CFE	0	No change	No change	No change	No change	No change
CFS	0	Actual state	Actual state	Actual state	Actual state	Actual state
CMC	01	No change	No change	No change	No change	No change

Symbol	Off (power-on default)	Standby	Normal (1)	Sleep	Overtempt	Reset
COSCS (2)	0	Actual state	Actual state	Actual state	Actual state	Actual state
CPNC (2)	0	No change	No change	No change	No change	No change
CPNERR (2)	1	Actual state	Actual state	Actual state	Actual state	Actual state
CPNS (2)	0	Actual state	Actual state	Actual state	Actual state	Actual state
CRCC	00000000	No change	No change	No change	No change	No change
CTS	0	0	Actual state	0	0	0
CW	0	No change	No change	No change	No change	No change
CWE	0	No change	No change	No change	No change	No change
DMn (2)	11111111	No change	No change	No change	No change	No change
DLC (2)	0000	No change	No change	No change	No change	No change
ECCS	Actual state	Actual state	Actual state	Actual state	Actual state	Actual state
FNMC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
FNMS	0	Actual state	Actual state	Actual state	Actual state	Actual state
GPMn	0	No change	No change	No change	No change	No change
IDn	0	No change	No change	No change	No change	No change
IDE	0	No change	No change	No change	No change	No change
IDS	See Table 35	No change	No change	No change	No change	No change
LHC	0	No change	No change	No change	1 if $t>t_{d(limp)}$, otherwise no change	1 if RCC=3 or $t>t_{d(limp)}$; otherwise, no change
LKnC	0	No change	No change	No change	No change	No change
MC	100	100	111	001	Don’t care	100
NMS	1	No change	0	No change	No change	No change
NVMPS	Actual state	Actual state	Actual state	Actual state	Actual state	Actual state
NWP	0100	No change	No change	No change	0100	0100
OTW	0	No change	No change	No change	No change	No change
OTWE	0	No change	No change	No change	No change	No change
OTWS	0	Actual state	Actual state	Actual state	Actual state	Actual state
PDC	0	No change	No change	No change	No change	No change
PNCOK (2)	0	No change	No change	No change	No change	No change
PNDM (2)	1	No change	No change	No change	No change	No change
PNFDE (2)	0	No change	No change	No change	No change	No change
PO	1	No change	No change	No change	No change	No change

Symbol	Off (power-on default)	Standby	Normal (1)	Sleep	Overtempt	Reset
RCC	00	No change	No change	No change	No change	RCC++
RLC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
RSS	00000	No change	No change	No change	10010	Reset source
SDMC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
SDMS	0	Actual state	Actual state	Actual state	Actual state	Actual state
SLPC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
SPIF	0	No change	No change	No change	No change	No change
SPIFE	0	No change	No change	No change	No change	No change
SUPE	0	No change	No change	No change	No change	No change
SYSE	1	No change	No change	No change	No change	No change
TRXE	0	No change	No change	No change	No change	No change
V1RTC	Determined by V1RTSUC in 5V variants (3)	No change	No change	No change	No change	No change
V1RTSUC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
V1S	0	Actual state	Actual state	Actual state	Actual state	Actual state
V1UE	0	No change	No change	No change	No change	No change
V1U	0	No change	No change	No change	No change	No change
VCS	0	Actual state	Actual state	Actual state	Actual state	Actual state
V2C (4) /VEXTC (5)	Determined by V2SUC (4)/VEXTSUC (5)	No change	No change	No change	No change	No change
V2O (4) /VEXTO (5)	0	No change	No change	No change	No change	No change
V2OE (4) /VEXTOE (5)	0	No change	No change	No change	No change	No change
V2S (4) /VEXTS (5)	00	Actual state	Actual state	Actual state	Actual state	Actual state
V2SUC (4) /VEXTSUC (5)	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
V2U (4)/ VEXTU (5)	0	No change	No change	No change	No change	No change
V2UE (4)/ VEXTUE (5)	0	No change	No change	No change	No change	No change
WDF	0	No change	No change	No change	No change	No change
WDS	0	Actual state	Actual state	Actual state	Actual state	Actual state

Symbol	Off (power-on default)	Standby	Normal (1)	Sleep	Overtempt	Reset
WMC	(6)	No change	No change	No change	No change	(6)
WPE	0	No change	No change	No change	No change	No change
WPF	0	No change	No change	No change	No change	No change
WPR	0	No change	No change	No change	No change	No change
WPFE	0	No change	No change	No change	No change	No change
WPRE	0	No change	No change	No change	No change	No change
WPVS	0	No change	No change	No change	No change	No change
WRCNTS	Actual state	Actual state	Actual state	Actual state	Actual state	Actual state

(1) Exceptions apply for Forced Normal mode (FNMC = 1).

(2) SIT1169QTK/F, SIT1169QTK/F/3, and SIT1169QTK/X/F only.

(3) Fixed at 00 in SIT1169QTK/3 and SIT1169QTK/F/3.

(4) SIT1169QTK, SIT1169QTK/3, SIT1169QTK/F and SIT1169QTK/F/3 only.

(5) SIT1169QTK/X and SIT1169QTK/X/F only.

(6) 001 if SDMC = 1; otherwise 010.

STATIC CHARACTERISTICS

Tvj = -40°C to +150°C; V_{BAT} = 2.8 V to 28 V; V_{CAN} = V_{V1} (SIT1169QTK/X, SIT1169QTK/X/F); V_{CAN} = V_{V2} (SIT1169QTK, SIT1169QTK/3, SIT1169QTK/F, SIT1169QTK/F/3); R_L= $R_{(CANH-CANL)}$ = 60Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified (1).

PIN BAT CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{BAT}	BAT supply current	Normal mode; MC = 111; CAN Active mode				
		CAN recessive; V_{TXD} = V_{V1}		4.3	7.5	mA
		CAN dominant; V_{TXD} = 0 V		43	60	mA
		Sleep mode; MC = 001; CAN Offline mode; V2/VEXT off; V_{BAT} = 7V to 18 V; -40 ºC < T_j < 85 ºC;		32	65	µA
		Standby mode; MC = 100; CAN Offline mode; V2/VEXT off I_{V1} = 0µA; V_{BAT} = 7 V to 18 V; -40 ºC < T_j < 85 ºC		105	180	µA
		Additional current with V2 on (V2C=01/10/11); I_{VEXT}=0µA; V_{BAT}=7V to 18V; -40 ºC < T_j < 85 ºC		8	32	µA
		Additional current with VEXT on (VEXTC=01/10/11); I_{VEXT}=0µA; V_{BAT}=7V to 18V; -40 ºC < T_j < 85 ºC		40	70	µA
		Additional current in CAN Offline Bias mode; -40 ºC < T_j < 85 ºC		25	50	µA
		Additional current in CAN Offline Bias mode with partial networking active; Standby or Sleep mode; -40 ºC < T_j < 85 ºC (2)		0.4	0.7	mA
		additional current from WAKE input WPRE = WPFE = 1； -40 ºC < T_j < 85 ºC		3	6	µA
$V_{th(det)pon}$	Power-on detection threshold voltage	V_{BAT} rising	4.1		4.6	V
$V_{th(det)poff}$	Power-off detection threshold voltage	V_{BAT} falling	2.8		3.3	V

PIN V1 CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_O	Output voltage	$V_{O(V1)nom}$ = 5 V; (2) V_{BAT} = 5.85 V to 28V; I_{V1} = -200 mA to 0 mA	4.9	5	5.1	V
		$V_{O(V1)nom}$ = 5 V; V_{BAT} = 6 V to 28 V; I_{V1} = -250 mA to 0 mA	4.9	5	5.1	V
		$V_{O(V1)nom}$ = 5 V; V_{BAT} below $V_{th(det)poff}$ and rising; $t < t_{startup}$; T_j < 125 ºC			5.5	V
		$V_{O(V1)nom}$ = 3.3 V; V_{BAT}=4.15V to 28V; I_{V1} = -200 mA to 0 mA	3.234	3.3	3.366	V
		$V_{O(V1)nom}$ = 3.3 V; V_{BAT}=4.3V to 28V; I_{V1} = -250 mA to 0 mA	3.234	3.3	3.366	V
$V_{ret(RAM)}$	RAM retention voltage difference	Between V_{BAT} and V_{V1}; 5V variants only				
		V_{BAT} = 2 V to 3 V; I_{V1} = -2 mA			100	mV
		V_{BAT} = 2 V to 3 V; (2) I_{V1} = -200 µA			10	mV
V_{drop}	Difference between V_{BAT} and V_{V1}	I_{V1}=-250mA			1000	mV
V_{uvd}	Undervoltage detection voltage	5V variants				
		$V_{uvd(nom)}$ = 90%	4.5		4.75	V
		$V_{uvd(nom)}$ = 80%	4		4.25	V
		$V_{uvd(nom)}$ = 70%	3.5		3.75	V
		$V_{uvd(nom)}$ = 60%	3		3.25	V
		3.3V variants				
		$V_{uvd(nom)}$ = 90%	2.97		3.315	V
V_{uvr}	Undervoltage recovery voltage	5V variants (90%)	4.5		4.75	V
		3.3V variants (90%)	2.97		3.135	V
$I_{O(sc)}$	Short-circuit output current		-600		-250	mA
$I_{DD(CAN)intV1}$	Internal CAN supply current from V1	Normal mode; MC = 111; CAN Active mode; CAN dominant; TXD=0V; Short-circuit on bus lines; -3V < (V_{CANH} = V_{CANL}) < +18V			95	mA

PIN VEXCTRL CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
PNP base						
$I_{O(SC)}$	Short-circuit output current	$V_{VEXCTRL} \geq$ -4.5V; V_{BAT}=7V to 28V	1.5	2.5	4	mA
$I_{th(act)PNP}$	PNP activation threshold current	Load current increasing; external PNP transistor connected				
		PDC 0			160	mA
		PDC 0; T_j=150°C (2)	50	80	140	mA
		PDC 1			120	mA
		PDC 1; T_j=150°C (2)	30	50	90	mA
$I_{th(deact)PNP}$	PNP deactivation threshold current	Load current falling; external PNP transistor connected				
		PDC 0			120	mA
		PDC 0; T_j=150°C (2)	30	45	90	mA
		PDC 1			80	mA
		PDC 1; T_j=150°C (2)	10	20	40	mA
$V_{th(Ictrl)PNP}$	PNP current control threshold voltage	rising edge on pin BAT	5.9		7.5	V
PNP collector						
$V_{th(act)Ilim}$	Current limiting activation threshold voltage	Measured across resistor connected between pins VEXCC and V1;2V≤V_{V1}≤5.5V;7V<V_{BAT}<28V	240		550	mV

PIN V2 CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_{BAT}=6V to 28V I_{V2}=-100mA to 0mA	4.9	5	5.1	V
$V_{th(uvp)}$	Undervoltage protection threshold voltage	Detection and recovery thresholds	4.5		4.75	V
$V_{th(ovp)}$	Overvoltage protection threshold voltage	Detection and recovery thresholds	5.2		5.5	V
V_{drop}	Difference between V_{BAT} and V_{V2}	I_{V2}=-100mA			1000	mV
$I_{O(sc)}$	Short-circuit output current		-350		-100	mA
$I_{DD(CAN)intV2}$	Internal CAN supply current from V2	Normal mode; MC=111; CAN Active mode; CAN dominant; V_{TXD}=0V; short-circuit on bus lines; -3V<(V_{CANH}=V_{CANL})<18V			95	mA

PIN VEXT CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_O	output voltage	V_{BAT} = 7V to 28V; I_{VEXT}=-100mA to 0mA	4.9	5	5.1	V
$V_{th(uvp)}$	Undervoltage protection threshold voltage	Detection and recovery thresholds	4.5		4.75	V
$V_{th(ovp)}$	Overvoltage protection threshold voltage	Detection and recovery thresholds	5.2		5.5	V
V_{drop}	Difference between V_{BAT} and V_{VEXT}	I_{VEXT}=-100mA			2000	mV
$I_{O(sc)}$	Short-circuit output current		-350		-100	mA

PIN LIMP CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_O	Output voltage	I_{LIMP}=0.8mA; LHC=1; T_j=-40°C to $T_{th(act)otp(max)}$			0.4	V
I_{LO}	Output leakage current	VLIMP = 0 V to 28 V; LHC = 0	-5		5	µA

PIN SDI/SCK/SCSN CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{th(sw)}$	Switching threshold voltage		0.25V_{V1}		0.75 V_{V1}	V
$V_{th(sw)hys}$	Switching threshold voltage hysteresis		0.05 V_{V1}			V
$R_{pd(SCK)}$	Pull-down resistance on pin SCK		40	60	80	kΩ
$R_{pu(SCSN)}$	Pull-up resistance on pin SCSN		40	60	80	kΩ
$R_{pd(SDI)}$	Pull-down resistance on pin SDI	SDI < $V_{th(sw)}$	40	60	80	kΩ
$R_{pu(SDI)}$	Pull-up resistance on pin SDI	SDI > $V_{th(sw)}$	40	60	80	kΩ
C_i	Input capacitance	V_i=V_{V1} (2)		3	6	pF

PIN SDO CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OH}	HIGH-level output volatge	I_{OH} = -4 mA	V_{V1}-0.4			V
V_{OL}	LOW-level output volatge	I_{OL} = 4 mA			0.4	V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$I_{LO(off)}$	Off-state output leakage current	SCSN = V_{VI}; SDO = 0 V or V_{VI}	-5		5	µA
C_O	Output capacitance	SCSN=V_{VI} (2)		3	6	pF

PIN TXD CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{th(sw)}$	Switching threshold voltage		0.25 V_{VI}		0.75 V_{VI}	V
$V_{th(sw)hys}$	Switching threshold voltage hysteresis		0.05 V_{VI}			V
R_{pu}	Pull-up resistance		40	60	80	kΩ

PIN RXD CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = -4 mA	V_{VI}-0.4			V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA			0.4	V
R_{pu}	Pull-up resistance	CAN Offline mode	40	60	80	kΩ

PIN WAKE CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{th(sw)r}$	Rising switching threshold voltage		2.8		4.1	V
$V_{th(sw)f}$	Falling switching threshold voltage		2.4		3.75	V
$V_{hys(i)}$	Input hysteresis voltage		250		800	mV
I_i	Input current	T_j = -40 ºC to +85 ºC			1.5	µA

PIN CANH/CANL CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{O(dom)}$	Dominant output voltage	CAN Active mode; TXD = 0 V				
		Pin CANH; R_L=50Ω to 65Ω	2.75	3.5	4.5	V
		Pin CANL; R_L=50Ω to 65Ω	0.5	1.5	2.25	V
$V_{dom(TX)sym}$	Transmitter dominant voltage symmetry	$V_{dom(TX)sym}$ = V_{CAN} - V_{CANH} -V_{CANL}; V_{CAN} = 5 V	-400		400	mV
V_{TXsym}	Transmitter voltage symmetry	V_{TXsym} = V_{CANH} + V_{CANL}; (2) f_{TXD} = 250 kHz, 1MHz or 2.5MHz; (3) C_{SPLIT} = 4.7nF; V_{CAN} = 4.75 V to 5.25 V	0.9V_{CAN}		1.1V_{CAN}	V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{O(dif)}$	Differential output voltage	CAN Active mode (dominant); TXD = 0 V; V_{CAN} = 4.75 V to 5.5 V				
		R_L = 50 Ω to 65Ω	1.5		3	V
		R_L = 45 Ω to 70Ω	1.4		3.3	V
		R_L = 2240Ω	1.5		5	V
		Recessive; R_L = no load				
		CAN Active / Listen only / Offline bias mode; TXD = V1	-50		50	mV
		CAN Offline mode	-0.2		0.2	V
$V_{O(rec)}$	Recessive output voltage	CAN Active mode; TXD = V1; R_L = no load	2	0.5V_{CAN}	3	V
		CAN Offline mode; R_L = no load	-0.1	0	0.1	V
		CAN Listen only / Offline bias mode; R_L= no load	2	2.5	3	V
$I_{O(sc)dom}$	Dominant short-circuit output current	CAN Active mode; TXD = 0 V; V_{CAN} = 5 V				
		Pin CANH; -3 V < V_{CANH} < +27 V	-115			mA
		Pin CANL; -15 V < V_{CANL} < +18 V			115	mA
$I_{O(sc)rec}$	Recessive short-circuit output current	V_{CANL} = V_{CANH} = -27 V to +32 V; TXD = V1	-3		3	mA
$V_{th(RX)dif}$	Differential receiver threshold voltage	-12 V < V_{CANL} < +12 V; -12 V < V_{CANH} < +12 V				
		CAN Active / Listen only modes	0.5	0.7	0.9	V
		CAN Offline mode	0.4	0.7	1.15	V
$V_{rec(RX)}$	Receiver recessive voltage	-12 V < V_{CANL} < +12 V; -12 V < V_{CANH} < +12 V				
		CAN Active / Listen only modes	-4[2]		0.5	V
		CAN Offline / Offline bias modes	-4[2]		0.4	V
$V_{dom(RX)}$	Receiver dominant voltage	-12 V < V_{CANL} < +12 V; -12 V < V_{CANH} < +12 V				
		CAN Active / Listen only modes	0.9		9.0[2]	V
		CAN Offline / Offline bias modes	1.15		9.0[2]	V
$V_{th(RX)dif(hys)}$	Differential receiver threshold voltage hysteresis	CAN Active / Listen only mode; -12 V < V_{CANL} < +12 V; -12 V < V_{CANH} < +12 V	70	130	200	mV
R_i	Input resistance	-2 V < V_{CANL} < +7 V; -2 V < V_{CANH} < +7 V	25	40	55	kΩ

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ΔR_i	Input resistance deviation	0 V < V_{CANL} < +5 V; 0 V < V_{CANH} < +5 V	-1		1	%
$R_{i(dif)}$	Differential input resistance	-2 V < V_{CANL} < +7 V; -2 V < V_{CANH} < +7 V	60	80	100	kΩ
$C_{i(cm)}$	Common-mode input capacitance	(2)			40	pF
$C_{i(dif)}$	Differential input capacitance	(2)			20	pF
I_L	Leakage current	V_{BAT}=V_{CAN}=0V or V_{BAT}=V_{CAN}=shorted to ground via 47kΩ V_{CANH} = V_{CANL} = 5 V	-5		5	μA
$V_{uvd(CAN)}$	CAN undervoltage detection voltage	On pin BAT; V_{BAT} falling	4.2		4.55	V
		At V_{CAN};	4.5		4.75	V
$V_{uvr(CAN)}$	CAN undervoltage recovery voltage	V_{BAT} Rising	4.5		5	V
		On V_{CAN};	4.5		4.75	V
$I_{DD(CAN)}$	CAN supply current	CAN Active mode; (4) CAN recessive; TXD = V_1	2.5	4.3	6	mA
		CAN Active mode; (4) CAN dominant; TXD = 0 V; R_L= no load	2.5	4.5	6	mA

PIN RSTN CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OL}	LOW-level output voltage	V_{V1} = 1.0 V to 5.5 V; Pull-up resistor to V1 > 900 Ω	0		0.2V_{V1}	V
R_{pu}	Pull-up resistance		40	60	80	kΩ
$V_{th(sw)}$	Switching threshold voltage		0.25V_{V1}		0.75V_{V1}	V
$V_{th(sw)hys}$	Switching threshold voltage hysteresis		0.05V_{V1}			V

OVERTEMPERATURE PROTECT

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$T_{th(act)otp}$	Overtemperature protection activation threshold temperature	(2)	160	177	195	ºC
$T_{th(rel)otp}$	Overtemperature protection release threshold temperature	(2)	120	137	155	ºC
$T_{th(warn)otp}$	Overtemperature protection warning threshold temperature	(2)	120	137	155	ºC

MTP CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$N_{cy(W)MTP}$	Number of MTP write cycles	V_{BAT} = 6 V to 28 V; T_j = 0 ºC to +125 ºC			200	-

(1)All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

(2) Not tested in production; guaranteed by design.

(3)The test circuit used to measure the bus output voltage symmetry (which includes CSPLIT).

(4) From V1 in VEXT versions (SIT1169QTK/X and SIT1169QTK/X/F) and from V2 in other variants.

DYNAMIC CHARACTERISTICS

Tvj = -40°C to +150°C; V_{BAT} = 2.8 V to 28 V; V_{CAN} = V_{V1} (SIT1169QTK/X, SIT1169QTK/X/F); V_{CAN} = V_{V2} (SIT1169QTK, SIT1169QTK/3, SIT1169QTK/F, SIT1169QTK/F/3); R_L= $R_{(CANH-CANL)}$ = 60Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified(1).

PIN V1 TIMING CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{startup}$	Start-up time	From V_{BAT} exceeding the power-on detection threshold until V1 exceeds the 90% undervoltage threshold; C_{V1} = 4.7µF		2.8	4.7	ms
$t_{d(uvd)}$	Undervoltage detection delay time	V1 falling		1		ms
$t_{d(uvd-RSTNL)}$	Delay time from undervoltage detection to RSTN LOW	Undervoltage on V1			63	µs

PIN V2/VEXT TIMING CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{d(uvd)}$	Undervoltage detection delay time	V_{V2}/V_{VEXT} falling	6		32	µs
		At start-up of V_{V2}/V_{VEXT}	2.2	2.5	2.8	ms
$t_{d(ovd)}$	Overvoltage detection delay time	V_{V2}/V_{VEXT} falling	6		32	µs

PINS SCSN/SCK/SDI/SDO TIMING CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{cy(clk)}$	Clock cycle time		250			ns
$t_{SPILEAD}$	SPI enable lead time		50			ns
t_{SPILAG}	SPI enable lag time		50			ns
$t_{clk(H)}$	Clock HIGH time		100			ns
$t_{clk(L)}$	Clock LOW time		100			ns
$t_{su(D)}$	Data input set-up time		50			ns
$t_{h(D)}$	Data input hold time		50			ns
$t_{v(Q)}$	Data output valid time	Pin SDO; C_L = 20 pF			50	ns
$t_{d(SDI-SDO)}$	SDI to SDO delay time	SPI address bits and read-only bit; C_L = 20 pF			50	ns
$t_{WH(S)}$	Chip select pulse width HIGH	Pin SCSN	2			µs

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{d(SCKL-SCSNL)}$	Delay time from SCK LOW to SCSN LOW		50			ns

PINS CANH/CANL/TXD/RXD TIMING CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{d(TXD-busdom)}$	Delay time from TXD to bus dominant			45		ns
$t_{d(TXD-busrec)}$	Delay time from TXD to bus recessive			45		ns
$t_{d(busdom-RXD)}$	Delay time from bus dominant to RXD			60		ns
$t_{d(busrec-RXD)}$	Delay time from Bus recessive to RXD			60		ns
$t_{d(TXDL-RXDL)}$	Delay time from TXD LOW to RXD LOW	$t_{bit(TXD)}$=200ns			255	ns
$t_{d(TXDH-RXDH)}$	Delay time from TXD HIGH to RXD HIGH	$t_{bit(TXD)}$=200ns			255	ns
$t_{bit(bus)}$	Transmitted recessive bit width	$t_{bit(TXD)}$=500ns	435		530	ns
		$t_{bit(TXD)}$=200 ns	155		210	ns
$t_{bit(RXD)}$	Bit time on pin RXD	$t_{bit(TXD)}$=500 ns	400		550	ns
		$t_{bit(TXD)}$=200 ns	120		220	ns
Δt_{rec}	Receiver timing symmetry	$t_{bit(TXD)}$=500 ns	-65		40	ns
		$t_{bit(TXD)}$=200 ns	-45		15	ns
$t_{wake(busdom)}$	Bus dominant wake-up time	First pulse (after first recessive) for wake-up on pins CANH and CANL; CAN Offline mode	0.5		1.8	µs
		Second pulse for wake-up on pins CANH and CANL	0.5		1.8	µs
$t_{wake(busrec)}$	Bus recessive wake-up time	First pulse for wake-up on pins CANH and CANL; CAN Offline mode	0.5		1.8	µs
		Second pulse (after first dominant) for wake-up on pins CANH and CANL	0.5		1.8	µs
$t_{to(wake)bus}$	Bus wake-up time-out time	Between first and second dominant pulses; CAN Offline mode	0.8		10	ms
$t_{to(dom)TXD}$	TXD dominant time-out time	CAN Active mode; TXD=0V	2.7		3.3	ms

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{to(silence)}$	Bus silence time-out time	Recessive time measurement started in all CAN modes	0.95		1.17	s
$t_{d(busact-bias)}$	Delay time from bus Active to Bias				200	μs
$t_{startup(CAN)}$	CAN start-up time	to CTS = 1; when switching to Active mode			220	μs

CAN PARTIAL NETWORKING

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$N_{bit(idle)}$	Number of idle bits	Before a new SOF is accepted CFDC=1 (2)	6		10	
$t_{fltr(bit)dom}$	Dominant bit filter time	Arbitration data rate ≤ 500kbit/s; CFDC=1 (2)	5		17.5	%

PIN RXD TIMING CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{d(event)}$	Event capture delay time	CAN Offline mode	0.9		1.1	ms
t_{blank}	Blanking time	When switching from Offline to Active/Listen-only mode			25	μs

WATCHDOG TIMING CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{trig(wd)1}$	Watchdog trigger time 1	Normal mode; watchdog Window mode only	0.45*NWP		0.55*NWP	ms
$t_{trig(wd)2}$	Watchdog trigger time 2	Normal/Standby mode	0.9*NWP		1.11*NWP	ms
$t_{d(SCSNH-RSTNL)}$	Delay time from SCSN HIGH to RSTN LOW	Rising edge to falling edge; watchdog in window mode, triggered in the first half of the watchdog period (before $t_{trig(wd)1}$) (2)			0.2	ms

PIN RSTN TIMING CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{w(rst)}$	Reset pulse width	Output pulse width				
		RLC=00	20		25	ms
		RLC=01	10		12.5	ms
		RLC=10	3.6		5	ms
		RLC=11	1		1.5	ms
		Input pulse width	18			μs

PIN LIMP TIMING CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{d(limp)}$	Limp delay time		117		145	ms

PIN WAKE TIMING CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{wake}	Wake-up time		50			μs

MTP TIMING CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{d(MTPNV)}$	MTPNV delay time	Before factory presets are restored; V_{BAT} = 6 V to 28 V	0.9		1.1	s
$t_{ret(data)}$	Data retention time	T_j=150ºC	10			year
$t_{prog(MTPNV)}$	MTPNV programming time	Correct CRC code received at address 075h; V_{BAT} = 6V to 28V	10	12	14	ms

MODE TRANSITIONS TIMING CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{d(act)norm}$	Normal mode activation delay time	MC=111; Delay before CAN is activated after the SBC switches to Normal mode			320	μs

(1) All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

(2) Not tested in production; guaranteed by design.

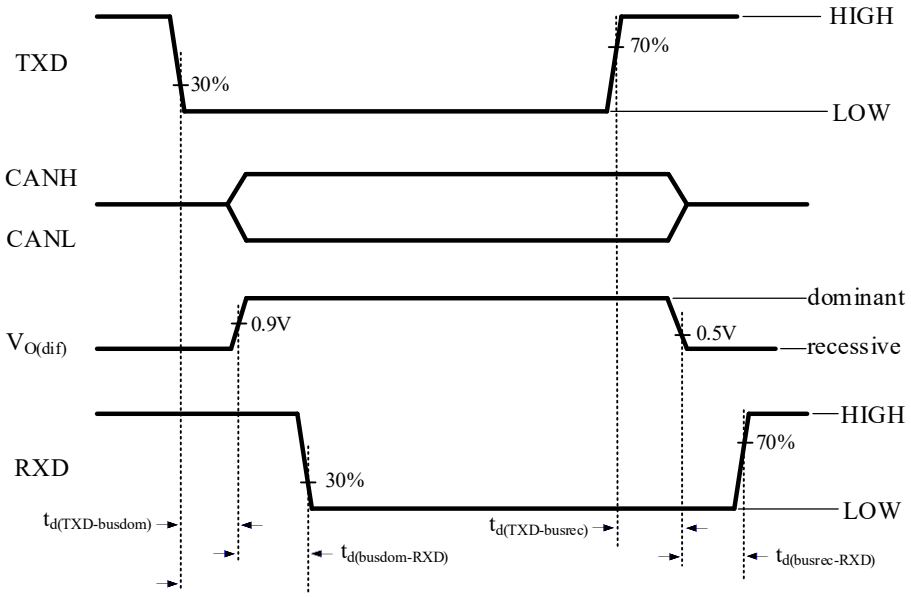


Figure 17 CAN transceiver timing diagram

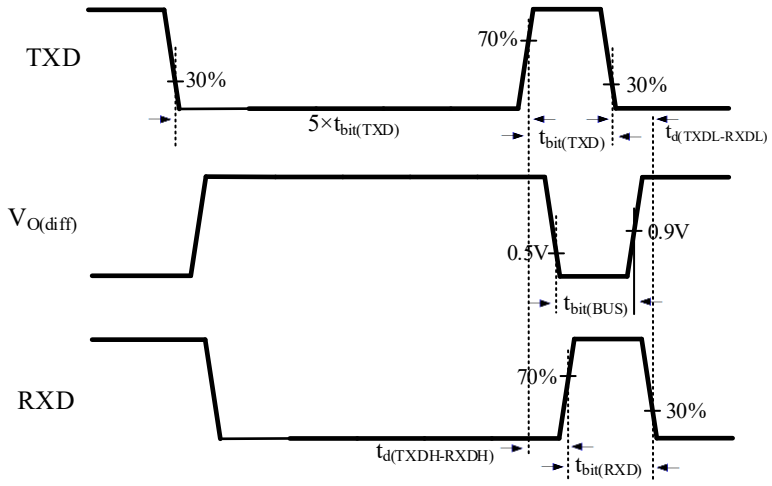
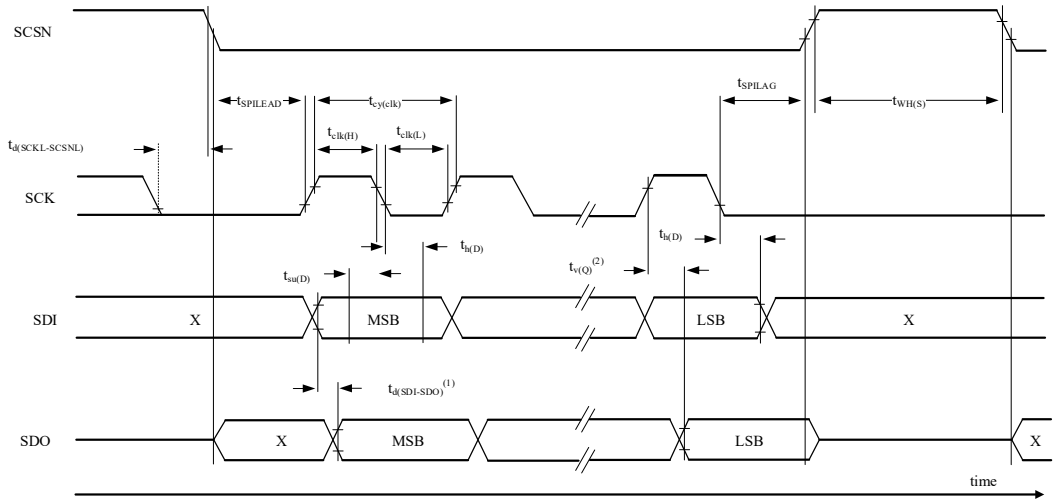


Figure 18 CAN FD timing definitions according to ISO 11898-2:2016



（1）The SDI-to-SDO delay time is valid for SPI address bits and the read-only bit.
（2）The data output valid time is valid for the SPI data bits.

Figure 19 SPI timing diagram

APPLICATION INFORMATION

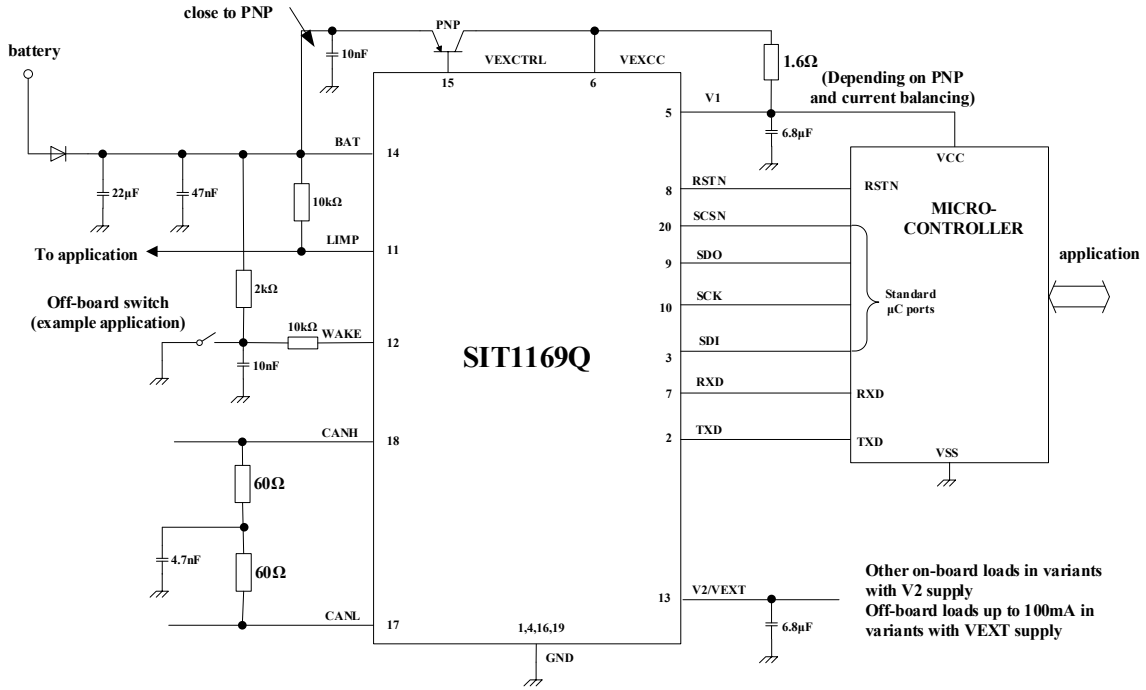


Figure 20 SIT1169Q Typical Application Diagram

APPLICATION HITS

Further information on the application of the SIT1169Q can be found in the SIT application hints document.

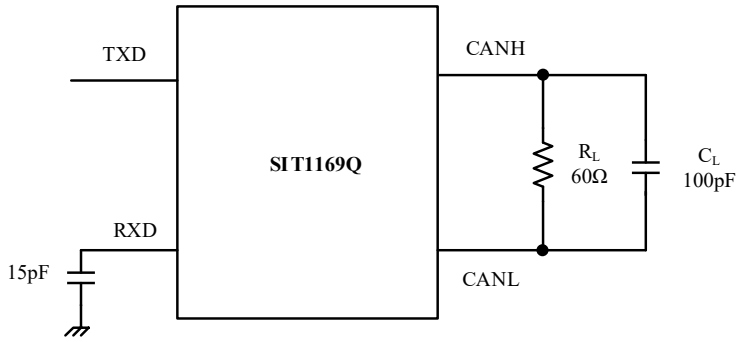


Figure 21 Timing test circuit for CAN transceiver

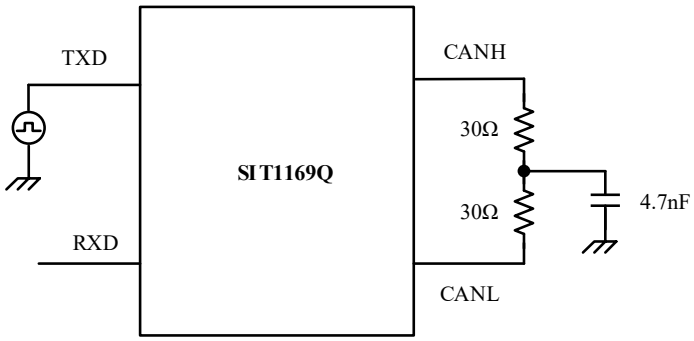
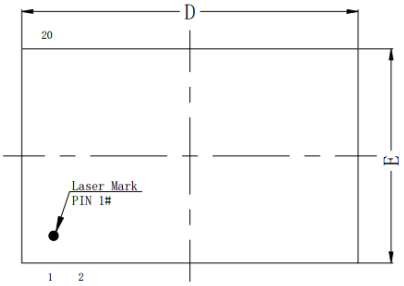


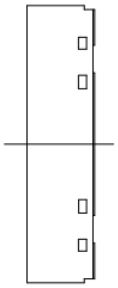
Figure 22 Test circuit for measuring transceiver driver symmetry

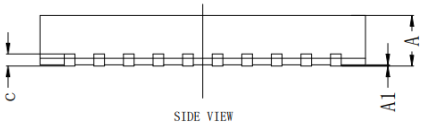
DFN20 DIMENSIONS

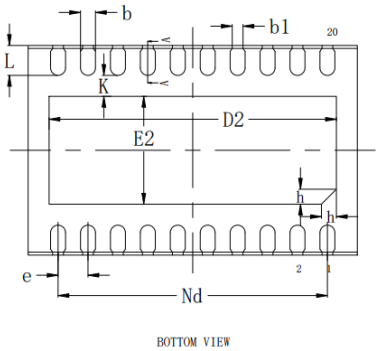
Package size

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
b1		0.18REF	
c		0.203REF	
D	5.40	5.50	5.60
D2	4.70	4.80	4.90
e		0.50BSC	
Nd		4.50BSC	
E	3.40	3.50	3.60
E2	1.70	1.80	1.90
L	0.45	0.50	0.55
h	0.20	0.25	0.30
K		0.35REF	

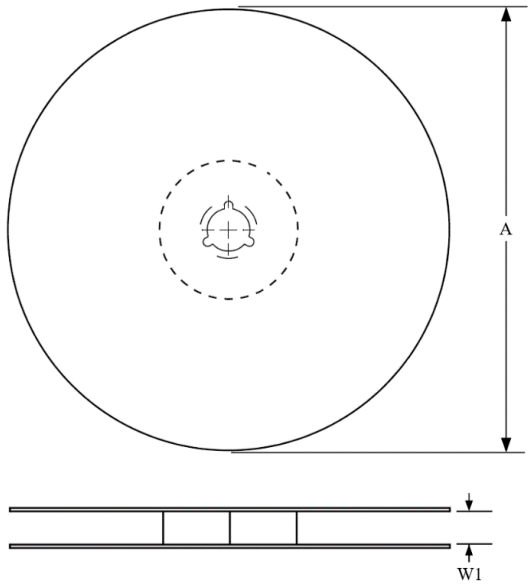




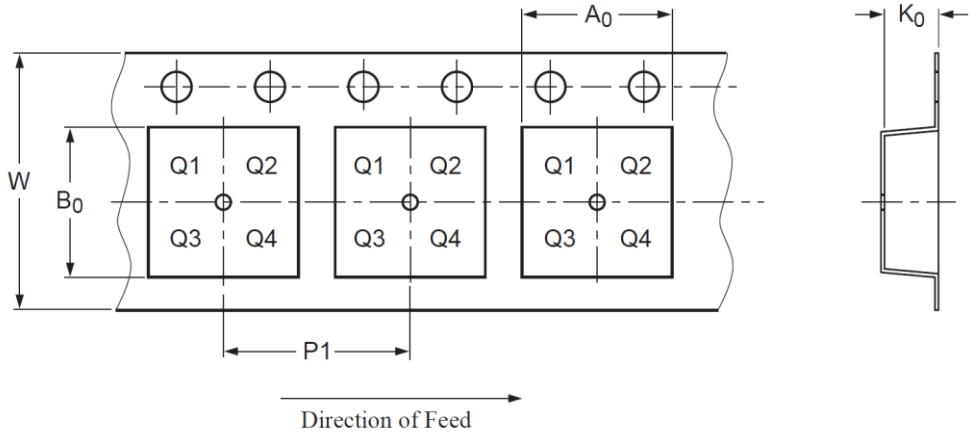




TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



PIN1 is in quadrant 1

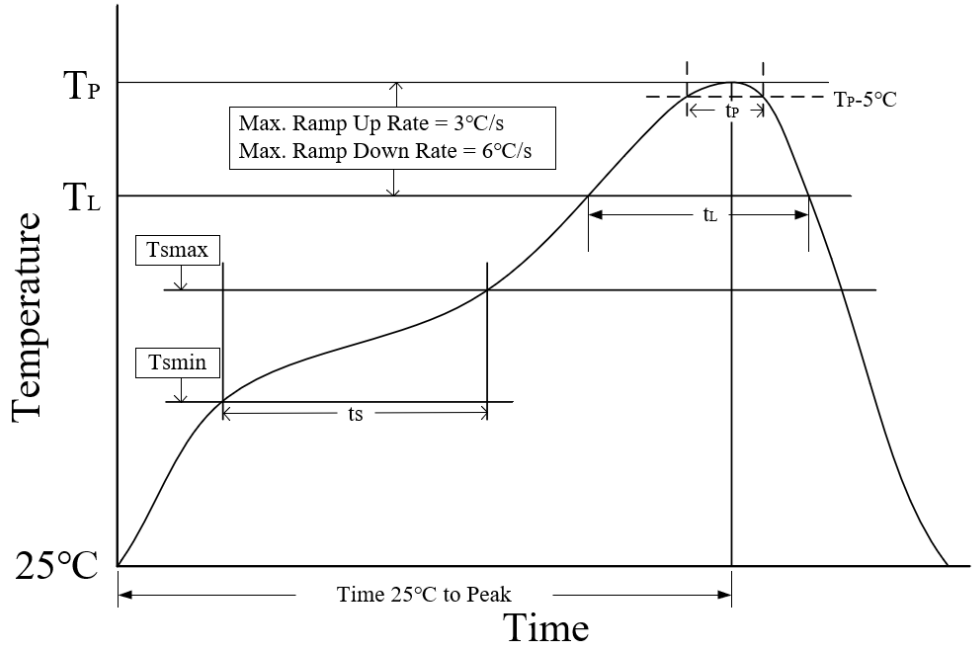
Package Type	Reel Diameter A (mm)	Tape Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
DFN20	329±1	12.8±1	3.80±0.1	5.80±0.10	1.05±0.1	8.00±0.1	12.00±0.30

ORDERING INFORMATION

Type number	Modes			Supplies					Host Interface		Additional Features						Package	MSL	Packing
	Normal and Standby modes	Sleep mode	Reset mode	V1:5V, µC only	V1:5V, µC and CAN	V1:3.3V, µC only	V2:5V, CAN + on-board loads	VEXT: 5V, external loads	SPI: for control and diagnostics	RSTN: reset pin	Watchdog	Local WAKE pin	LIMP pin	Non-volatile memory	CAN partial networking	CAN FD passive			
SIT1169QTK	•	•	•	•			•		•	•	•	•	•	•			DFN20	MSL 1	Tape and reel
SIT1169QTK/X	•	•	•		•			•	•	•	•	•	•	•			DFN20	MSL 1	Tape and reel
SIT1169QTK/F	•	•	•	•			•		•	•	•	•	•	•	•	•	DFN20	MSL 1	Tape and reel
SIT1169QTK/X/F	•	•	•		•			•	•	•	•	•	•	•	•	•	DFN20	MSL 1	Tape and reel
SIT1169QTK/3	•	•	•			•	•		•	•	•	•	•	•			DFN20	MSL 1	Tape and reel
SIT1169QTK/F/3	•	•	•			•	•		•	•	•	•	•	•	•	•	DFN20	MSL 1	Tape and reel

DFN20 is packed with 5000 pieces/disc in braided packaging.

REFLOW SOLDERING



Parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	3 °C/second max
Preheat time ts (T_{smin}=150 °C to T_{smax}=200 °C)	60-120 seconds
Melting time t_L (T_L=217 °C)	60-150 seconds
Peak temp T_P	260-265 °C
5 °C below peak temperature t_P	30 seconds
Ave cooling rate (T_P to T_L)	6 °C/second max
Normal temperature 25°C to peak temperature T_P time	8 minutes max

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Datasheet status	Revision Date
V1.0	Initial version.	2025.08