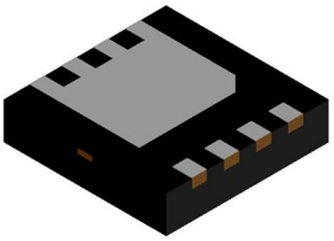
SPM038R0DRA

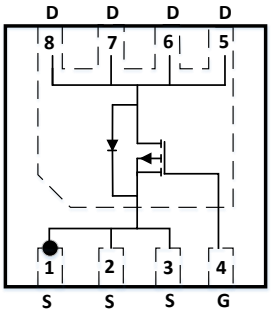
Single P-Channel, -30V, -49A Power MOSFET

http://www.sitcores.com/

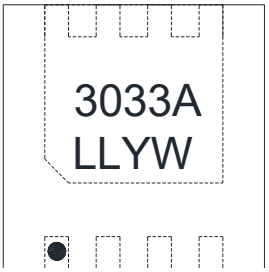
V_{DS} (V)	Max. $R_{DS(on)}$ (mΩ)
-30	8.0 @ V_{GS}=-10V
	13.0 @ V_{GS}=-4.5V



DFN3333-8L



Pin configuration (Top view)



3033A = Device Code
LL = Special Code
Y = Year
W = Week (A~z)

Marking

Description

The SPM038R0DRA is P-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product SPM038R0DRA is in compliance with RoHS.

Features

- Trench Technology
- Supper high density cell design
- Low ON resistance
- Package DFN3333-8L
- 100% UIS and Rg Tested
- MSL3

Applications

- DC/DC converters
- Power supply converters circuit
- Power Switching for portable device

Order information

Device	Package	Shipping
SPM038R0DRA-8/TR	DFN3333-8L	3000/Tape&Reel

Absolute Maximum ratings

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±25	
Continuous Drain Current [d]	T_C=25°C	I_D	-49	A
	T_C=100°C		-42	A
Pulsed Drain Current [c]		I_{DM}	-166	A
Continuous Drain Current	T_A=25°C	I_{DSM}	-21	A
	T_A=70°C		-17	
Avalanche Energy L=0.3mH		E_{AS}	87	mJ
Power Dissipation [b]	T_C=25°C	P_D	54	W
	T_C=100°C		22	
Power Dissipation [a]	T_A=25°C	P_{DSM}	5.4	W
	T_A=70°C		3.5	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature Range		T_{STG}	-55 to 150	°C

Thermal resistance ratings

Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance [a]	t ≤ 10 s	$R_{\theta JA}$	18.5	23.0	°C/W
	Steady State		42.5	53.0	
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	1.85	2.30	

Note:

a FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) partially covered with copper (645mm^2 area). The power adissipation P_{DSM} is based on Junction-to-Ambient thermal resistance $R_{\theta JA}$ t≤10s value and the $T_{J(MAX)}$=150°C. The value is only for reference, any application depends on the user's specific board design.

b The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in asetting the upper dissipation limit for cases where additional heat sinking is used.

c Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial T_J =25°C, the maximum allowed junction temperature of 150°C.

d The maximum current rating by source bonding technology.

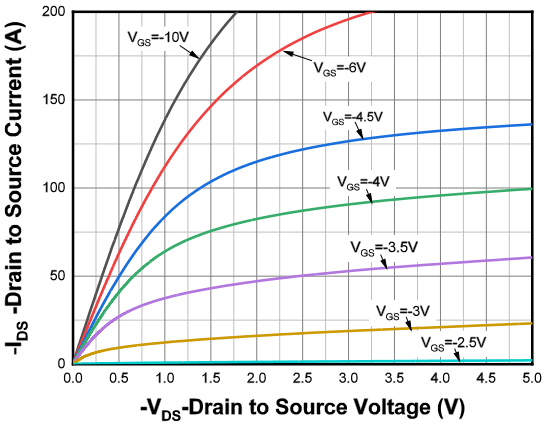
e The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

f The parameter is not subject to production test – verified by design / characterization.

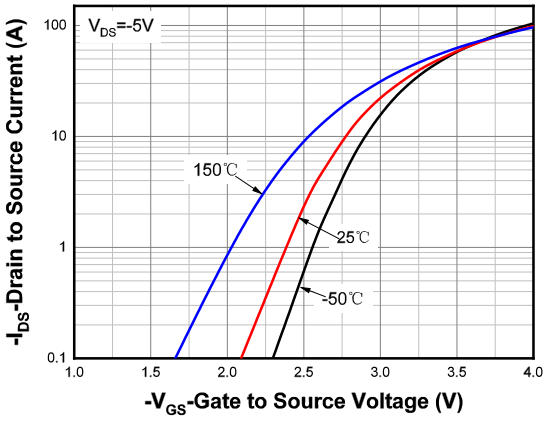
Electronics Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = -250uA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V			-1	uA
Gate-to-source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±25V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = -250uA	-1.2	-1.7	-2.2	V
Drain-to-source On-resistance [e]	$R_{DS(on)}$	V_{GS} = -10V, I_D = -20A		6.5	8.0	mΩ
		V_{GS} = -4.5V, I_D = -16A		9.5	13.0	
CHARGES, CAPACITANCES AND GATE RESISTANCE [f]						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0MHz, V_{DS} = -15 V		2433		pF
Output Capacitance	C_{OSS}			447		
Reverse Transfer Capacitance	C_{RSS}			376		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = -10V, V_{DD} = -15V, I_D = -20 A		51.8		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = -4.5V, V_{DD}= -15V, I_D = -20 A		27.0		
Gate-to-Source Charge	Q_{GS}	V_{GS} = -10V, V_{DD} = -15V, I_D = -20 A		7.2		
Gate-to-Drain Charge	Q_{GD}			13.0		
Gate Resistance	R_g	f=1MHz		7.5		Ω
SWITCHING CHARACTERISTICS [f]						
Turn-On Delay Time	$td_{(ON)}$	V_{GS} = -10V, V_{DD} = -15V, I_D = -20A, R_G= 3Ω		6.3		ns
Rise Time	tr			57.6		
Turn-Off Delay Time	$td_{(OFF)}$			92.1		
Fall Time	tf			53.1		
BODY DIODE CHARACTERISTICS						
Forward Voltage [e]	V_{SD}	V_{GS} = 0 V, I_S = -1A		-0.7	-1.2	V
Maximum Continuous Current [d]	I_S				-49	A
Body Diode Reverse Recovery Time	trr	I_F=-20A, dI/dt=100A/μs		64.5		ns
Body Diode Reverse Recovery Charge	Qrr			52.5		nC

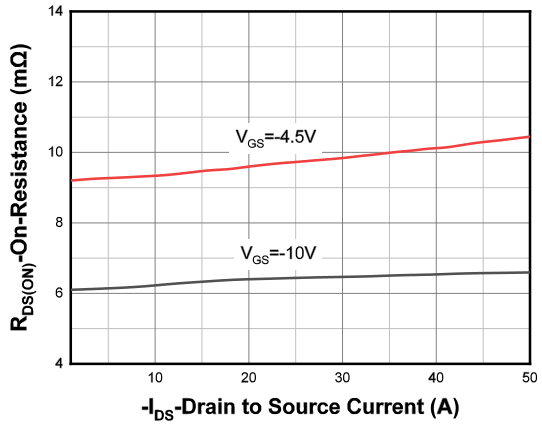
Typical Characteristics (Ta=25°C, unless otherwise noted)



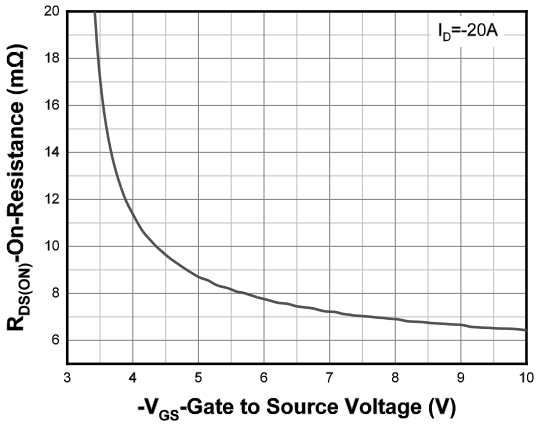
Output Characteristics [e]



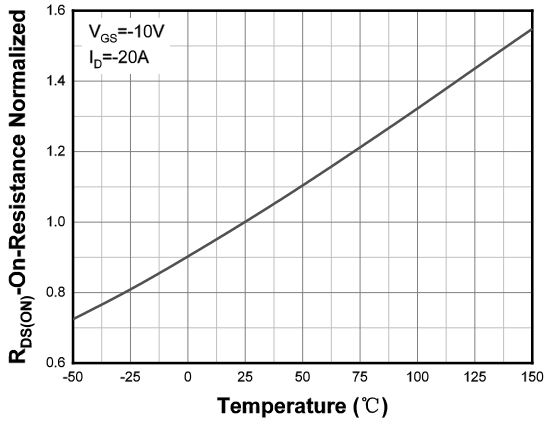
Transfer Characteristics [e]



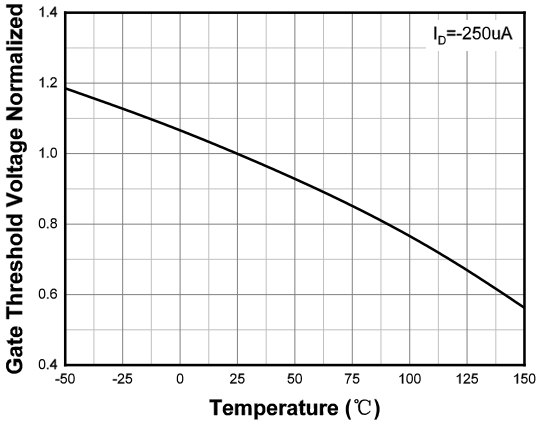
On-Resistance vs. Drain Current [e]



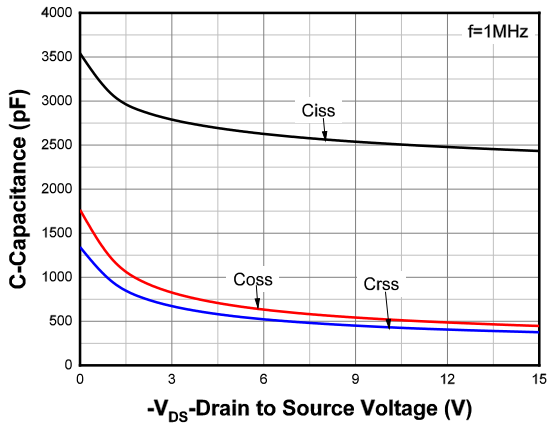
On-Resistance vs. Gate-to-Source Voltage [e]



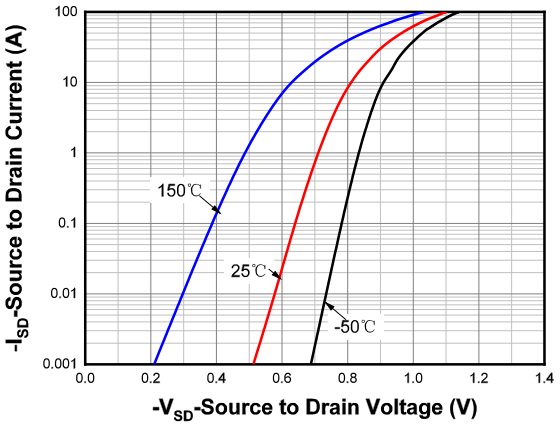
On-Resistance vs. Junction Temperature [e]



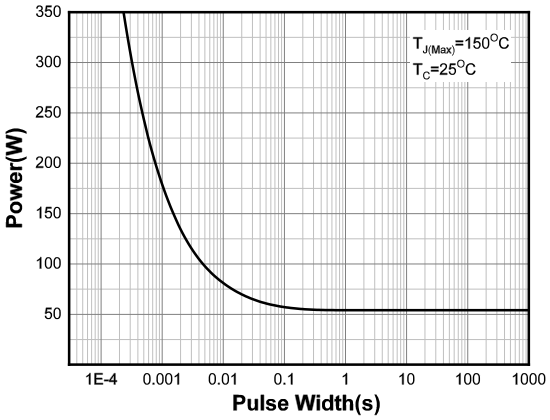
Threshold Voltage vs. Temperature



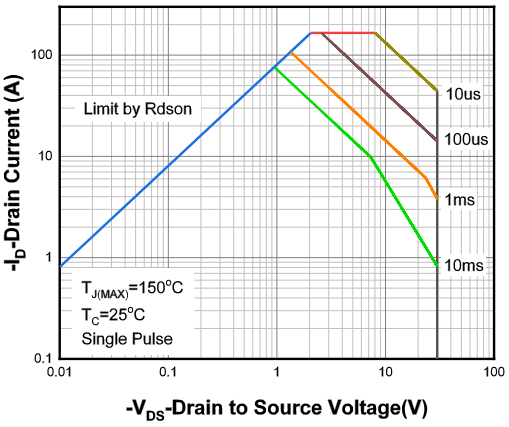
Capacitance



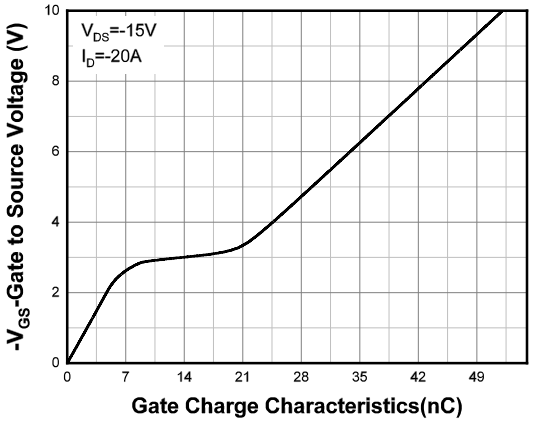
Body Diode Forward Voltage [e]



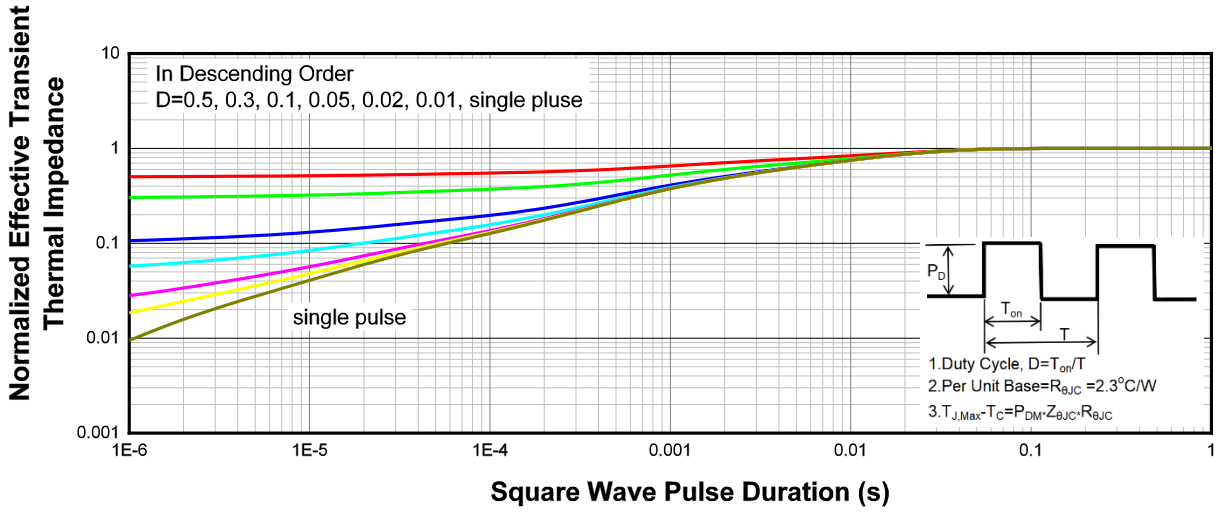
Single Pulse power



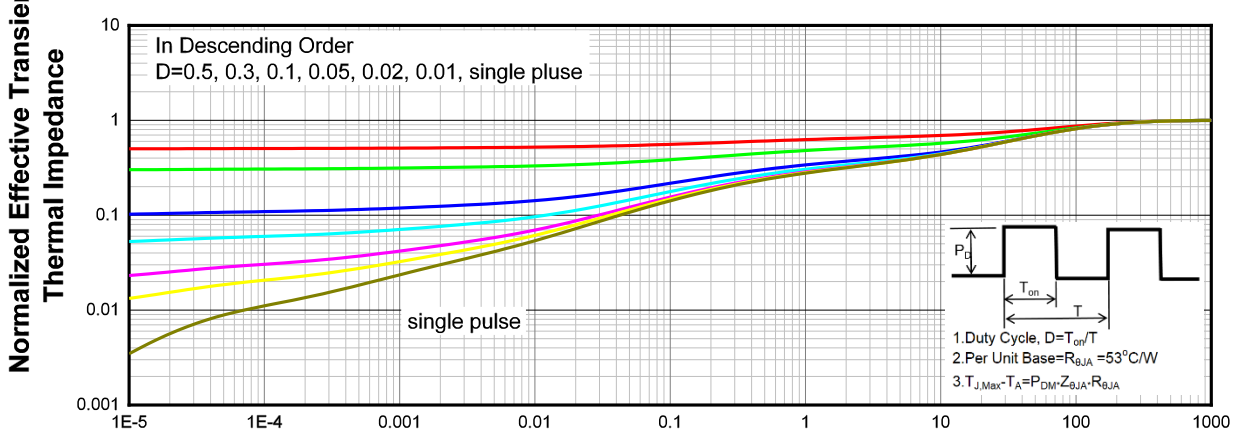
Safe Operating Area



Gate Charge Characteristics



Transient Thermal Response (Junction-to-Case)



Transient Thermal Response (Junction-to-Ambient)

PACKAGE OUTLINE DIMENSIONS

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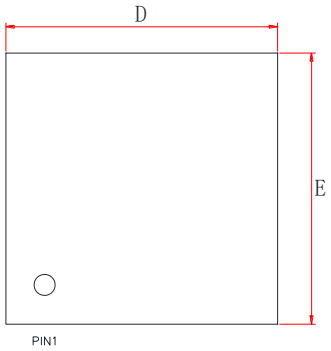
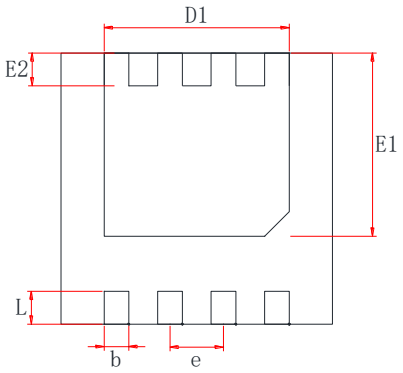
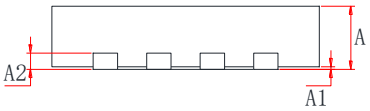


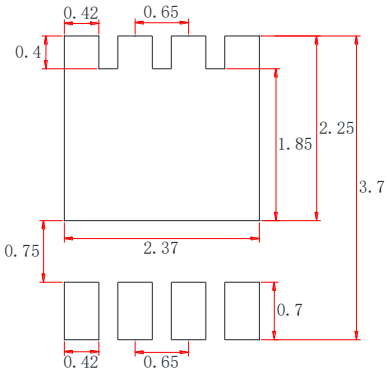
TOP VIEW



BOTTOM VIEW



SIDE VIEW

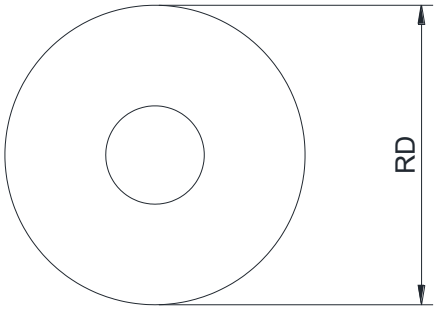


RECOMMENDED LAND PATTERN(unit:mm)

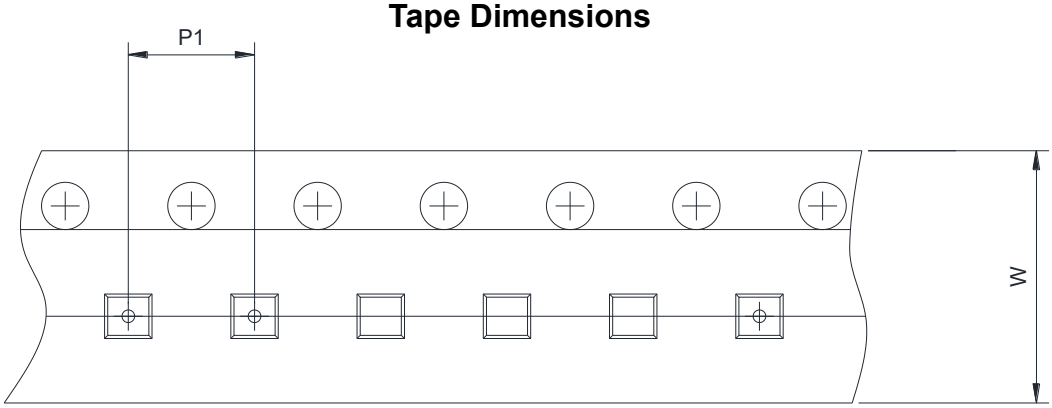
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	-	-	0.05
A2	0.15	0.20	0.25
b	0.24	0.30	0.35
D	3.20	3.30	3.40
D1	2.15	2.25	2.35
E	3.20	3.30	3.40
E1	2.13	2.23	2.33
E2	0.30	0.40	0.50
e	0.65 BSC		
L	0.30	0.40	0.50

TAPE AND REEL INFORMATION

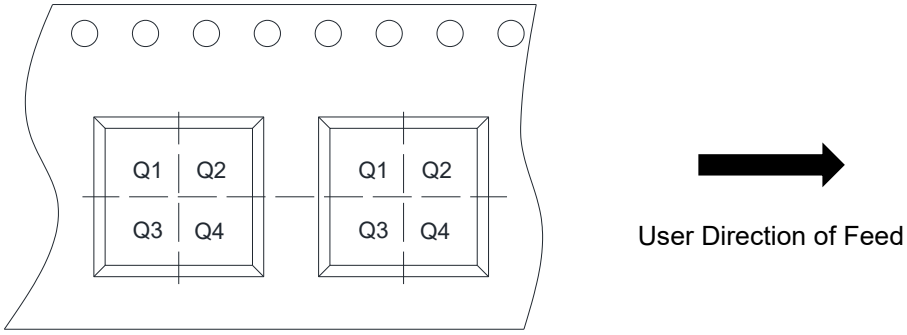
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☐ 7inch ☑ 13inch
W	Overall width of the carrier tape	☐ 8mm ☑ 12mm ☐ 16mm
P1	Pitch between successive cavity centers	☐ 2mm ☐ 4mm ☑ 8mm
Pin1	Pin1 Quadrant	☑ Q1 ☐ Q2 ☐ Q3 ☐ Q4