FEATURES

- Input voltage range: 4V to 40V
- Ultra-low quiescent current: 12μA (disable WDG)
- Low dropout voltage: 280mV @ 300mA
- Maximum output current: 300mA
- Ultra-low power sleep mode
- ±2% accuracy, Fixed 3.3V and 5V version
- Shutdown current: 1μA
- PSRR 66dB @ 100Hz
- Stable loop, requiring only a 4.7μF low-ESR output ceramic capacitor
- Enable (EN) pin with 40V withstand voltage
- Current limit, short-circuit protection
- Ambient temperature: -40℃ to 125℃
- Thermal shutdown and automatic restart recovery
- Integrated soft start
- Configurable for both window watchdog and standard watchdog
- Window ratio can be configured as 1:1 or 8:1
- Adjustable watchdog period (10ms to 500ms)
- 10% accuracy watchdog period
- $\overline{\text{WD\_EN}}$ is dedicated pin for watchdog enable/disable control
- Adjustable PG threshold and PG delay time
- Low input voltage tracking function for UVLO
- PG flag with Programmable Delay, specifically designed for MCU applications
- Available in ETSSOP16 package

DESCRIPTION

The SIT24XX3Q series are watchdog linear regulators (LDO) capable of operating over a wide input voltage range of 4V to 40V. Different models in the series provide fixed output voltages of either 3.3V or 5V, with an output load capability of 300mA. They are suitable for automotive microcontroller or microprocessor power applications.

Under typical application conditions, the quiescent current is only 12μA (with watchdog disabled) under no load, and the typical consumption during sleep mode is only 1μA.

The series also offers programmable options for either a window or standard watchdog function, using an external resistor to set the watchdog period, with an accuracy of <10%.

The PG output of the SIT24XX3Q series can directly drive the reset pin of a microprocessor (MCU). The PG function integrates fixed delay times and rise/fall thresholds. Alternatively, an external capacitor on the DELAY pin can be used to adjust the PG delay time, and voltage divider resistors on PGADJ can adjust the rise/fall thresholds.

The SIT24XX3Q features integrated current limit and over-temperature protection. In the event of an output short-circuit to ground, the output current is clamped to the current limit value. If the temperature exceeds the safe threshold, the integrated protection mechanism shuts down the LDO until the temperature drops to a safe range, after which normal operation resumes.

The SIT24XX3Q series products are offered in an ETSSOP16 package with an enhanced thermal pad.

PIN CONFIGURATION

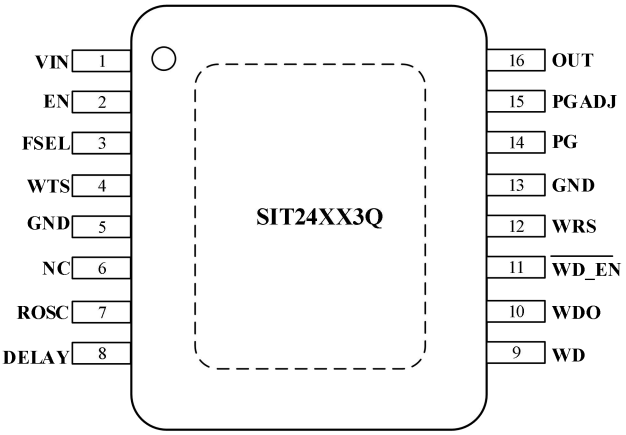


Figure 1 Pin configuration

PIN DESCRIPTION

Pin	Symbol	Pin description
1	VIN	Input Power-supply Voltage Pin.
2	EN	Enable pin, connect to a logic control signal or to VIN directly.
3	FSEL	Internal oscillator frequency selection pin. Pull this pin down to low-level voltage to select the high-frequency oscillator. Pull this pin up to high-level voltage to select the low-frequency oscillator.
4	WTS	Watchdog type-selection pin. To set the window watchdog, connect this pin to the GND pin. To set the standard watchdog, pull this pin high.
5	GND	Ground.
6	NC	No connection.
7	ROSC	Watchdog timer adjustment pin. Connect a resistor between the ROSC pin and the GND pin to set the duration of the watchdog monitor. Leaving this pin open or connecting this pin to ground results in the watchdog reporting a fault at the watchdog output (WDO).
8	DELAY	PG Delay Pin. Connect an external capacitor to ground to adjust the PG delay time.
9	WD	Watchdog Signal Input Pin.
10	WDO	Watchdog Status Pin. Connect an external pull-up resistor to OUT.
11	$\overline{\text{WD\_EN}}$	Watchdog Enable Pin. Active low.
12	WRS	Window Ratio Adjustment Pin (valid only in window watchdog mode). When pulled low, sets the window ratio to 1:1; when pulled high, sets the window ratio to 8:1.
13	GND	Ground.
14	PG	Power Good Pin:Connect an external pull-up resistor to OUT.

Pin	Symbol	Pin description
15	PGADJ	PG Threshold Adjustment Pin. Grounding sets a fixed threshold; connecting a voltage divider chain between OUT and GND to PGADJ adjusts the PG threshold.
16	OUT	Output pin.

Note: ETSSOP16 is recommended that the thermal pad is soldered to board ground.

FUNCTION BLOCK DIAGRAM

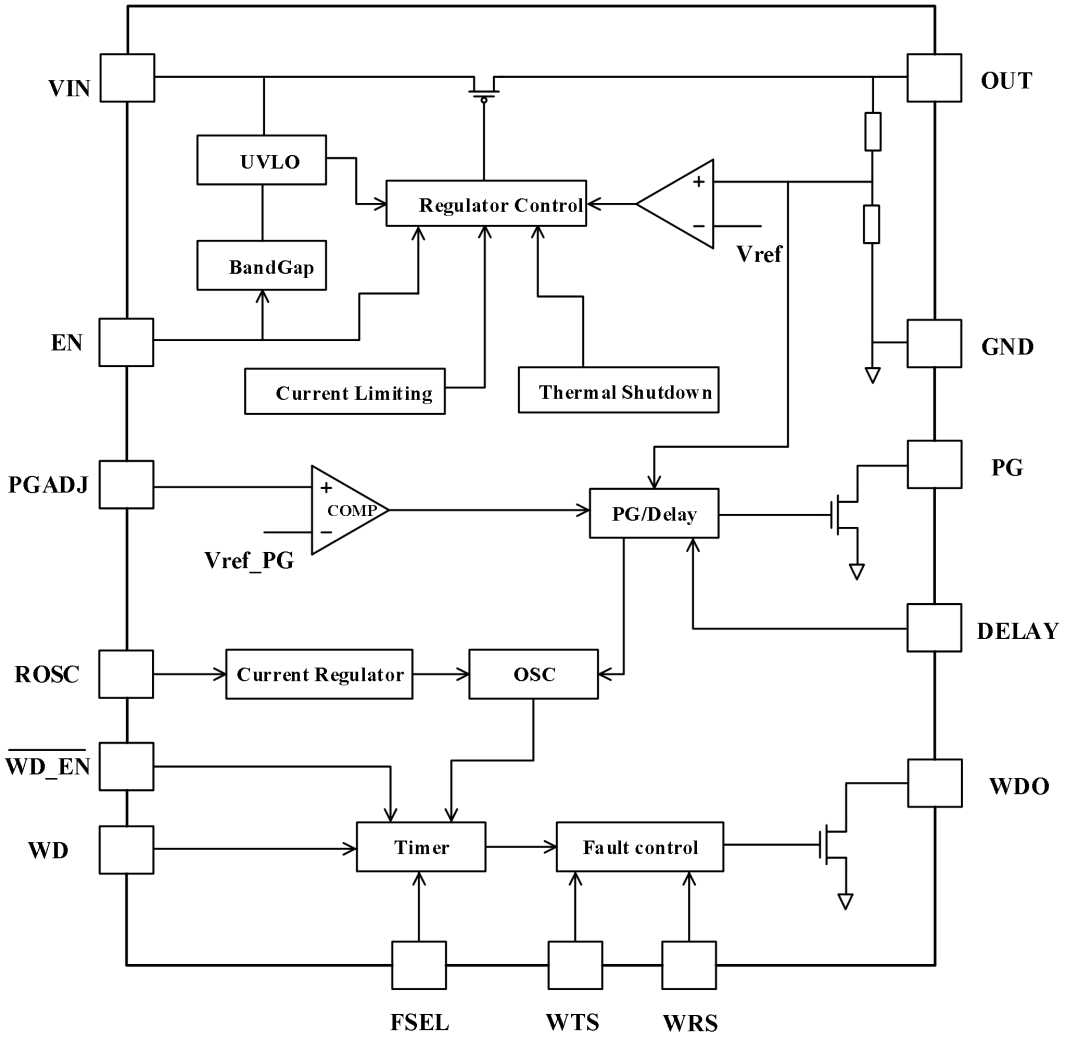


Figure 2 Internal block diagram of SIT24XX3Q series

FEATURE DESCRIPTION

Overview

The SIT24XX3Q series are ultra-low quiescent current, watchdog-timed low-dropout linear regulators (LDOs) that operate over a wide input voltage range of 4V to 40V. The series features exceptionally low quiescent currents: 1μA in shutdown, 12μA under no-load with the watchdog disabled, and 21μA under no-load with the watchdog enabled.

This product series provides fixed 3.3V or 5V outputs, capable of delivering up to 300mA of load current.

The SIT24XX3Q incorporates a configurable Power Good (PG) function that can directly drive a microprocessor (MCU) reset pin. The PG threshold is programmable via the PGADJ pin, which connects to an external resistor divider from OUT to GND. The divided voltage is compared internally with a 1.1V reference. By altering the divider ratio, users can set a custom PG threshold. If PGADJ is grounded, the device defaults to an internal fixed threshold.

The PG delay time is set using an external capacitor on the DELAY pin to ground. Once the output voltage reaches the PG rise threshold (V_PG_RISE), the DELAY pin begins sourcing a charge current. The PG output is allowed to assert high only after the voltage on the DELAY pin reaches its internal rise threshold (V_RISE). Users can select a capacitor value based on the MCU's timing requirements. If the DELAY pin is left floating, the device reverts to a fixed internal delay of 100μs.

The series offers a programmable watchdog function, selectable as either Window (WTS=0) or Standard (WTS=1) mode. $\overline{\text{WD\_EN}}$ is provided to control the watchdog enable/disable,and watchdog period is set with an external resistor (ROSC) to ground, with an accuracy better than 10%. The FSEL pin allows adjustment of the internal clock frequency to further modify the watchdog period. In Window mode, the open/close window ratio can be configured as 1:1 (WRS=0) or 8:1 (WRS=1).

During operation, the watchdog can be triggered to start its initialization count by a PG pull-up event, $\overline{\text{WD\_EN}}$ to zero, or a WDO fault recovery pull-up. The watchdog must be serviced by applying a high-level pulse (>100μs) to the WD input pin according to strict timing rules:

1.The first service pulse must occur within the initialization period.

2.In Window mode, subsequent pulses must occur only during the open window period.

3.Pulses are prohibited during the closed window period (Standard mode has no closed window).

If these timing rules are violated, the WDO pin will be pulled low and remain low for an fault period equal to 20% of the watchdog timeout time (t_WD). The ROSC pin must not be left floating or directly grounded, as this will cause the WDO pin to be held low continuously.

All watchdog timing parameters are specified in the table below:

	Window watchdog	Standard watchdog
FSEL HIGH	$t_{(WD)} = R_{ROSC} \times 0.5 \times 10^{-6}$	
FSEL LOW	$t_{(WD)} = R_{ROSC} \times 2.5 \times 10^{-6}$	
Watchdog initialization time	$t_{(WD\_INI)} = 8 \times t_{(WD)}$	
Open watchdog time $t_{(OW)}$ and Close watchdog time $t_{(CW)}$	$t_{(WD)} = t_{(OW)} + t_{(CW)}$	$t_{(WD)} = t_{(OW)}$
WRS HIGH	$t_{(OW)} = t_{(CW)} = 50\% \times t_{(WD)}$	-
WRS LOW	$t_{(OW)} = 8 \times t_{(CW)}) = (8 / 9) \times t_{(WD)}$	-
Fault Duration	$t_{(FLT)} = 20\% \times t_{(WD)}$	

The SIT24XX3Q series features integrated protection functions including current limit, over-temperature shutdown, and automatic restart.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Input voltage	VIN	-0.3	42	V
Enable voltage	EN	-0.3	VIN	V
Feedback voltage	FB	-0.3	5.5	V
Power Good	PG	-0.3	5.5	V
Output voltage	OUT	-0.3	5.5	V
Delay	DELAY	-0.3	5.5	V
Internal clock reference voltage	ROSC	-0.3	5.5	V
Watchdog status output	WDO	-0.3	5.5	V
Watchdog frequency selection	FSEL	-0.3	VIN	V
Watchdog type selection	WTS	-0.3	VIN	V
Watchdog enabled	$\overline{WD\_EN}$	-0.3	5.5	V
Watchdog signal input	WD	-0.3	5.5	V
Watchdog window ratio selection	WRS	-0.3	5.5	V
Ambient temperature	T_{amb}	-40	125	℃
Junction temperature	T_j	-40	150	℃
Storage temperature	T_{stg}	-55	150	℃

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to these conditions is not conducive to proper device operation, and continuous operation at or near these extremes may affect long-term reliability. Unless otherwise specified, all voltages are referenced to ground.

THERMAL INFORMATION

Symbol	Parameter	Package	Value	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	ETSSOP16	40	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	ETSSOP16	20.1	℃/W

DC CHARACTERISTICS

Unless otherwise specified, the following parameters' maximum and minimum values cover the recommended operating temperature range of -40℃≤T_{amb}≤125℃. Typical conditions: VIN = 14V, output capacitor = 10μF ceramic capacitor, T_{amb}=25℃.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage and current						
V_{IN}	Input voltage		4		40	V
$I_{(SD)}$	Shutdown supply current	EN=0, VIN=14V		1	4	μA
$I_{(Q)}$	Quiescent current	VIN=6~40V (SIT24503QT); VIN=4~40V (SIT24333QT); IOUT=1mA, EN=5V, Watchdog disabled; T_{amb}<80℃		12	29.6	μA
		VIN=6~40V (SIT24503QT); VIN=4~40V (SIT24333QT); IOUT=1mA, EN=5V, Watchdog enable		21	42	μA
		VIN=6~40V (SIT24503QT); VIN=4~40V (SIT24333QT); IOUT=100mA, EN=5V, Watchdog enable		72	105	μA
$V_{UVLO(RISING)}$	UVLO rising threshold voltage	V_{IN} rising	2.63	2.7	2.98	V
$V_{UVLO(HYST)}$	UVLO hysteresis			200		mV
Enable Input (EN), Watchdog Frequency Select Input (FSEL), Watchdog Mode Select Input (WTS)						
V_{IL}	Logic input low level				0.7	V
V_{IH}	Logic input high level		2			V
V_{hys}	Hysteresis			200		mV
Watchdog Enable Input（$\overline{WD\_EN}$）						
V_{IL}	$\overline{WD\_EN}$ pin low input threshold voltage	Watchdog enable			0.7	V
V_{IH}	$\overline{WD\_EN}$ pin high input threshold voltage	Watchdog disabled	2			V
I_{WD_EN}	$\overline{WD\_EN}$ pin low input threshold voltage	V_{WD_EN}=5V			3	μA
Watchdog（WD,WDO,WRS）						
V_{IL}	WD, WRS pin low-level input threshold voltage				30	% of V_{OUT}
V_{IH}	WD, WRS Pin high-level		70			% of

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	input threshold voltage					V_{OUT}
$V_{(HYST)}$	Hysteresis			10		% of V_{OUT}
I_{WD}	WD pin pull-down current	V_{WD}=5V		2	4	μA
$V_{(OL)}$	WDO Pin low-level output Voltage				0.4	V
I_{lkg}	WDO pin leakage current	WDO is pulled up to VOUT through a 10kΩ resistor			1	μA
ROSC Pin Current Reference Voltage						
V_{ROSC}	Reference voltage		0.95	1	1.05	V
Output						
V_{OUT}	Output voltage, stable output version	VIN = OUT + $V_{(Dropout)}$ to 40 V, I_{OUT} = 1mA to I_{MAX}	-2		2	%
$V_{(Line-Reg)}$	Line regulation	VIN = 6 V to 40 V, I_{OUT} = 10 mA			10	mV
$V_{(Load-Reg)}$	Load regulation	VIN = VOUT+1V, I_{OUT} = 1 mA to I_{MAX}			40	mV
Dropout Voltage						
$V_{(Dropout)100mA}$	Output differential voltage	OUT=5V, I_{OUT}=100mA		93	157	mV
$V_{(Dropout)300mA}$	Output differential voltage	OUT=5V, I_{OUT}=300mA		280	567	mV
Current limit						
$I_{(CL)-500mA}$	Output current limit		500	680		mA
PSRR						
PSRR	Power supply rejection ratio	I_{OUT} =100mA, frequency=100Hz, C_{OUT}=10 μF		60 (1)		dB
		I_{OUT} =100mA, frequency=100kHz, C_{OUT}=10μF		30 (1)		
Thermal shutdown						
$T_{(SD)}$	Over-temperature protection			175 (1)		℃
$T_{(HYST)}$	Over-temperature protection hysteresis window			20 (1)		℃
Power Good Signal						

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(PG-OL)}$	PG Low-Level Output Voltage				0.4	V
$V_{(PG-RISE)}$	PG rise threshold		87.5	92.5	97.5	%
$V_{(PG-FALL)}$	PG fall threshold		82.5	87.5	92.5	%
$V_{(PG-HYST)}$	PG hysteresis			5		%
$I_{(CHARGE)}$	Delay capacitor charging current	V_{DELAY}=1V		5		μA
$V_{(RISE)}$	Delay voltage rise threshold		0.95	1	1.05	V
$I_{DLY(DIS)}$	DELAY capacitor discharging current		0.5			mA
Adjustable Power Good Signal						
$V_{(PGADJ\_TH)falling}$	PGADJ Pin Switch Voltage		1.067	1.1	1.133	V
$V_{(PGADJ\_HYST)}$	PGADJ hysteresis			30		mV

Note (1): Guaranteed by design, not tested in production.

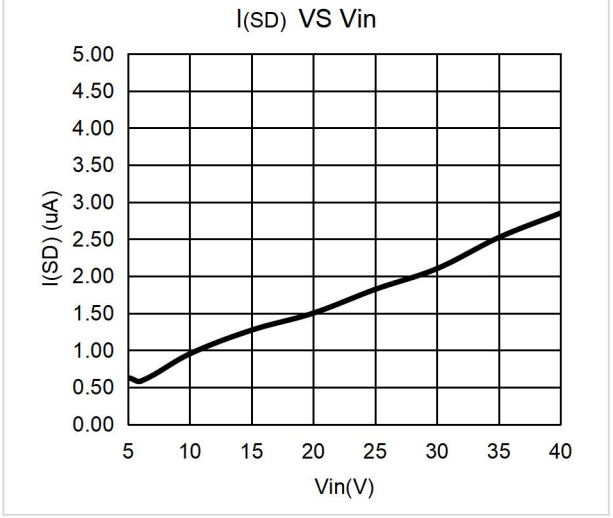
ESD RATINGS

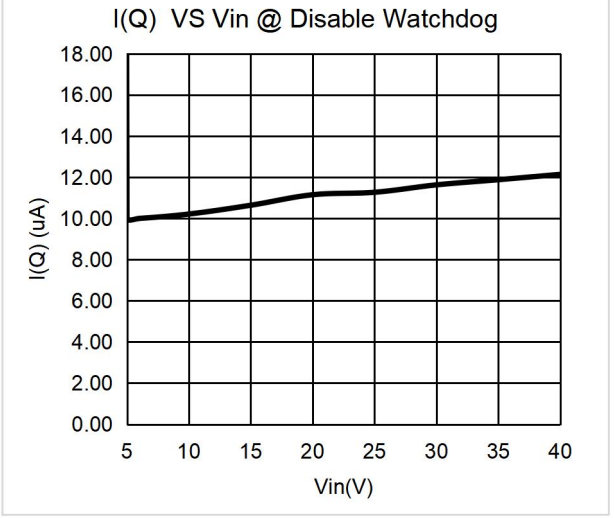
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ESD}	HBM				±3	kV
	CDM	All pins			±500	V
		Corner pins (1, 8, 9 and 16)			±750	V

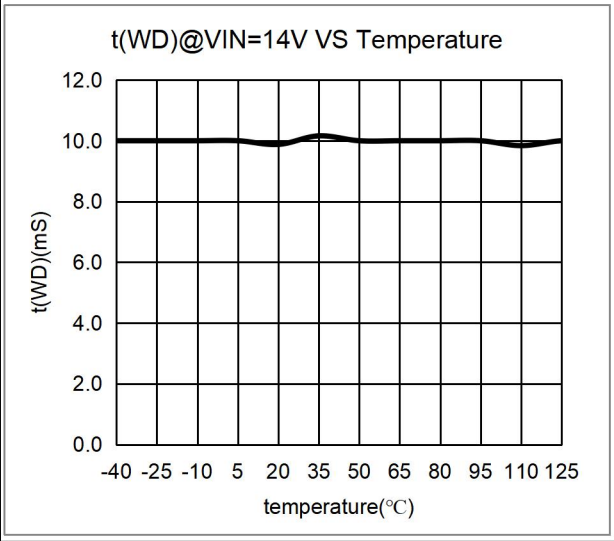
SWITCHING CHARACTERISTICS

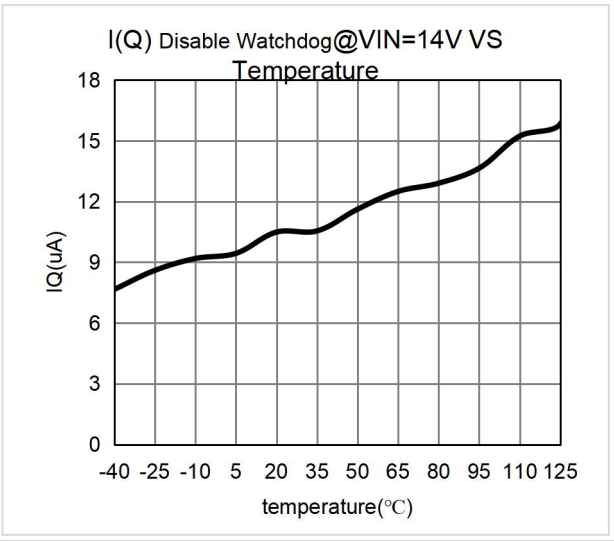
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Good Signal Delay Time						
$t_{(DLY\_FIX)}$	PG output delay	Pin DELAY floating		250		μs
$t_{(Deglitch)}$	PG de-bounce time	Pin DELAY floating		115		μs
$t_{(DLY)}$	PG output delay	C_{DELAY}=100 nF		20		ms
Watchdog						
$t_{(WD)}$	Watchdog window duration	$R_{(ROSC)}$=20kΩ±1%, FSEL=LOW	9	10	11	ms
		$R_{(ROSC)}$=20kΩ±1%, FSEL=HIGH	45	50	55	ms
$t_{(WD\_TOL)}$	Watchdog window duration tolerance range	$R_{(ROSC)}$=20kΩ±1% to 100kΩ±1%	-10%		10%	
$t_{p(WD)}$	Dog feeding time		100			μs
$t_{(WD\_HOLD)}$	Watchdog output reset time (as a percentage of watchdog window duration)			20		% of $t_{(WD)}$
$t_{(WD\_RESET)}$	Watchdog output reset time	$R_{(ROSC)}$=20kΩ±1%, FSEL=LOW	1.8	2	2.2	ms
		$R_{(ROSC)}$=20kΩ±1%, FSEL=HIGH	9	10	11	

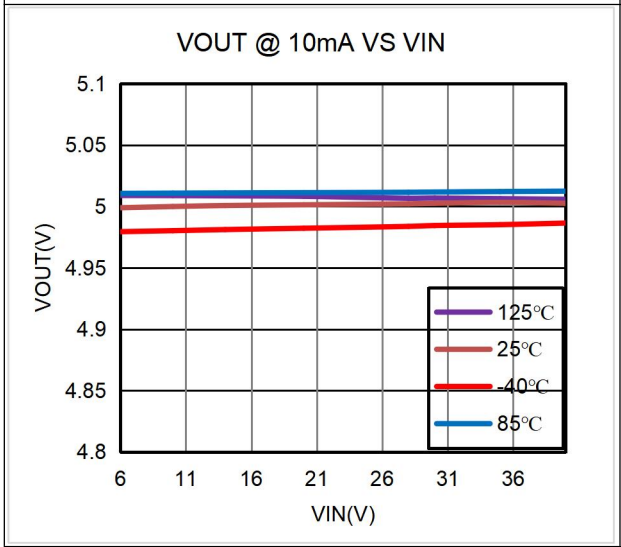
TYPICAL CHARACTERISTICS

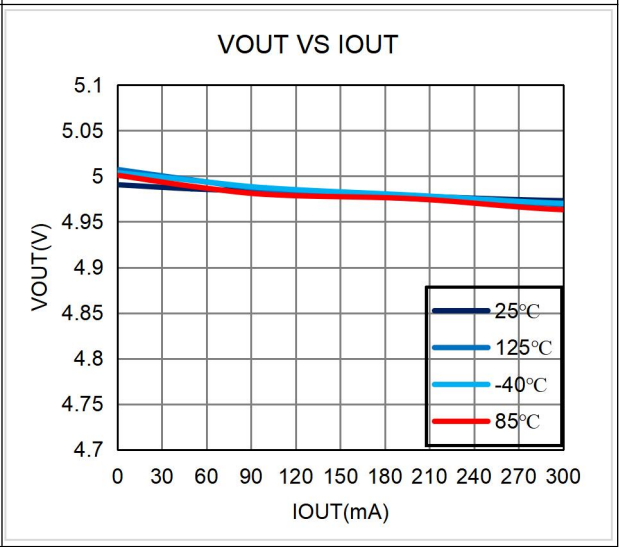


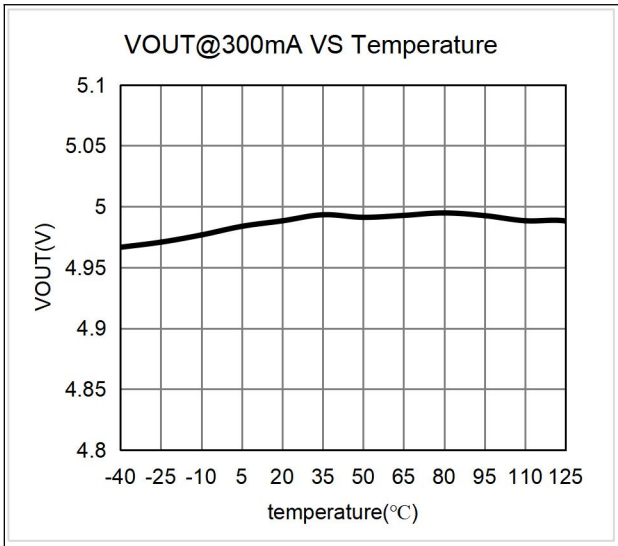


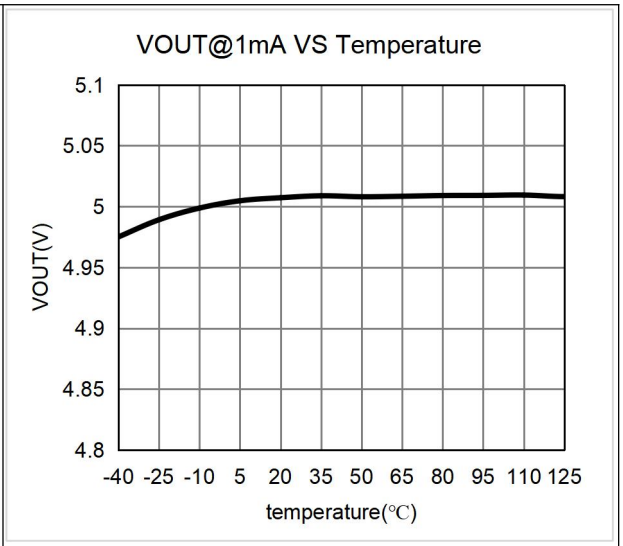


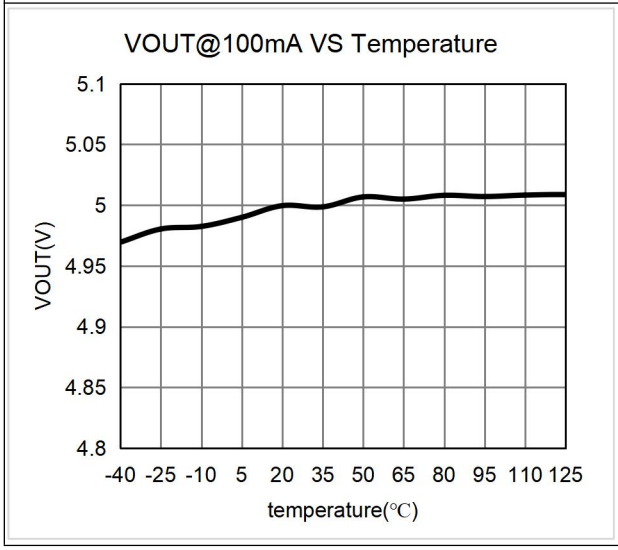


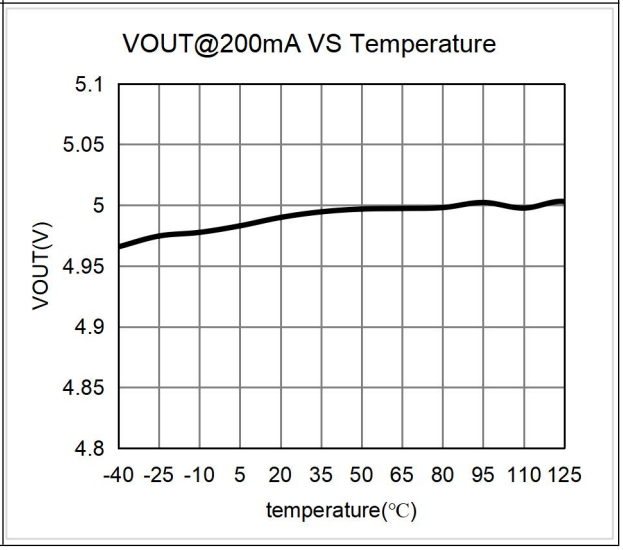





VOUT@300mA VS Temperature
VOUT(V)
5.1
5.05
5
4.95
4.9
4.85
4.8
-40 -25 -10 5 20 35 50 65 80 95 110 125
temperature(℃)

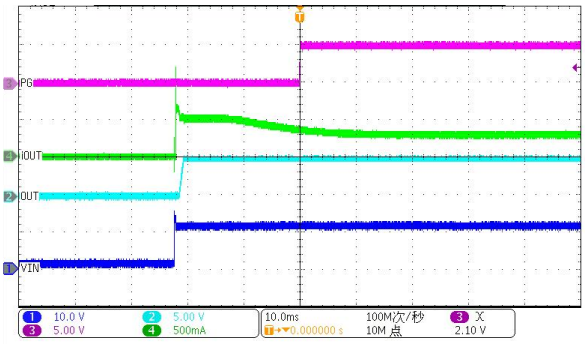

VOUT@1mA VS Temperature
VOUT(V)
5.1
5.05
5
4.95
4.9
4.85
4.8
-40 -25 -10 5 20 35 50 65 80 95 110 125
temperature(℃)


VOUT@100mA VS Temperature
VOUT(V)
5.1
5.05
5
4.95
4.9
4.85
4.8
-40 -25 -10 5 20 35 50 65 80 95 110 125
temperature(℃)

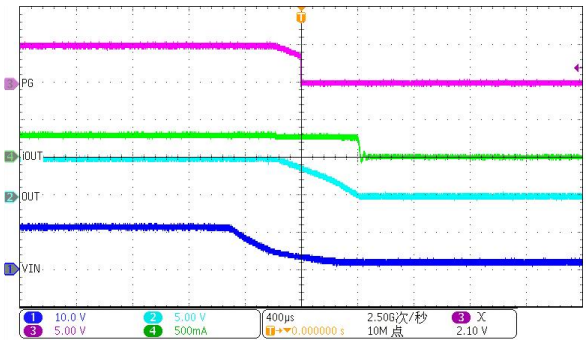

VOUT@200mA VS Temperature
VOUT(V)
5.1
5.05
5
4.95
4.9
4.85
4.8
-40 -25 -10 5 20 35 50 65 80 95 110 125
temperature(℃)

TYPICAL WAVEFORM

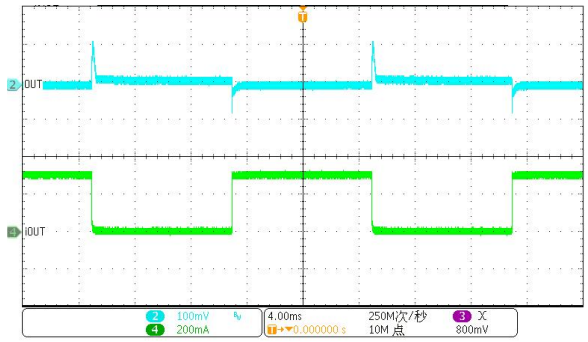
Unless otherwise specified, then VIN=12V, WRS= WTS= FSEL=WD_EN=GND, ROSC=20K.



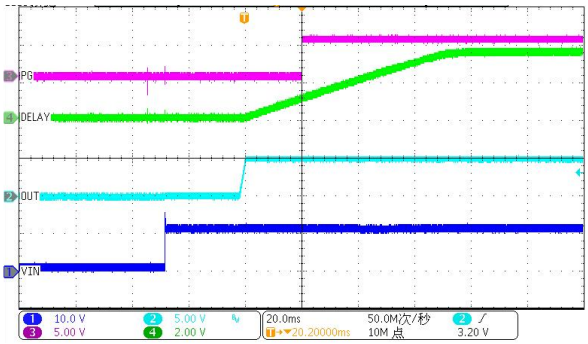
Power-Up @ Vin=VEN=12V, Vout=5V, IOUT=300mA



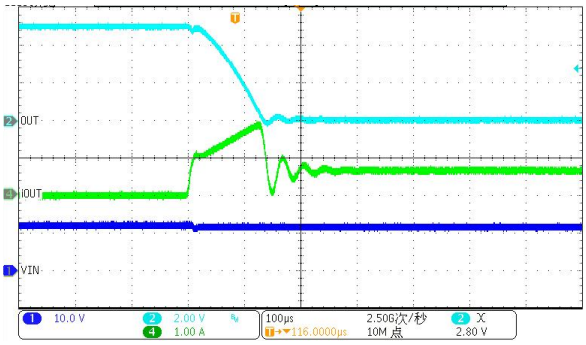
Power-Up @ Vin=VEN=12V, Vout=5V, IOUT=300mA



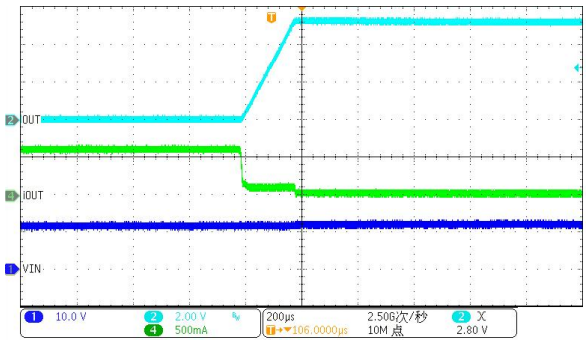
iOUT=1 <-> 300mA @ Vin=12V, Vout=5V



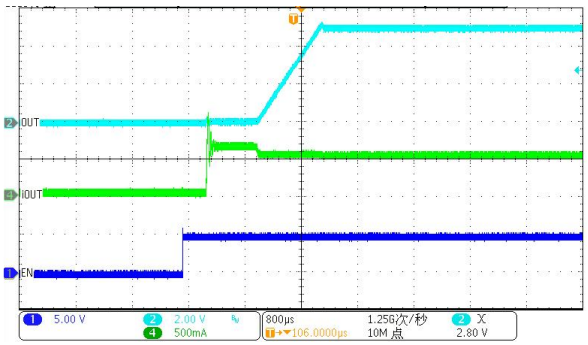
PG VS POWER UP@ Vin=12V, Vout=5V, IOUT=300mA，CDELAY=100 nF



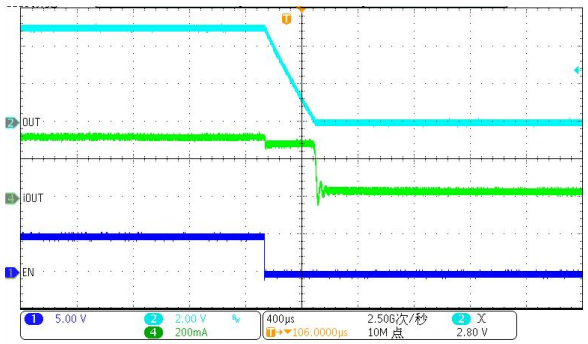
Short Circuit Entry @ no load



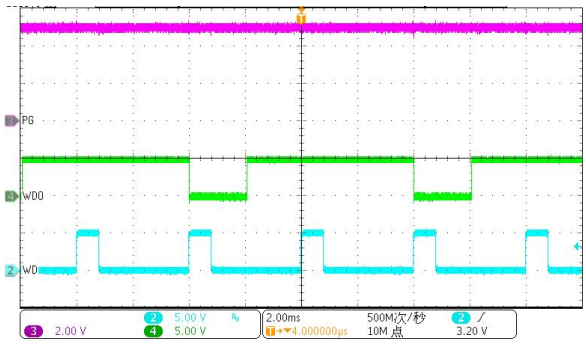
Short Circuit Recovery @ no load



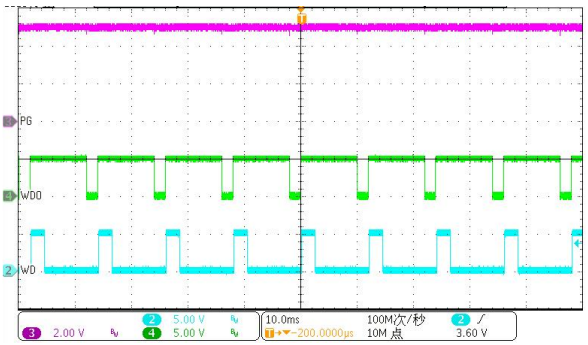
EN=L→H @ Vin=12V, Vout=5V, IOUT=300mA



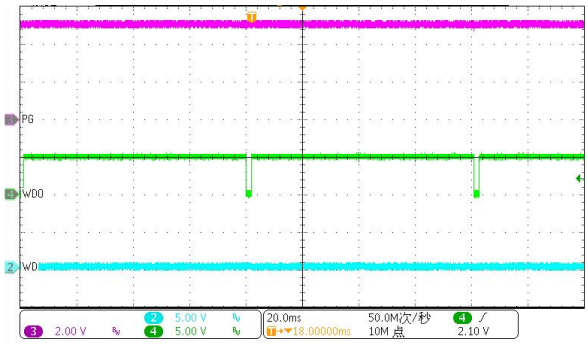
EN=H→L @ Vin=12V, Vout=5V, IOUT=300mA



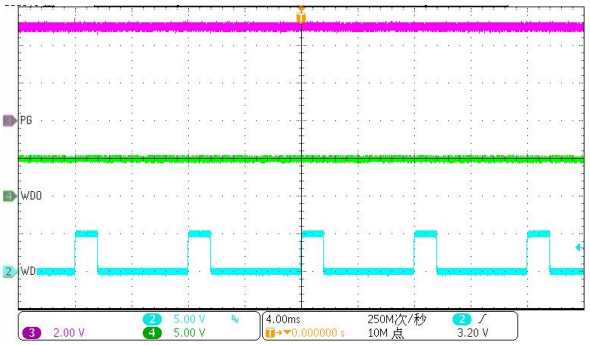
Fault (Receiving a WD rising edge during the closed window)



Fault (over maximum open-window duration t(WD) / 2)



Fault (no signal with WD)



Feed the watchdog normally

TYPICAL APPLICATION

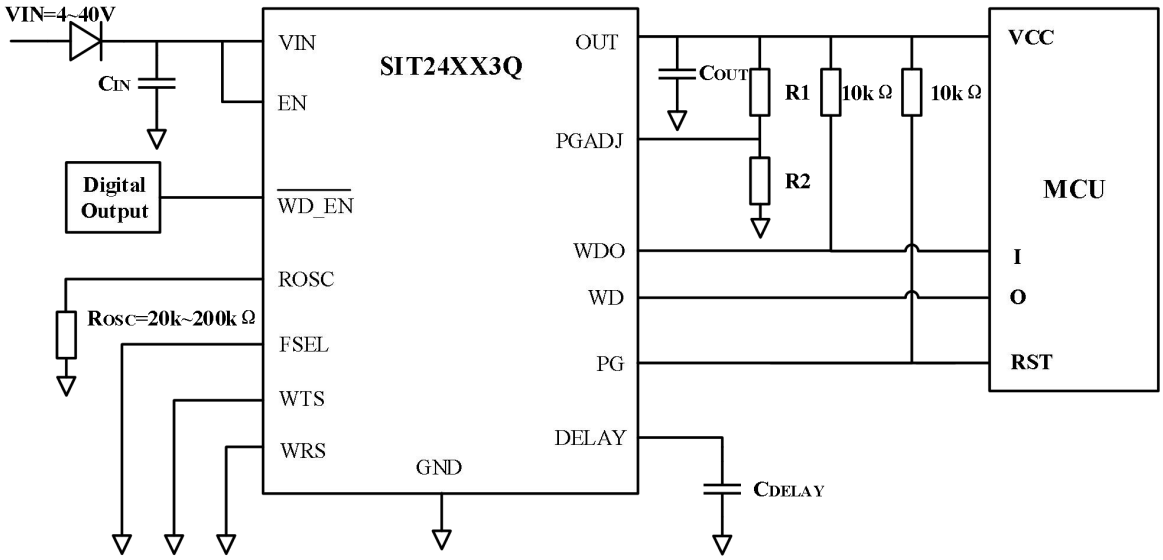


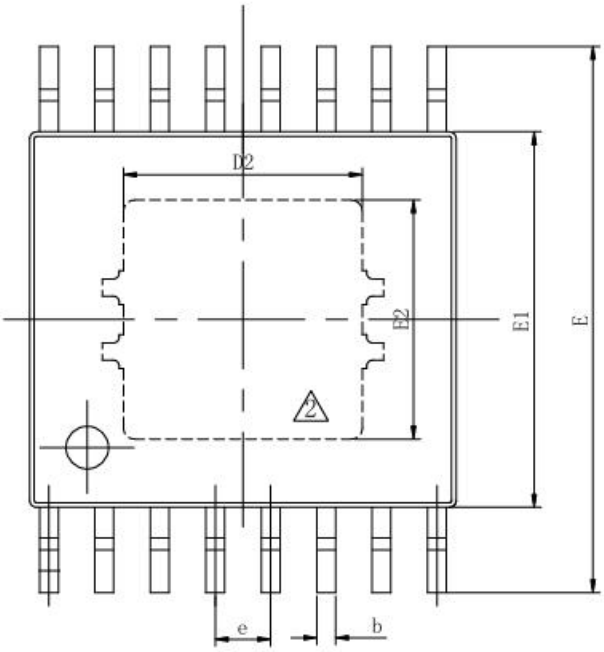
Figure 3 SIT24XX3Q series typical application diagram

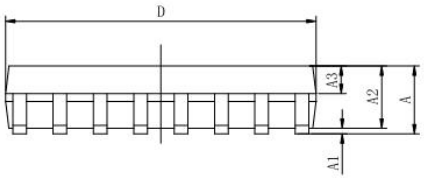
Note: Using an input rectifier diode is not recommended when the VIN voltage is low, as it will reduce the minimum operating voltage range of VIN.

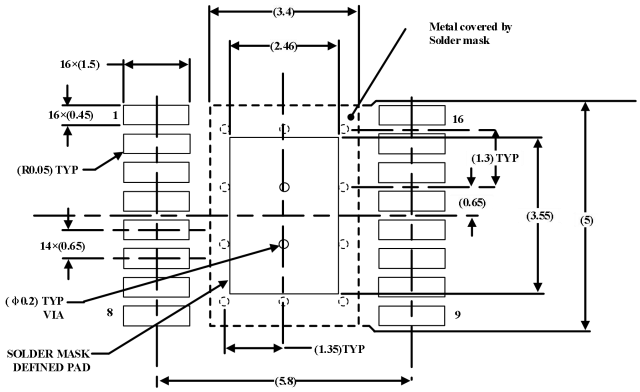
ETSSOP16 DIMENSIONS

PACKAGE SIZE

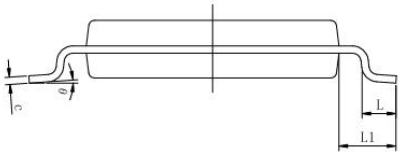
SYMBOL	MIN	NOM	MAX
A	-	-	1.20
A1	0.00	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
c	0.13	-	0.17
D	4.90	5.00	5.10
D2		2.80REF	
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2		2.10REF	
e		0.65BSC	
L	0.45	-	0.75
L1		1.00BSC	
θ	0°	-	8°







LAND PATTERN EXAMPLE（mm）

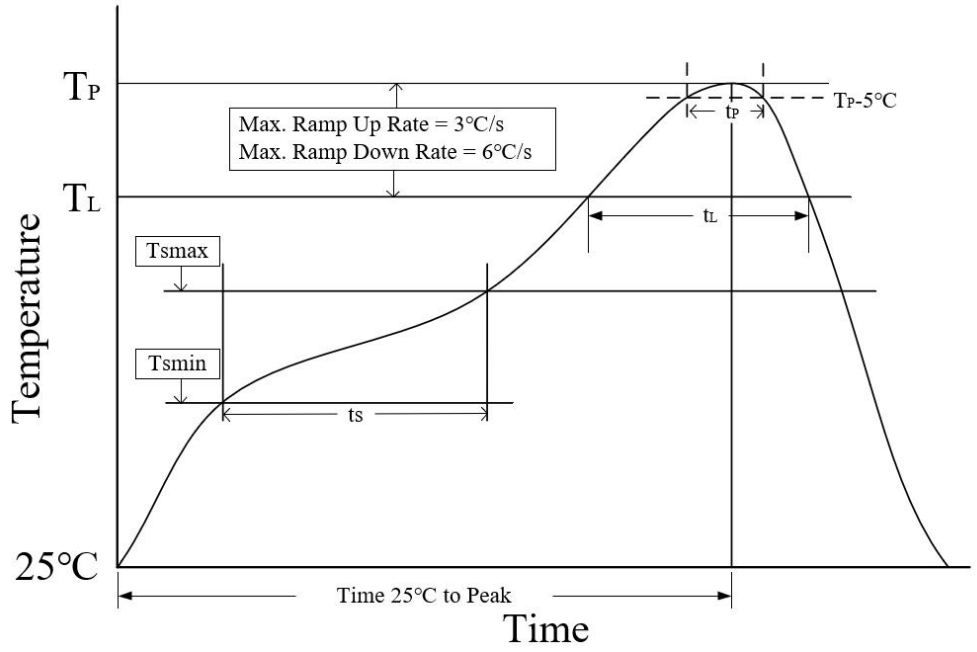


ORDERING INFORMATION

Type number	Output voltage	Output current	PG	Quiescent current (Disable WDG)	Package	MSL	Packing
SIT24503QT	5V	300mA	√	12μA	ETSSOP16	MSL 1	Tape and reel
SIT24333QT	3.3V	300mA	√	12μA	ETSSOP16	MSL 1	Tape and reel

2500 pieces/disc in taped packages.

REFLOW SOLDERING



Parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	3 °C/second max
Preheat time ts (T_{smin}=150 °C to T_{smax}=200 °C)	60-120 seconds
Melting time t_L (T_L=217 °C)	60-150 seconds
Peak temp T_P	260-265 °C
5 °C below peak temperature t_P	30 seconds
Ave cooling rate (T_P to T_L)	6 °C/second max
Normal temperature 25°Cto peak temperature T_P time	8 minutes max

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Datasheet status	Revision date
V1.0	Initial version.	June 2025
V1.1	Revised the D2, E2 packaging dimensions; Added the ordering information.	September 2025