

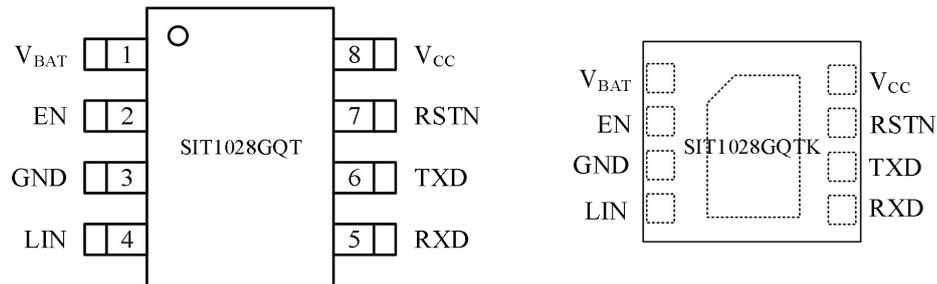
## FEATURES

- Compliant with LIN 2.x, ISO 17987-4:2016 (12V) and SAE J2602;
- AEC-Q100 qualified;
- With 5V/3.3V voltage regulator ;
- Integrated over-temperature protection function (thermal shutdown);
- Integrated dominant timeout function;
- Bus current limiting protection;
- Voltage regulator current limiting protection;
- Voltage regulator output undervoltage detection;
- Very low power consumption in sleep mode;
- Support LIN bus remote wake-up;
- LIN data transmission rate up to 20kbps;
- Available in SOP8 and DFN3\*3-8 packages; DFN3\*3-8 DFN3\*3-8 with improved Automated Optical Inspection (AOI) capability.

## DESCRIPTION

The SIT1028GQ is a Local Interconnect Network (LIN) physical layer transceiver with internal integrated high voltage input LDO. It can provide stable 5V/3.3V power supply for external ECU (Electronic Control Unit) microcontroller or related peripherals. The LIN transceiver is compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016(12V) and SAE J2602 standards. It is mainly suitable for in-vehicle networks with a transmission rate of 1kbps to 20kbps. The LIN bus output pin of the SIT1028GQ has an internal pull-up resistor with a bus output waveform shaping function to reduce electromagnetic radiation (EME). TXD pin is used as the input end to send the low-voltage signal of the microcontroller to LIN bus. Meanwhile, LIN pin receives the data stream on the bus, and the data is transmitted back to the microcontroller or to other microcontrollers by RXD output pin of the receiver.

The SIT1028GQ can operate in the range of 5.5V~28V and supports 12V application. The SIT1028GQ features extremely low current consumption in sleep mode, quickly minimizes power consumption in the event of failure, and can be remotely woken up via the LIN bus or placed in normal operating mode via a signal on the EN pin. SIT1028GQ provides a 5V/3.3V voltage regulator power on and power off detection output pin RSTN to facilitate the microcontroller to monitor the power supply of the regulator.

**PIN CONFIGURATION**

**Figure 1 SIT1028GQ pin configuration diagrams**
**PIN DESCRIPTION**
**Table 1 SIT1028GQ pin description**

Pin	Symbol	Description
1	V <sub>BAT</sub>	Battery supply voltage.
2	EN	Enable input.
3	GND	Ground.
4	LIN	LIN bus line input/output.
5	RXD	Receive data output; active LOW after a wake-up event.
6	TXD	Transmit data input.
7	RSTN	Voltage regulator reset signal output.
8	V <sub>CC</sub>	Voltage regulator output.

NOTE: In the DFN3\*3-8 package, the pad on the back is connected to the GND pin of the chip. In order to obtain better heat dissipation performance, the pad on the back can be connected to a suitable "ground" on the PCB board.

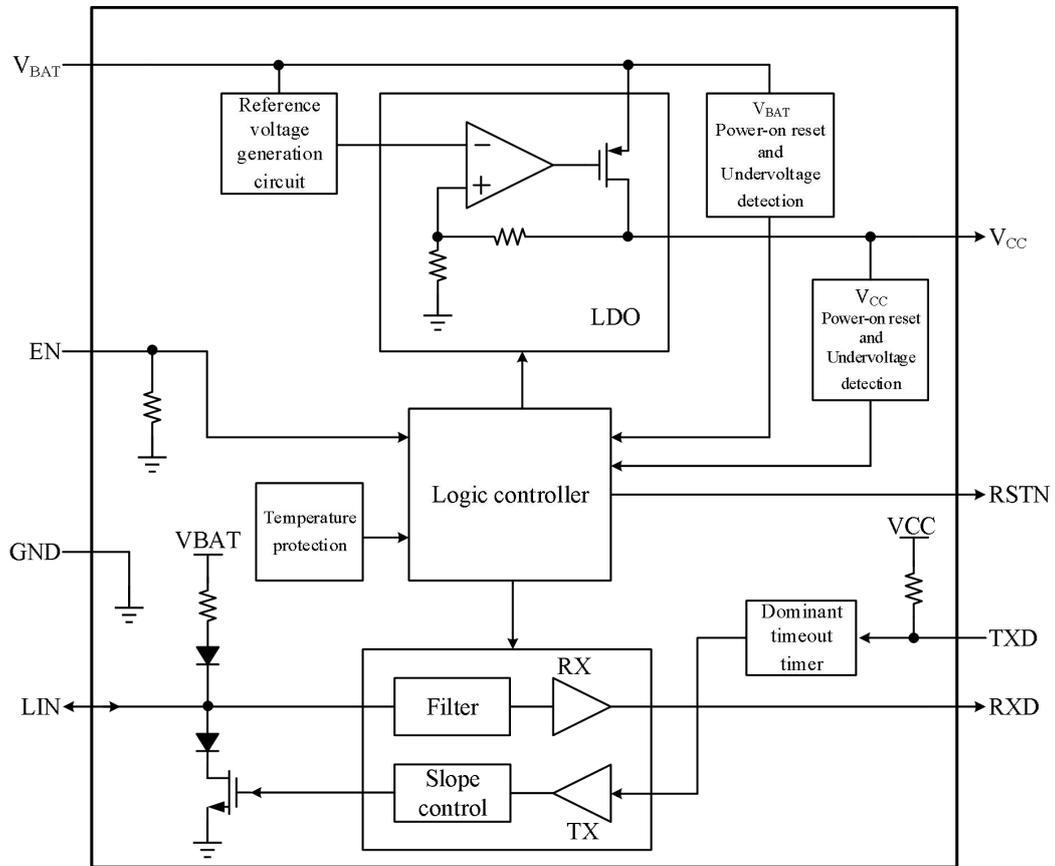
## LIMITING VALUES

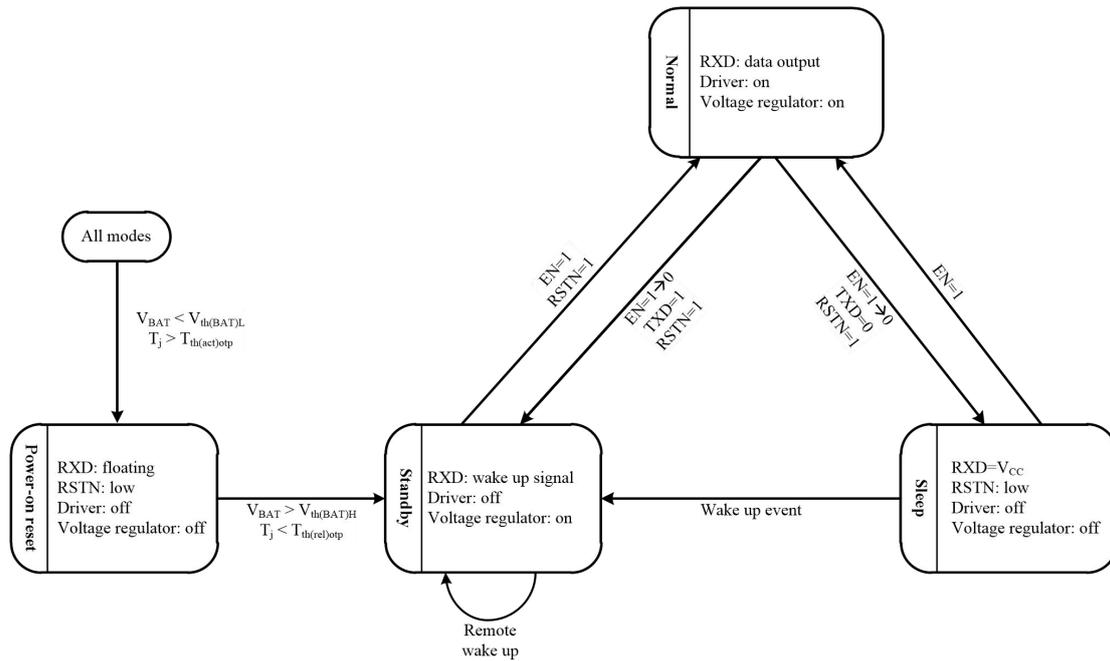
Parameter	Symbol	Conditions	Value	Unit
battery supply voltage	$V_{BAT}$	with respect to GND	-0.3 ~ +40	V
voltage on pins	$V_{CC}$	with respect to GND	-0.3 ~ +7	V
	$V_{RXD}$	with respect to GND	-0.3 ~ $V_{CC}+0.3$	V
	$V_{EN}$	with respect to GND	-0.3 ~ $V_{CC}+0.3$	V
	$V_{RSTN}$	with respect to GND	-0.3 ~ $V_{CC}+0.3$	V
	$V_{TXD}$	with respect to GND	-0.3 ~ $V_{CC}+0.3$	V
	$V_{LIN}$	with respect to GND and $V_{BAT}$	-40 ~ +40	V
	virtual junction temperature	$T_j$		-40 ~ 150
ambient temperature	$T_{amb}$		-40 ~ 125	°C
storage temperature	$T_{stg}$		-55 ~ 150	°C

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

## THERMAL INFORMATION

Symbol	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	SOP8	95	°C/W
		DFN3*3-8	65	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	SOP8	46	°C/W
		DFN3*3-8	35	°C/W

**BLOCK DIAGRAM**

**Figure 2 SIT1028GQ block diagram**

**FEATURE DESCRIPTION**

**Figure 3 State diagram**

## 1 Overview

The SIT1028GQ is an internally integrated high-voltage LDO chip that can be applied to the interface between the LIN protocol controller and the physical bus. It can be applied to the fields of in-vehicle and industrial control, and the transmission rate is up to 20kbps. The SIT1028GQ receives the transmit data stream from the protocol controller at the TXD terminal and converts it into the bus signal with the best voltage swing rate and waveform shaping; The input data on the LIN bus is output from the RXD port of the receiver to the external microcontroller. This device is compatible with the "LIN 2.x/ISO 17987-4:2016 (12V)/SAE J2602" standard.

## 2 Operating modes

As shown in **Figure 3**, the SIT1028GQ supports four operating modes for Power-on mode, Standby mode, Normal mode and Sleep mode.

### 2.1 Power-on mode

If the voltage on  $V_{BAT}$  is less than the power-down detection threshold  $V_{th(BAT)L}$  or an overtemperature event occurs, the SIT1028GQ will be in Power-on mode and both the voltage regulator and LIN transceiver will be off,  $RSTN = 0$ .

### 2.2 Standby mode

The SIT1028GQ can switch to Standby mode via other three operating modes and the voltage regulator

remains on. LIN transceiver is off and bus remote wake up function is enable (RXD = 0 as wake up flag).

When  $V_{BAT}$  voltage is greater than the power on detection threshold  $V_{th(BAT)H}$  and no over temperature event, SIT1028GQ will automatically switch from Power-on mode to Standby mode.

When SIT1028GQ is in normal mode, during the mode selection window, if  $EN = 0$ ,  $TXD = 1$  and  $RSTN = 1$ , SIT1028GQ will switch from Normal mode to Standby mode (as shown in **Figure 4**).

When SIT1028GQ is in sleep mode, it can switch to standby mode through the bus remote wake-up, the remote wake up behavior as shown in **Figure 5**.

### 2.3 Normal mode

After the SIT1028GQ is powered on and started normally, SIT1028GQ enters Standby mode firstly. When the EN is raised at  $RSTN = 1$ , SIT1028GQ switches from Standby mode to Normal mode. If SIT1028GQ is in Sleep mode, it can switch to Normal mode after raising the EN.

In normal mode, SIT1028GQ can normally send and receive data through LIN bus with the voltage regulator and LIN transceiver on. At this time, the microcontroller can send data to LIN bus through TXD input pins to convert low level logic level signals into high level  $V_{BAT}$  (battery) level signals (high level represents recessive, low level represents dominant), and perform bus waveform shaping to inhibit electromagnetic emission (EME). At the same time, the signal on the bus can be received by the pin LIN and output to the pin RXD via the SIT1028GQ receiver, which can be converted into low level logic level data for processing by the external microcontroller.

### 2.4 Sleep mode

It is the mode with the lowest power consumption of SIT1028GQ. In this case, both the voltage regulator and LIN transceiver are shut down, and  $RSTN$  is forced to pull down, which can be remotely awakened through LIN bus.

As shown in **Figure 3**, only Normal mode can switch to Sleep mode. During the mode selection window, if  $EN = 0$ ,  $TXD = 0$  and  $RSTN = 1$ , SIT1028GQ will switch from Normal mode to Sleep mode (as shown in **Figure 4**).

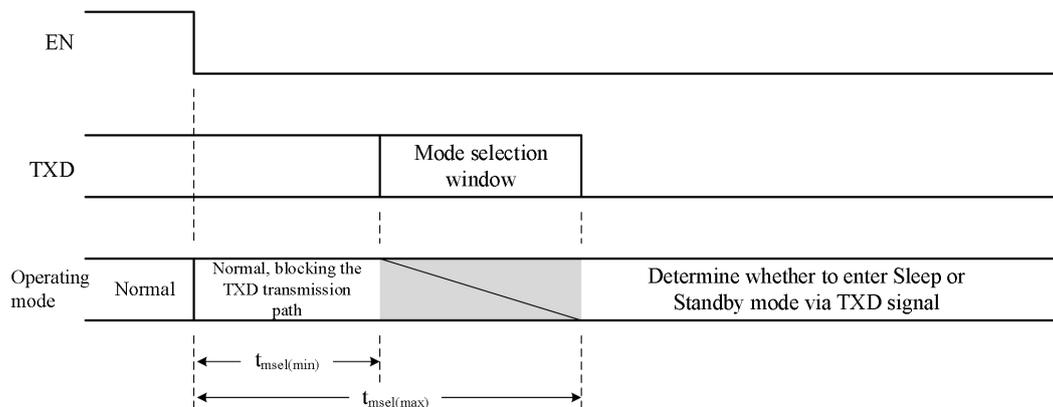
### 2.5 Switch from Normal to Sleep/Standby mode

As shown in **Figure 4**, SIT1028GQ first blocks the transmission path from TXD to LIN after EN is pulled down, and then enters the mode selection window after waiting for  $t_{msel(min)}$ . At this time, if  $TXD = 1$ , it enters the Standby mode, and if  $TXD = 0$ , it enters the Sleep mode. The total mode selection time after EN is pulled down is  $t_{msel(max)}$ .

## 3 Internal integrated voltage regulator $V_{CC}$

The SIT1028GQ is powered by a single power supply. With the pin  $V_{BAT}$  as the input, the internal integrated high voltage LDO (input voltage withstand 40V) provides stable 5V/3.3V to the external microcontroller and related peripherals through the pin  $V_{CC}$ , and the output current can reach 100mA. The undervoltage of  $V_{CC}$

can be reflected by the output signal of RSTN. When the  $V_{CC}$  is lower than the undervoltage detection threshold  $V_{UVD}$ , the RSTN output is low.



**Figure 4 Timing waveform of switching Normal to Standby/Sleep**

#### 4 Remote wake-up

Remote wake up on the LIN pin: When the LIN pin is pulled down to the low level through a falling edge, a rising edge appears at the next time, and the low-level maintenance time between the rising edge and the previous falling edge is greater than  $t_{wake(busdom)min}$ , then the process is regarded as an effective remote wake up (as shown in **Figure 5**). RXD is set to a low level to indicate the wake-up flag after a remote wake up occurs.

#### 5 Dominant time-out function

If the TXD pin due to hardware and/or software application failure is forced to permanent low level, the integrated TXD dominant timeout timer circuit can prevent the bus line are driven to permanent dominant status (blocking all network communication). The timer is triggered by the falling edge on the pin TXD. If the low level on the pin TXD maintain time longer than the internal timer ( $t_{to(dom)TXD}$ ), the transmitter will be disabled, to drive the bus into the recessive state. The timer is reset by the rising edge on the pin TXD.

#### 6 Overtemperature protection function

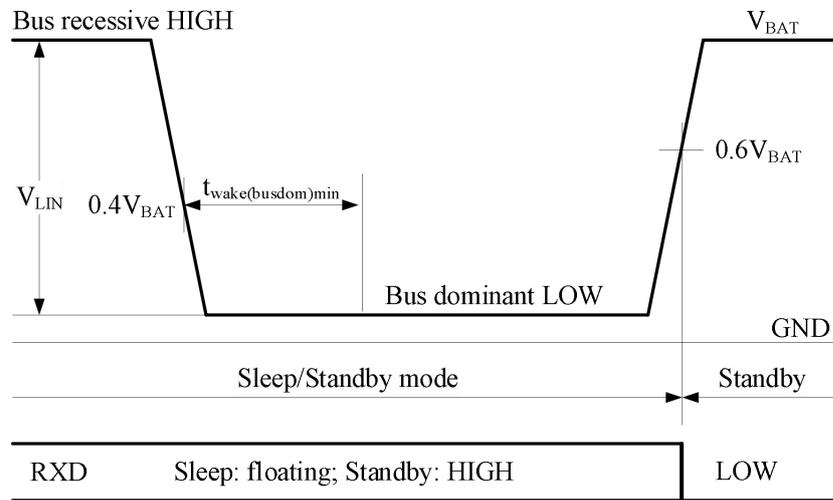
If an overtemperature event occurs when the SIT1028GQ is in normal or standby mode, it will be switched to Power-on mode, and the voltage regulator and LIN transceiver module will be shut down. When the temperature drops below the overtemperature protection recovery threshold, the SIT1028GQ switches from the Power-on mode to the standby mode.

#### 7 Fail-safe feature

- A pull-up to  $V_{CC}$  on pin TXD ensures that when the pin TXD is virtual welded or the microcontroller pin is floating, it remains bus recessive level.
- The current in the transmitter output stage is limited in order to protect the transmitter against burning

driver or affecting function when bus short circuits to pins  $V_{BAT}$ .

- A loss of power has no impact on the bus port and there is no reverse current on it.
- When EN or RSTN is low, the LIN driver will shut down automatically.
- After switching to normal mode, the LIN driver is enabled only if high level is detected in TXD.



**Figure 5 Remote wake-up behavior**

**STATIC CHARACTERISTICS**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Power consumption</b>						
Battery supply current	I <sub>BAT</sub>	Sleep mode (V <sub>LIN</sub> = V <sub>BAT</sub> )	2	10	40	μA
		Standby mode (V <sub>LIN</sub> = V <sub>BAT</sub> )	10	35	70	μA
		Normal mode (recessive) (V <sub>LIN</sub> = V <sub>BAT</sub> ; V <sub>TXD</sub> = V <sub>CC</sub> ; V <sub>RSTN</sub> = HIGH)	-	200	500	μA
		Normal mode (dominant) (V <sub>BAT</sub> = 12V; V <sub>TXD</sub> = 0V; V <sub>RSTN</sub> = HIGH)	-	1.6	3.5	mA
<b>Power-on reset</b>						
V <sub>BAT</sub> power-off detection threshold voltage	V <sub>th(BAT)L</sub>		3	3.8	4.2	V
V <sub>BAT</sub> power-on detection threshold voltage	V <sub>th(BAT)H</sub>		-	4.1	4.5	V
V <sub>BAT</sub> hysteresis voltage	V <sub>hys(BAT)</sub>		50	-	-	mV
<b>Pin V<sub>CC</sub></b>						
Voltage regulator output voltage	V <sub>CC</sub>	V <sub>CC(nom)</sub> = 5V; I <sub>CC</sub> = -100mA ~ 0	4.9	5	5.1	V
		V <sub>CC(nom)</sub> = 3.3V; I <sub>CC</sub> = -100mA ~ 0	3.234	3.3	3.366	V
Current limitation for voltage regulator	I <sub>Olim</sub>	V <sub>CC</sub> = 0 ~ 5.5V	-400	-	-100	mA
Undervoltage detection voltage	V <sub>UVd</sub>	V <sub>CC(nom)</sub> = 5V	4.2	-	4.75	V
		V <sub>CC(nom)</sub> = 3.3V	2.75	-	3.135	V
Undervoltage recover voltage	V <sub>UVR</sub>	V <sub>CC(nom)</sub> = 5V	4.35	-	4.9	V
		V <sub>CC(nom)</sub> = 3.3V	2.85	-	3.234	V
V <sub>BAT</sub> to V <sub>CC</sub> conduction resistance	R <sub>(VBAT-VCC)</sub> [1]	V <sub>CC(nom)</sub> = 5 V; V <sub>BAT</sub> = 4.5V ~ 5.5V; I <sub>V1</sub> = -100 mA ~ -5mA	-	-	9	Ω
Output capacitance	C <sub>O</sub> [1]	ESR < 5Ω	2.2	10	-	μF
<b>Pin TXD</b>						
Input threshold voltage	V <sub>th(SW)</sub>	V <sub>CC</sub> = 2.97 V ~ 5.5 V	0.3 V <sub>CC</sub>	-	0.7 V <sub>CC</sub>	V
Input hysteresis voltage	V <sub>hys(i)</sub>	V <sub>CC</sub> = 2.97 V ~ 5.5 V	200	-	-	mV
Pull-up resistance	R <sub>pu</sub>		5	12	25	kΩ
<b>Pin RXD</b>						

Parameter	Symbol	Condition	Min	Typ	Max	Unit
HIGH-level output current	$I_{OH}$	Normal mode; $V_{LIN} = V_{BAT}$ ; $V_{RXD} = V_{CC} - 0.4 V$	-	-	-0.4	mA
LOW-level output current	$I_{OL}$	Normal mode; $V_{LIN} = 0$ ; $V_{RXD} = 0.4 V$	0.4	-	-	mA
<b>Pin EN</b>						
Input threshold voltage	$V_{th(SW)}$		0.8	-	2	V
Pull-down resistance	$R_{pd}$		50	130	400	k $\Omega$
<b>Pin RSTN</b>						
Pull-up resistance	$R_{pu}$	$V_{RSTN} = V_{CC} - 0.4 V$ ; $V_{CC} = 2.97 V \sim 5.5 V$	3	-	12	k $\Omega$
LOW-level output current	$I_{OL}$	$V_{RSTN} = 0.4 V$ ; $V_{CC} = 2.97 V \sim 5.5 V$	3.2	-	40	mA
LOW-level output voltage	$V_{OL}$	$V_{CC} = 2.5 V \sim 5.5 V$	0	-	0.5	V
HIGH-level output voltage	$V_{OH}$		$0.8 V_{CC}$	-	$V_{CC} + 0.3$	V
<b>Pin LIN</b>						
Current limitation for driver dominant state	$I_{BUS\_LIM}$	$V_{TXD} = 0V$ ; $V_{LIN} = V_{BAT} = 18V$	40	-	100	mA
Receiver recessive input leakage current	$I_{BUS\_PAS\_rec}$	$V_{TXD} = V_{CC}$ ; $V_{LIN} = 18V$ ; $V_{BAT} = 5.5V$	-	-	15	$\mu A$
Receiver dominant input leakage current	$I_{BUS\_PAS\_dom}$	Normal mode $V_{TXD} = V_{CC}$ ; $V_{LIN} = 0V$ ; $V_{BAT} = 12V$	-1000	-	-	$\mu A$
Loss-of-ground bus leakage current	$I_{BUS\_NO\_GND}$	$V_{BAT} = 18V$ ; $V_{LIN} = 0V$	-1000	-	10	$\mu A$
Loss-of-power bus leakage current	$I_{BUS\_NO\_BAT}$	$V_{BAT} = 0V$ ; $V_{LIN} = 18V$	-	-	5	$\mu A$
Receiver dominant reverse threshold voltage	$V_{th(dom)RX}$	$V_{BAT} = 5.5 V \sim 18 V$	-	-	$0.4V_{BAT}$	V
Receiver recessive reverse threshold voltage	$V_{th(rec)RX}$	$V_{BAT} = 5.5 V \sim 18 V$	$0.6V_{BAT}$	-	-	V
Receiver center reverse threshold voltage	$V_{th(RX)entr}$	$V_{BAT} = 5.5 V \sim 18 V$ $V_{th(RX)entr} = (V_{th(rec)RX} + V_{th(dom)RX})/2$	$0.475V_{BAT}$	$0.5 V_{BAT}$	$0.525V_{BAT}$	V
Receiver hysteresis threshold voltage	$V_{th(hys)RX}$	$V_{BAT} = 5.5 V \sim 18 V$ $V_{th(hys)RX} = V_{th(rec)RX} - V_{th(dom)RX}$	-	-	$0.175V_{BAT}$	V
Slave resistance	$R_{slave}$	equivalent resistance between pins LIN and $V_{BAT}$ ; $V_{LIN} = 0V$ ; $V_{BAT} = 12V$	20	30	60	k $\Omega$
Capacitance on pin LIN	$C_{LIN}^{[1]}$		-	-	30	pF

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Dominant output voltage	$V_{o(dom)}$	Normal mode; $V_{TXD} = 0V$ ; $V_{BAT} = 7V$	-	-	1.4	V
		Normal mode; $V_{TXD} = 0V$ ; $V_{BAT} = 18V$	-	-	2.0	V
<b>Overtemperature protection</b>						
Overtemperature protection	$T_{th(act)otp}^{[1]}$		160	170	190	°C
Overtemperature recovery	$T_{th(rel)otp}^{[1]}$		125	140	155	°C

(Unless specified otherwise;  $5.5V \leq V_{BAT} \leq 28V$ ,  $-40^{\circ}C \leq T_j \leq 150^{\circ}C$ ; typical in  $V_{BAT}=13V$ ,  $T_{amb}=25^{\circ}C$ .)

[1] Not tested in production; guaranteed by design.

## DYNAMIC CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Duty cycles</b>						
duty cycle 1	$\delta 1^{[1][2]}$	$V_{th(rec)(max)}=0.744 \times V_{BAT}$ ; $V_{th(dom)(max)}=0.581 \times V_{BAT}$ ; $t_{bit}=50\mu s$ ; $V_{BAT}=7V \sim 18V$ <b>Figure 6 &amp; Figure 8</b>	0.396			
		$V_{th(rec)(max)}=0.76 \times V_{BAT}$ ; $V_{th(dom)(max)}=0.593 \times V_{BAT}$ ; $t_{bit}=50\mu s$ ; $V_{BAT}=5.5V \sim 7V$ <b>Figure 6 &amp; Figure 8</b>	0.396			
duty cycle 2	$\delta 2^{[2][3]}$	$V_{th(rec)(min)}=0.422 \times V_{BAT}$ ; $V_{th(dom)(min)}=0.284 \times V_{BAT}$ ; $t_{bit}=50\mu s$ ; $V_{BAT}=7.6V \sim 18V$ <b>Figure 6 &amp; Figure 8</b>			0.581	
duty cycle 2	$\delta 2^{[2][3]}$	$V_{th(rec)(min)}=0.41 \times V_{BAT}$ ; $V_{th(dom)(min)}=0.275 \times V_{BAT}$ ; $t_{bit}=50\mu s$ ; $V_{BAT}=6.1V \sim 7.6V$ <b>Figure 6 &amp; Figure 8</b>			0.581	
duty cycle 3	$\delta 3^{[1][2]}$	$V_{th(rec)(max)}=0.778 \times V_{BAT}$ ; $V_{th(dom)(max)}=0.616 \times V_{BAT}$ ; $t_{bit}=96\mu s$ ; $V_{BAT}=7V \sim 18V$ <b>Figure 6 &amp; Figure 8</b>	0.417			
		$V_{th(rec)(max)}=0.797 \times V_{BAT}$ ; $V_{th(dom)(max)}=0.630 \times V_{BAT}$ ; $t_{bit}=96\mu s$ ; $V_{BAT}=5.5V \sim 7V$ <b>Figure 6 &amp; Figure 8</b>	0.417			

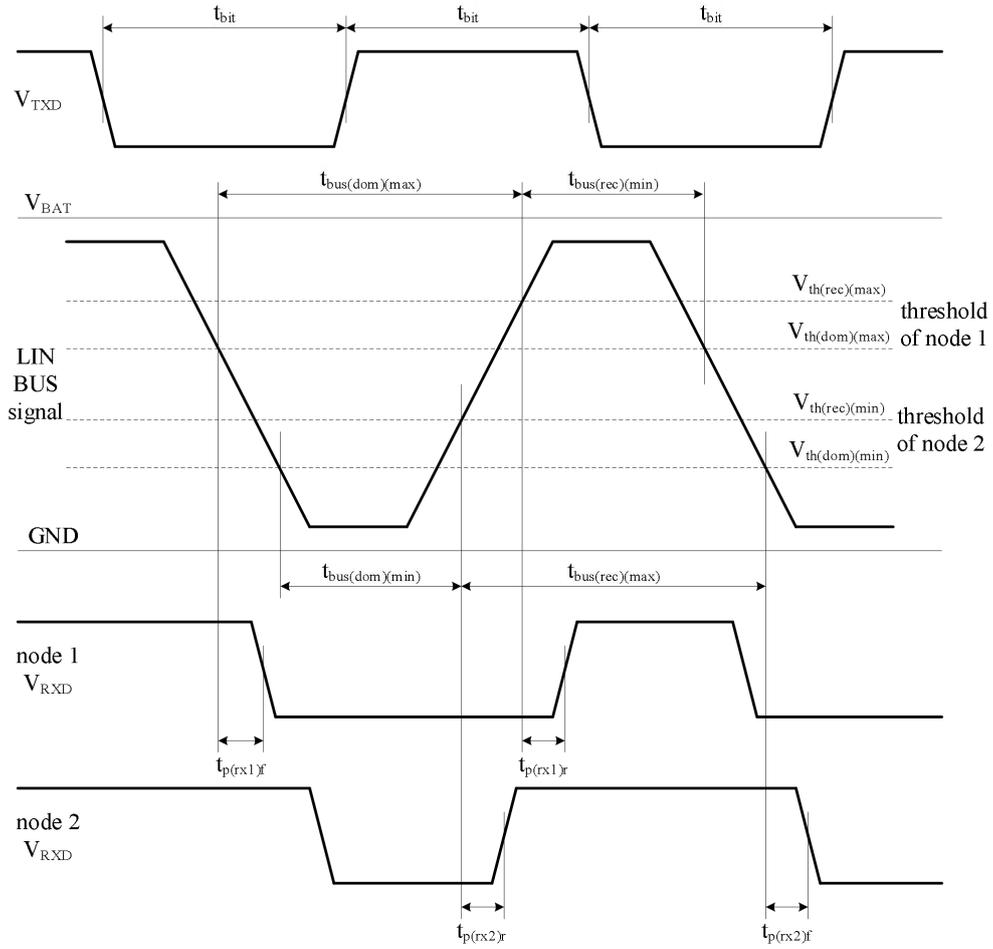
Parameter	Symbol	Condition	Min	Typ	Max	Unit
duty cycle 4	$\delta 4$ [2][3]	$V_{th(rec)(min)}=0.389 \times V_{BAT}$ ; $V_{th(dom)(min)}=0.251 \times V_{BAT}$ ; $t_{bit}=96\mu s$ ; $V_{BAT}=7.6V \sim 18V$ <b>Figure 6 &amp; Figure 8</b>			0.590	
		$V_{th(rec)(min)}=0.378 \times V_{BAT}$ ; $V_{th(dom)(min)}=0.242 \times V_{BAT}$ ; $t_{bit}=96\mu s$ ; $V_{BAT}=6.1V \sim 7.6V$ <b>Figure 6 &amp; Figure 8</b>			0.590	
<b>Timing characteristics</b>						
receiver propagation delay	$t_{PD(RX)}$	$C_{RXD} = 20 \text{ pF}$			6	$\mu s$
receiver propagation delay symmetry	$t_{PD(RX)sym}$	$C_{RXD} = 20 \text{ pF}$	-2		2	$\mu s$
Bus dominant wake-up time	$t_{wake(busdom)min}$	Sleep mode	30	80	150	$\mu s$
TXD dominant time-out time	$t_{to(dom)TXD}$	$V_{TXD}=0V$	6	-	20	ms
mode selection time	$t_{msel}$		5	-	35	$\mu s$
<b>Pin RSTN</b>						
reset time	$t_{rst}$		2	-	8	ms

(Unless specified otherwise;  $5.5V \leq V_{BAT} \leq 28V$ ,  $-40^\circ C \leq T_j \leq 150^\circ C$ ; typical in  $V_{BAT}=13V$ ,  $T_{amb}=25^\circ C$ .)

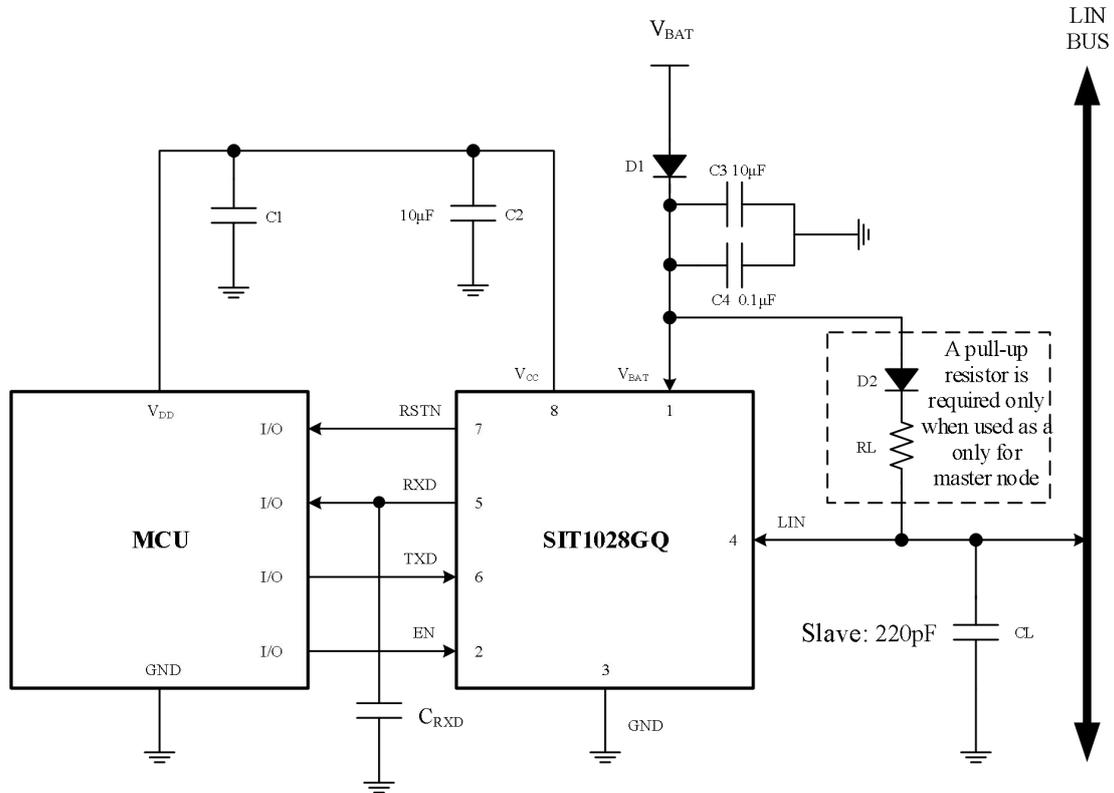
$$[1] \quad \delta 1, \delta 3 = \frac{t_{bus(rec)(min)}}{2 \times t_{bit}}$$

[2] Bus load conditions: (1)  $C_L=1nF$ ,  $R_L=1k\Omega$ ; (2)  $C_L=6.8nF$ ,  $R_L=660\Omega$ ; (3)  $C_L=10nF$ ,  $R_L=500\Omega$ .

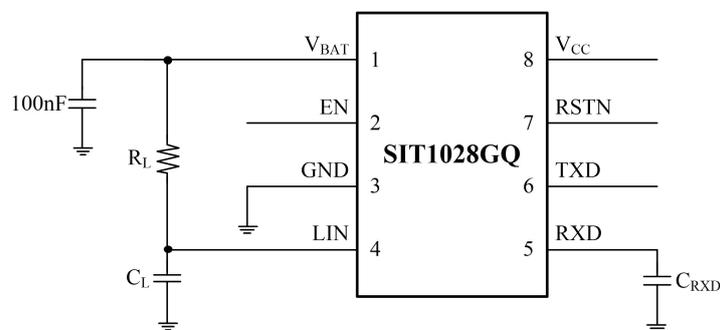
$$[3] \quad \delta 2, \delta 4 = \frac{t_{bus(rec)(max)}}{2 \times t_{bit}}$$



**Figure 6 Timing diagram of LIN transceiver duty cycle**

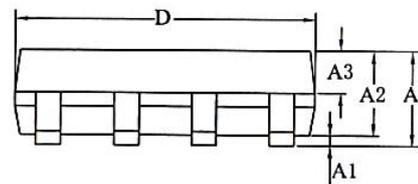
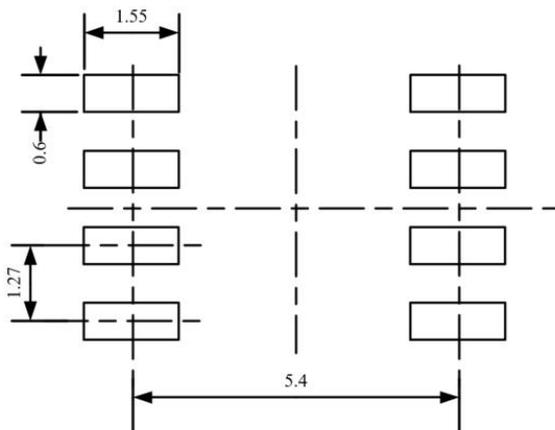
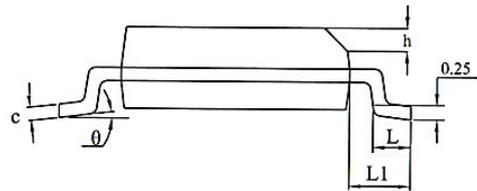
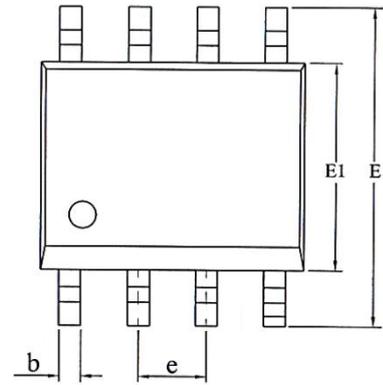
**TYPICAL APPLICATION**

**Figure 7 Typical application of the of SIT1028GQ**

Note:  $R_L/C_L$  combination of  $660\Omega/6.8nF$  is recommended when the master node is used to obtain a slower bus waveform slope.

**TEST MODEL**

**Figure 8 Switching characteristic test circuit**

**SOP8 DIMENSIONS**
**PACKAGE SIZE**

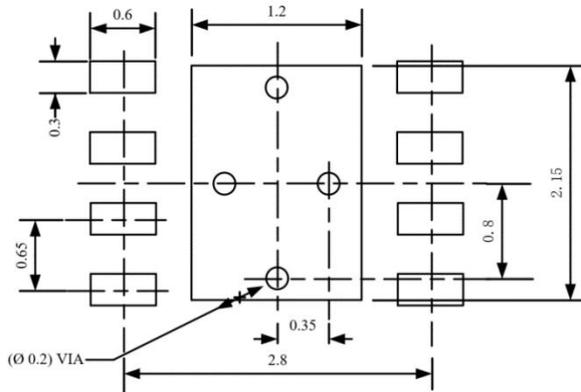
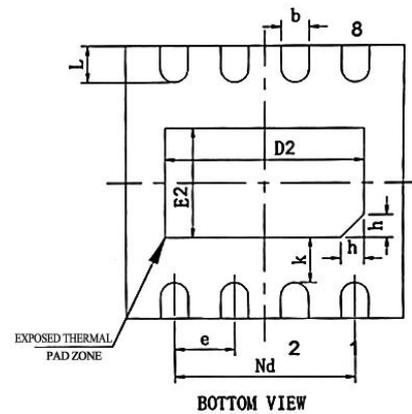
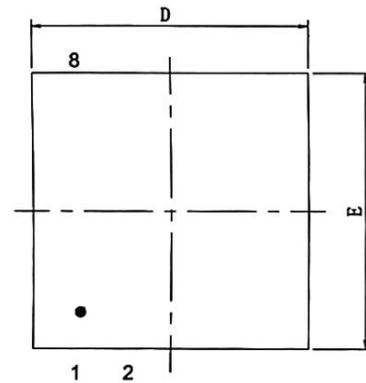
SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	1.40	-	1.80
A1	0.10	-	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.38	-	0.51
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.40	0.60	0.80
L1	1.05REF		
c	0.20	-	0.25
$\theta$	0°	-	8°



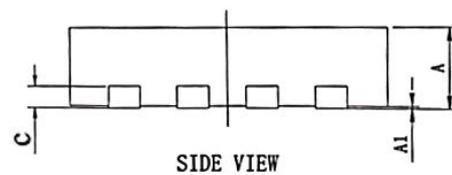
LAND PATTERN EXAMPLE (Unit: mm)

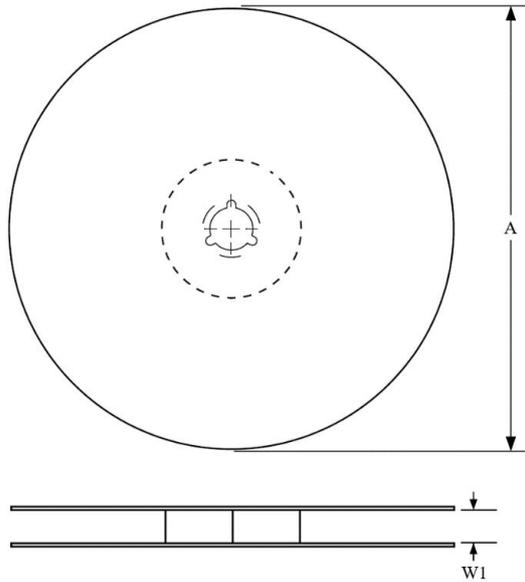
**DFN3\*3-8 DIMENSIONS**
**PACKAGE SIZE**

SYMBOL	MIN/mm	TYP /mm	MAX/mm
A	0.70	0.75	0.80
A1	0	0.02	0.05
c	0.203 REF		
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	2.05	2.15	2.25
Nd	1.95BSC		
E2	1.10	1.20	1.30
b	0.25	0.30	0.35
e	0.65 TYP		
k	0.50REF		
L	0.35	0.4	0.45
h	0.20	0.25	0.30

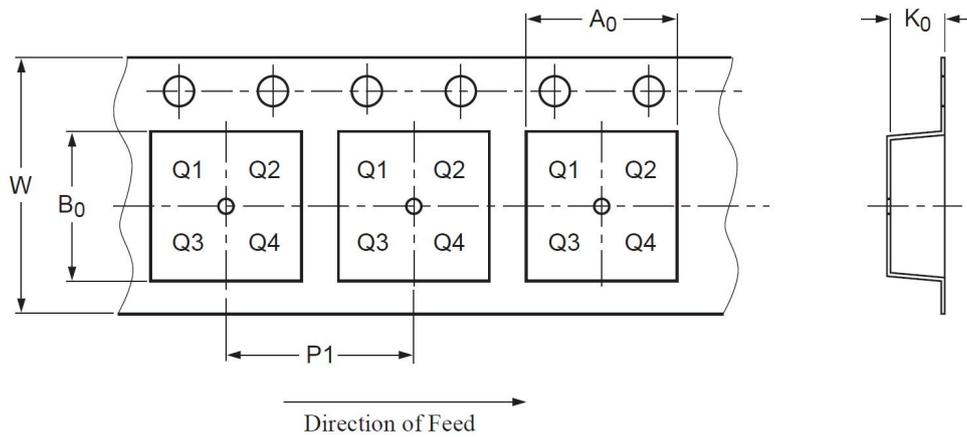


LAND PATTERN EXAMPLE (Unit: mm)



**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



PIN1 is in quadrant 1

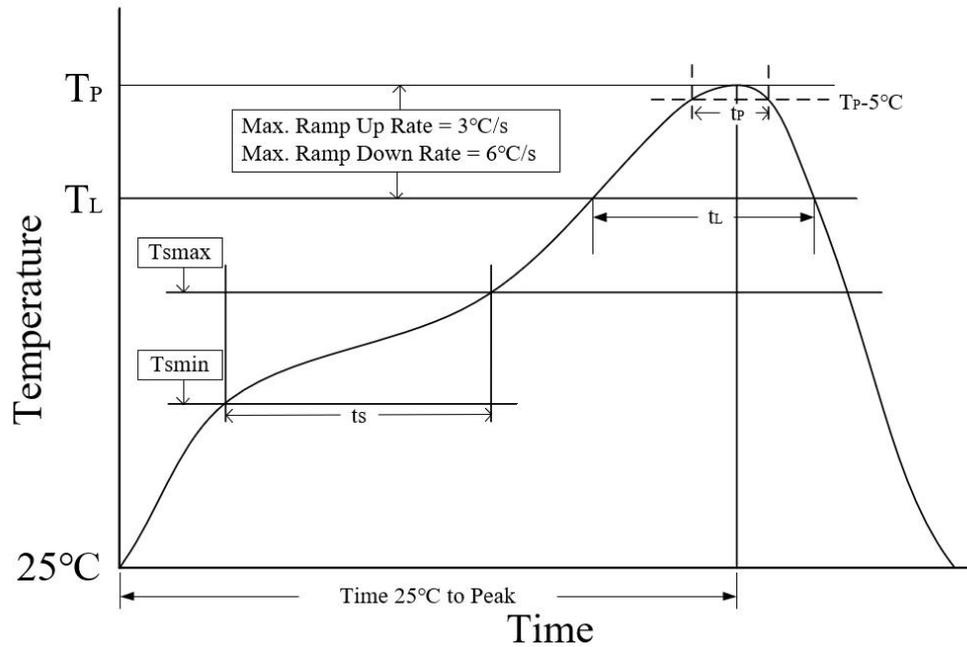
Package type	Reel diameter A (mm)	Tape width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
SOP8	330±1	12.4	6.60±0.1	5.30±0.10	1.90±0.1	8.00±0.1	12.00±0.1
DFN3*3-8	329±1	12.4	3.30±0.1	3.30±0.1	1.10±0.1	8.00±0.1	12.00±0.3

**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE	PACKING
SIT1028GQT/5V0	SOP8	Tape and reel
SIT1028GQT/3V3	SOP8	Tape and reel
SIT1028GQTK/5V0	DFN3*3-8, small outline, no leads	Tape and reel
SIT1028GQTK/3V3	DFN3*3-8, small outline, no leads	Tape and reel

SOP8 is packed with 2500 pieces/disc in braided packaging. Leadless DFN3\*3-8 is package with 6000 pieces/disc in braided packaging.

Note: SIT1028GQT/5V0 and SIT1028GQTK/5V0 are 5V voltage regulator versions;  
SIT1028GQT/3V3 and SIT1028GQTK/3V3 are 3.3V voltage regulator versions.

**REFLOW SOLDERING**


Parameter	Lead-free soldering conditions
Ave ramp up rate ( $T_L$ to $T_P$ )	3 °C/second max
Preheat time $t_s$ ( $T_{smin}=150$ °C to $T_{smax}=200$ °C)	60-120 seconds
Melting time $t_L$ ( $T_L=217$ °C)	60-150 seconds
Peak temp $T_P$	260-265 °C
5°C below peak temperature $t_P$	30 seconds
Ave cooling rate ( $T_P$ to $T_L$ )	6 °C/second max
Normal temperature 25°C to peak temperature $T_P$ time	8 minutes max

**Important statement**

SIT reserves the right to change the above-mentioned information without prior notice.

**REVISION HISTORY**

Version number	Data sheet status	Revision date
V1.0	Initial version.	January 2026