FEATURES

- Input voltage range: 3V to 40V
- AEC-Q100 Grade 1 qualified
- Ultra-low quiescent current: <6.5μA
- Low dropout voltage: 100mV @ 100mA
- Maximum output current: 300mA
- Ultra-low power sleep mode
- Shutdown current: 1μA
- Power Good (PG) indicator with adjustable delay time for MCU application
- High PSRR 70dB @ 100Hz
- Stable loop, requiring only a 4.7μF low-ESR output ceramic capacitor
- Enable (EN) pin with 40V withstand voltage
- Current limit, short-circuit protection
- Junction temperature: -40℃~ 150℃
- Thermal shutdown and automatic restart recovery
- Integrated soft start
- Available in ESOP8 package

DESCRIPTION

The SIT14503Q/P series is an ultra-low quiescent current, low dropout linear regulator (LDO) with a wide input voltage range from 3V to 40V. The series offers fixed output versions of 3.3V and 5V, as well as adjustable output versions with output voltages ranging from 3.0V to 18V, capable of delivering up to 300mA of load current. The quiescent current of the SIT14503Q/P series is less than 1μA in shutdown mode and less than 6.5μA under no-load conditions. The SIT14503Q/P series is suitable for power management applications in automotive electronics, industrial control systems, and wide-input-voltage battery-powered systems.

PIN CONFIGURATION

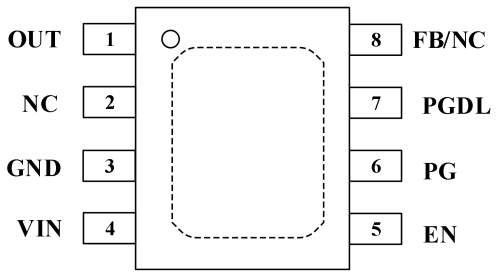


Figure 1 Pin configuration

PIN DESCRIPTION

Pin	Symbol	Pin description
1	OUT	Output pin. requiring only a low-value ceramic capacitor (≥4.7μF) between pins OUT and GND.
2	NC	No connection.
3	GND	Ground.
4	VIN	Input pin, only a low-value ceramic capacitor (≥1μF) between pins VIN and GND.
5	EN	Enable pin, connect to a logic control signal or to VIN directly.
6	PG	Power Good Pin. If not used, pin can be left floating.
7	PGDL	Programmable Power-Good Delay Time. If not used, pin can be left floating.
8	NC	No connection. (only SIT14503QT/P and SIT14333QT/P version)
8	FB	Feedback Input for Output Adjustable Version. FB is regulated to 0.65V nominally. This terminal is used to set output voltage.(only SIT14AJ3QT/P version)

Note: ESOP8 is recommended that the thermal pad is soldered to board ground.

FUNCTION BLOCK DIAGRAM

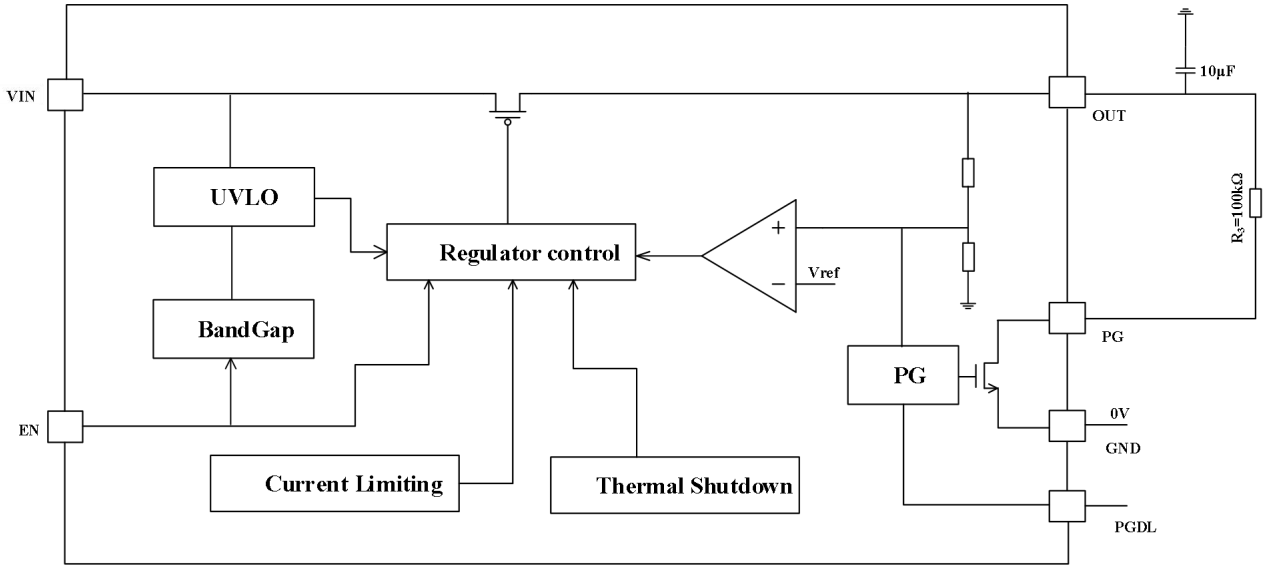


Figure 2 Internal Block Diagram of the SIT14503Q/P Fixed-Output Series

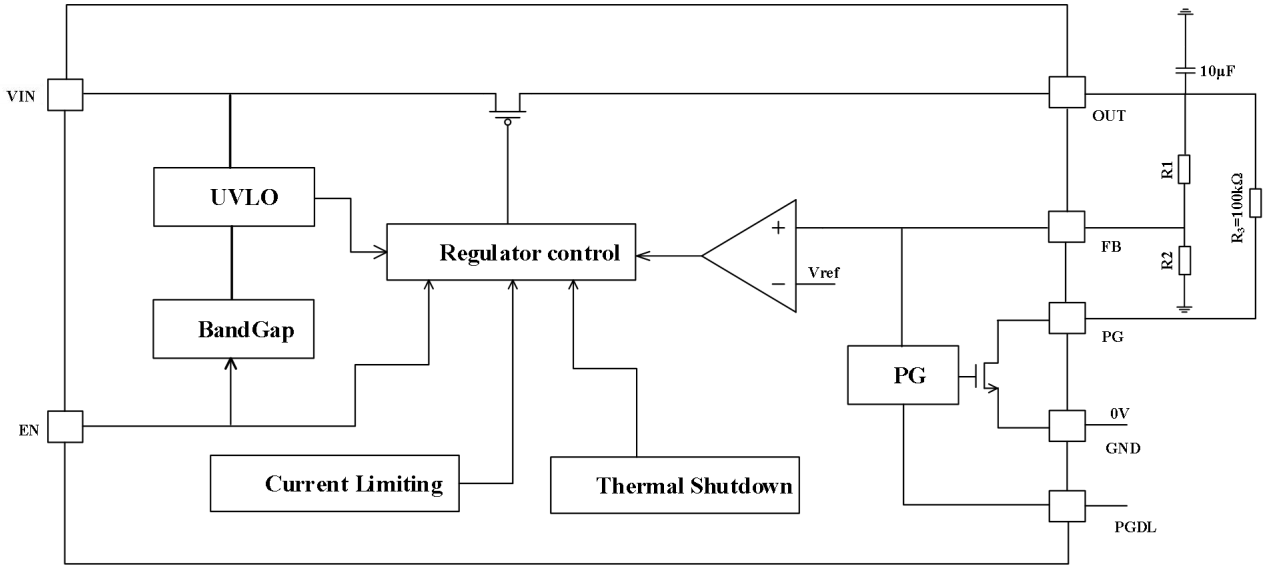


Figure 3 Internal Block Diagram of the SIT1AJ3Q/P Adjustable-Output Series

FEATURE DESCRIPTION

1 Overview

The SIT14503Q/P series is an ultra-low quiescent current, low dropout linear regulator (LDO) with a wide input voltage range from 3V to 40V. Its sleep mode current is less than 1μA, and the quiescent current under no-load conditions is less than 6.5μA. The series offers fixed output versions of 3.3V and 5V, as well as adjustable output versions with output voltages ranging from 3.0V to 18V. The adjustable output voltage versions use external resistor feedback, with a typical feedback (FB) pin voltage of 0.65V. The SIT14503Q/P series can deliver up to 300mA of load current. It features built-in protection functions including over-current protection, short-circuit protection, over-temperature shutdown, and automatic restart.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Input voltage	VIN	-0.3	42	V
Enable voltage	EN	-0.3	VIN	V
Feedback voltage	FB	-0.3	6	V
Output voltage	OUT	-0.3	20	V
Power Good	PG	-0.3	20	V
Delay	PGDL	-0.3	6	V
Output capacitor (Fixed version)	Cout	4.7	100	μF
Output capacitor (Adjustable version)	Cout	6.8	100	μF
Ambient temperature	T_{amb}	-40	125	℃
Junction temperature	T_j	-40	150	℃
Storage temperature	T_{stg}	-55	150	℃

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to these conditions is not conducive to proper device operation, and continuous operation at or near these extremes may affect long-term reliability. Unless otherwise specified, all voltages are referenced to ground.

THERMAL INFORMATION

Symbol	Parameter	Package	Value	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	ESOP8	42	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	ESOP8	8	℃/W

Note: According to JEDEC JESD51-2, JESD51-5, and JESD51-7, under natural convection conditions, using a 2s2p PCB (two signal layers and two power layers).

DC CHARACTERISTICS

Unless otherwise specified, the maximum and minimum values of the following parameters are specified over the recommended operating temperature range of -40℃≤T_{amb}≤125℃. Typical conditions: VIN = 14V, output capacitor = 10μF ceramic capacitor, T_{amb}=25℃

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage and current						
V_{IN}	Input voltage		3		40	V
$I_{(SD)}$	Shutdown supply current	EN=0, VIN=14V		0.7	3	μA
$I_{(Q)}$	Quiescent current	EN=5, VIN=14V I_{OUT}=0A		6.5	12	μA
Enable Input (EN)						
V_{IL}	Logic input low level				0.7	V
V_{IH}	Logic input high level		2			V
I_{EN}	EN input current	EN=5V		0.11	0.5	μA
Adjustable output						
V_{OUT}	Output voltage, stable output version	VIN = OUT + $V_{(Dropout)}$ to 40 V, I_{OUT} = 1mA to I_{MAX}	-2		2	%
$V_{(Line-Reg)}$	Line regulation	VIN = 6 V to 40 V, I_{OUT} = 10 mA			20	mV
$V_{(Load-Reg)}$	Load regulation	VIN = 14 V, I_{OUT} = 1 mA to I_{MAX}			50	mV
Dropout Voltage						
$V_{(Dropout)100mA}$	Output differential voltage	OUT=5V, I_{OUT}=100mA		100	180	mV
		OUT=3.3V, I_{OUT}=100mA		180	480	mV
$V_{(Dropout)300mA}$	Output differential voltage	OUT=5V, I_{OUT}=300mA		300	510	mV
		OUT=3.3V, I_{OUT}=300mA		500	960	mV
Feedback Voltage						
V_{FB}	Feedback voltage		0.63	0.65	0.663	V
I_{FB}	Feedback voltage leakage current	V_{FB}=0.65V	-0.1	0	0.1	μA
Current limit						
$I_{(CL)-300mA}$	Output current limit			400		mA
PSRR						
PSRR	Power supply rejection ratio	I_{OUT} =50mA, f=100Hz, C_{OUT}=10 μF		70 (1)		dB

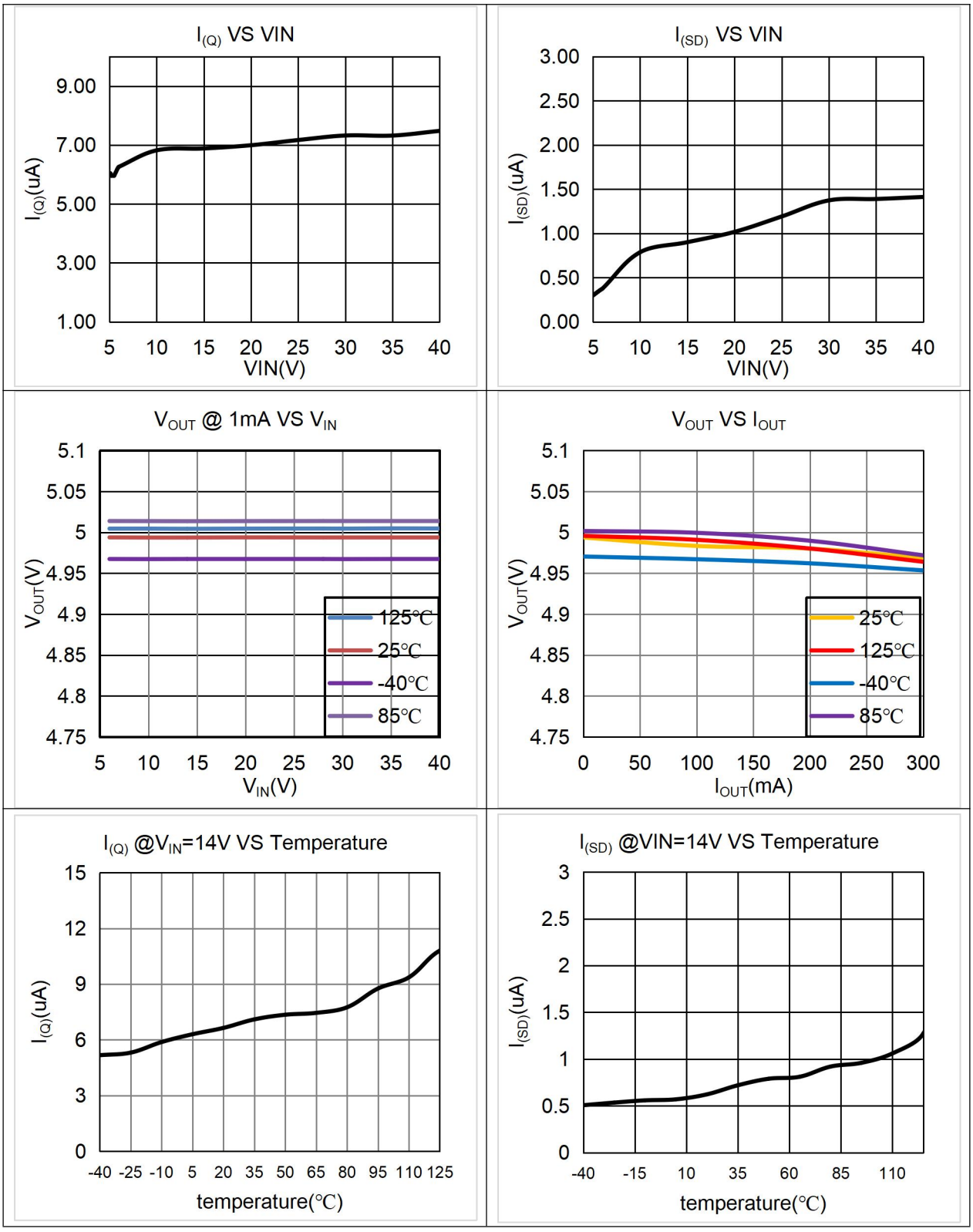
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Thermal shutdown						
$T_{(SD)}$	Over-temperature protection			160 (1)		℃
$T_{(REL)}$	Thermal Shutdown Recovery			140 (1)		℃
Power Good Signal						
$V_{(PG-OL)}$	PG Low-Level Output Voltage				0.4	V
$V_{(PG-RISE)}$	PG rise threshold		90		96	%
$V_{(PG-FALL)}$	PG fall threshold		84		90	%
$I_{(CHARGE)}$	Delay capacitor charging current			1.45		μA
$V_{(RISE)}$	PGDL voltage rise threshold		1.20	1.23	1.26	V
$t_{(DLY\_FIX)}$	PG output delay	PGDL pin left floating		104		μs
$t_{(Deglitch)}$	PG debounce Time	PGDL pin left floating		210		μs
$t_{(DLY)}$	PG output delay	C_{PGDL}=100 nF		84		ms

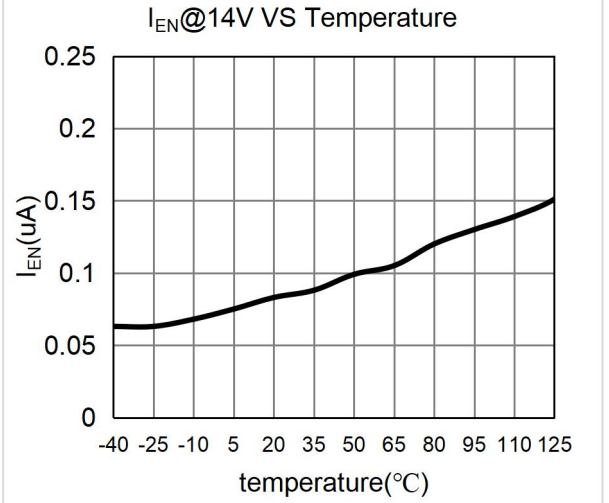
Note (1): Guaranteed by design, not tested in production.

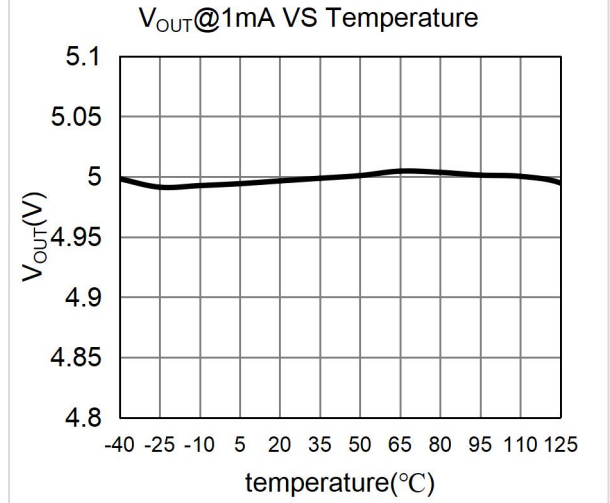
ESD RATINGS

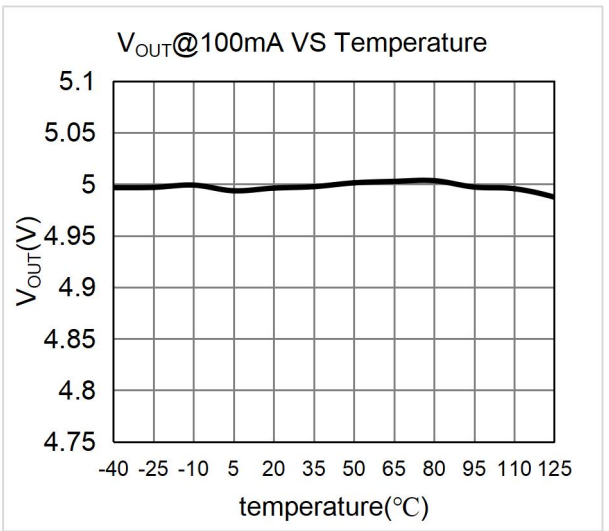
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ESD}	HBM				±4000	V
	CDM				±1500	V

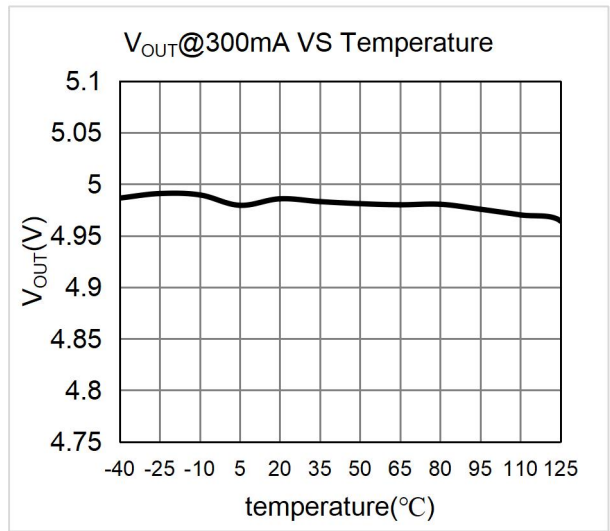
TYPICAL CHARACTERISTICS

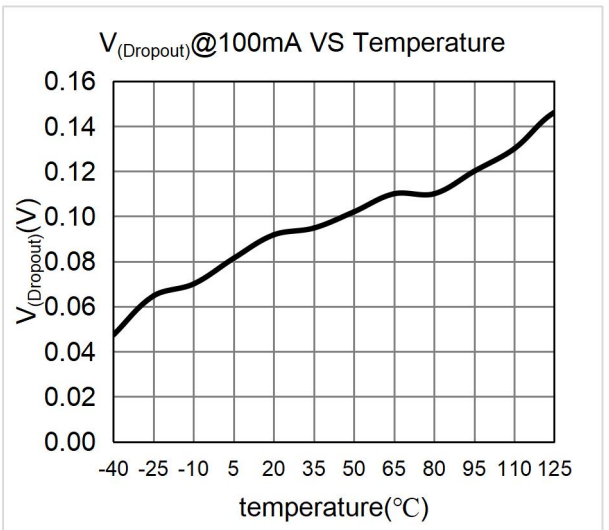


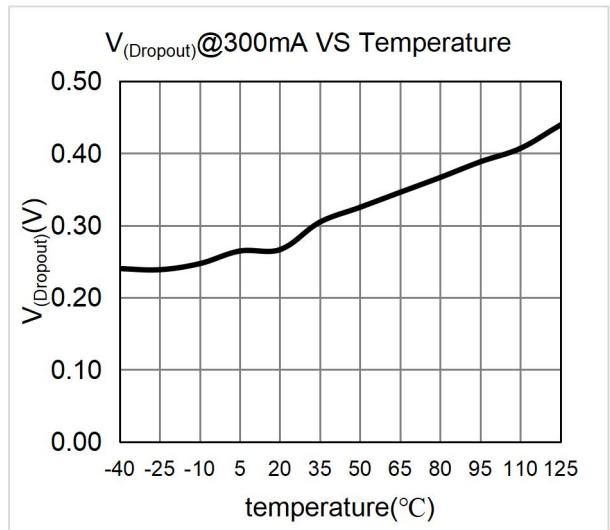

I_{EN}@14V VS Temperature
I_{EN}(uA)
0.25
0.2
0.15
0.1
0.05
0
-40 -25 -10 5 20 35 50 65 80 95 110 125
temperature(℃)


V_{OUT}@1mA VS Temperature
V_{OUT}(V)
5.1
5.05
5
4.95
4.9
4.85
4.8
-40 -25 -10 5 20 35 50 65 80 95 110 125
temperature(℃)

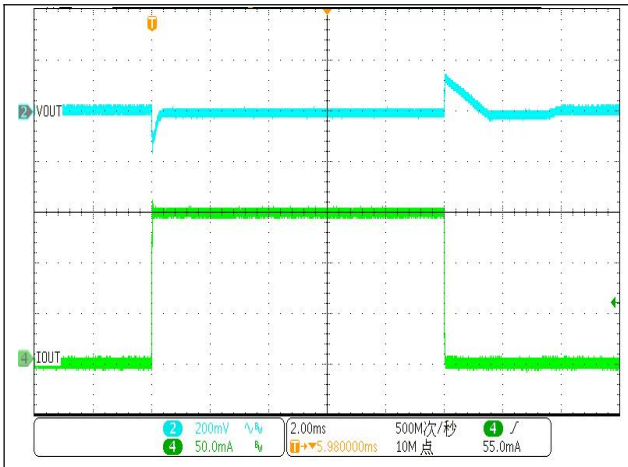

V_{OUT}@100mA VS Temperature
V_{OUT}(V)
5.1
5.05
5
4.95
4.9
4.85
4.8
4.75
-40 -25 -10 5 20 35 50 65 80 95 110 125
temperature(℃)


V_{OUT}@300mA VS Temperature
V_{OUT}(V)
5.1
5.05
5
4.95
4.9
4.85
4.8
4.75
-40 -25 -10 5 20 35 50 65 80 95 110 125
temperature(℃)

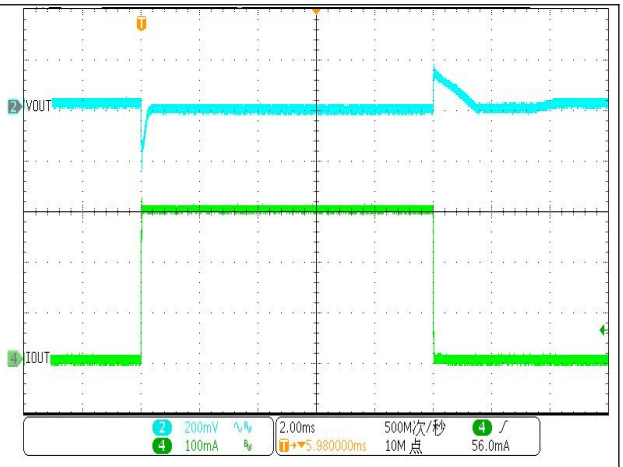

$V_{(Dropout)}$@100mA VS Temperature
$V_{(Dropout)}$(V)
0.16
0.14
0.12
0.10
0.08
0.06
0.04
0.02
0.00
-40 -25 -10 5 20 35 50 65 80 95 110 125
temperature(℃)


$V_{(Dropout)}$@300mA VS Temperature
$V_{(Dropout)}$(V)
0.50
0.40
0.30
0.20
0.10
0.00
-40 -25 -10 5 20 35 50 65 80 95 110 125
temperature(℃)

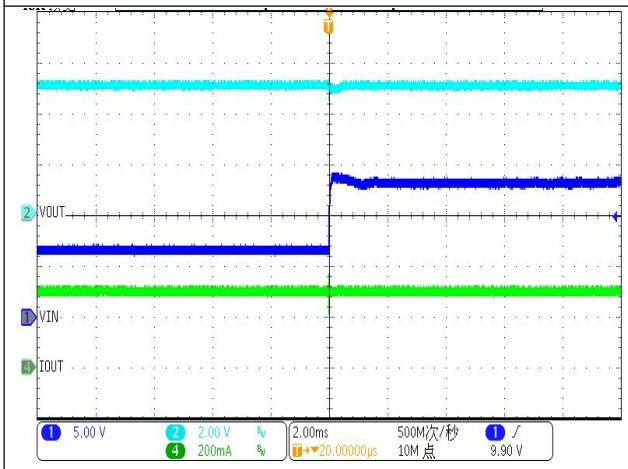
TYPICAL WAVEFORM



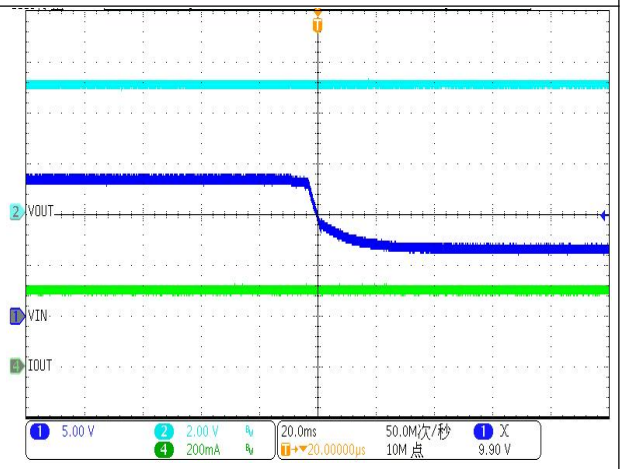
iOUT=1 <-> 150mA @ Vin=12V, Vout=5V



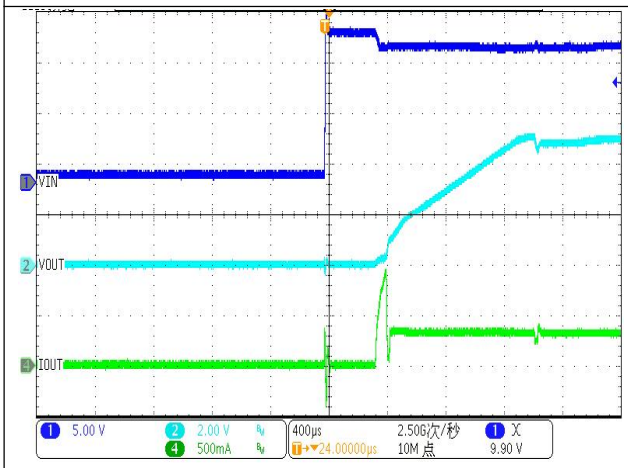
iOUT =1 <-> 300mA @ Vin=12V, Vout=5V



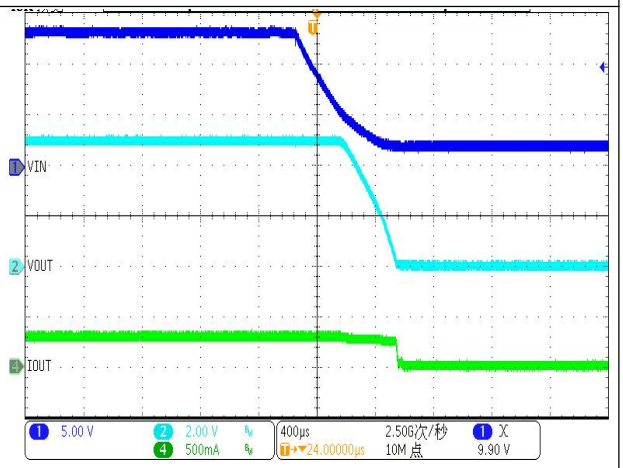
Line Transient 7 →14V vs @ Vout=5V, iOUT=300mA



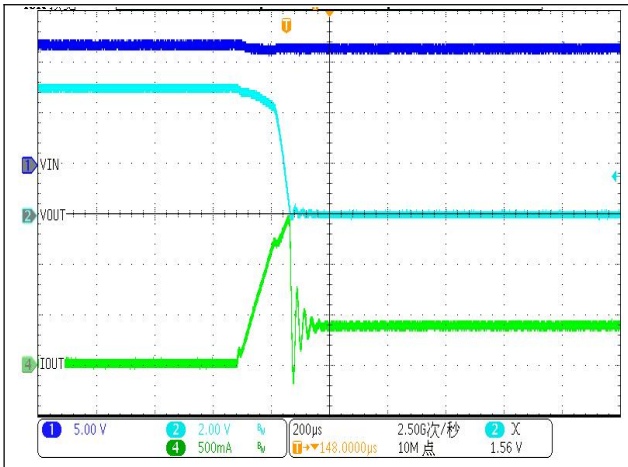
Line Transient 14V → 7V vs @ Vout=5V, iOUT=300mA



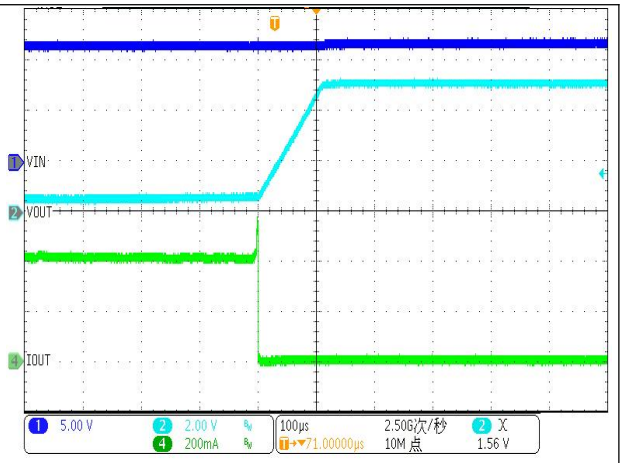
Power-Up @ Vin=VEN=14V, Vout=5V, Rload=16Ω



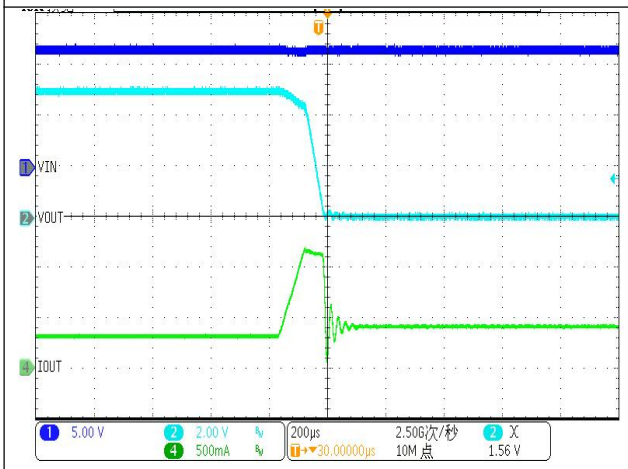
Power-OFF @ Vin=14V, Vout=5V, Rload=16Ω



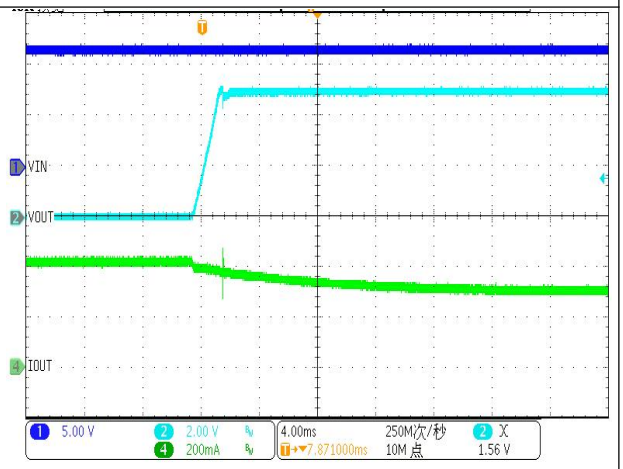
Short Circuit Entry @ no load



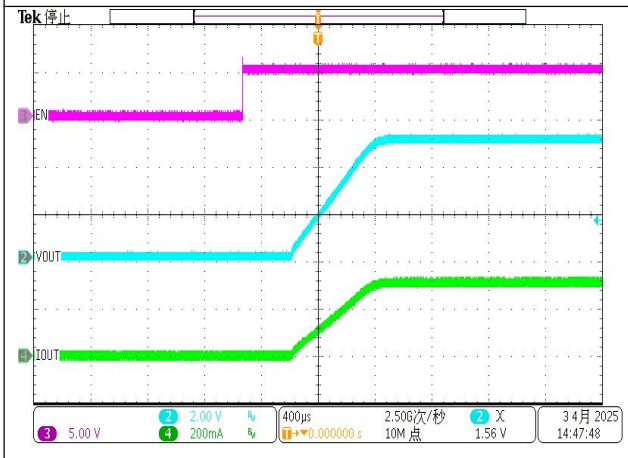
Short Circuit Recovery @ no load



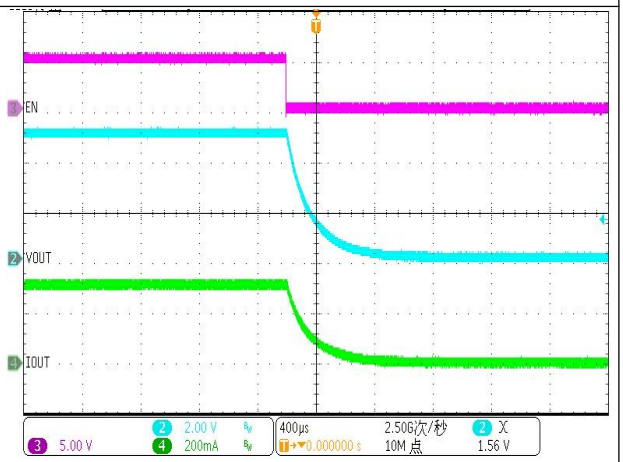
Short Circuit Entry @ IOUT=300mA



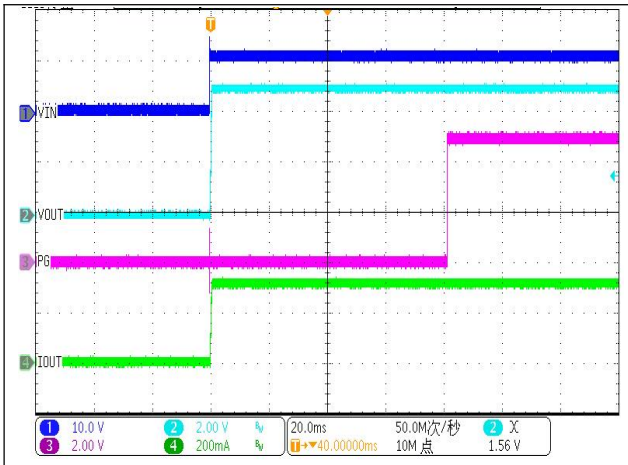
Short Circuit Recovery @ IOUT=300mA



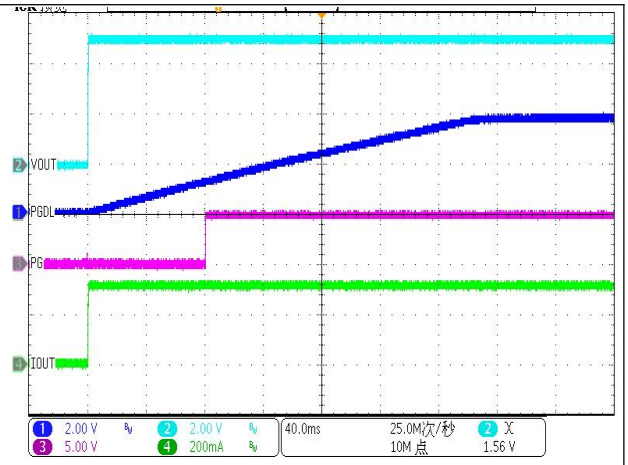
EN=L→H @ Vin=12V, Vout=5V, Rload=16Ω



EN=H→L @ Vin=12V, Vout=5V, Rload=16Ω



PG VS POWER UP@ Vin=12V, Vout=5V, IOUT=300mA，C_{PGDL}=100 nF



PGDL VS POWER UP@ Vin=12V, Vout=5V, IOUT=300mA，C_{PGDL}=100 nF

TYPICAL APPLICATION

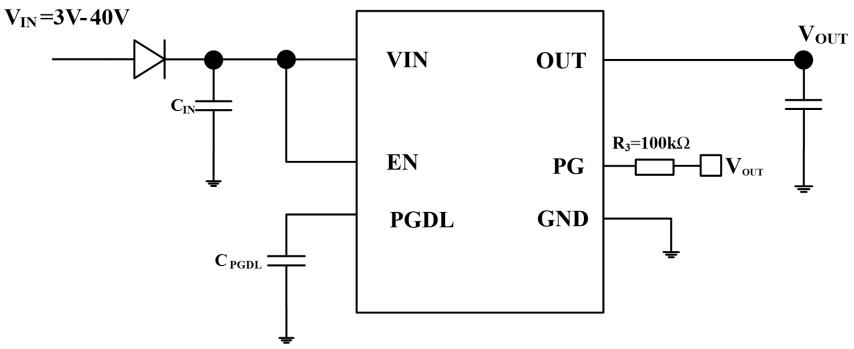


Figure 4 Application diagram of SIT14503QT/P & SIT14333QT/P

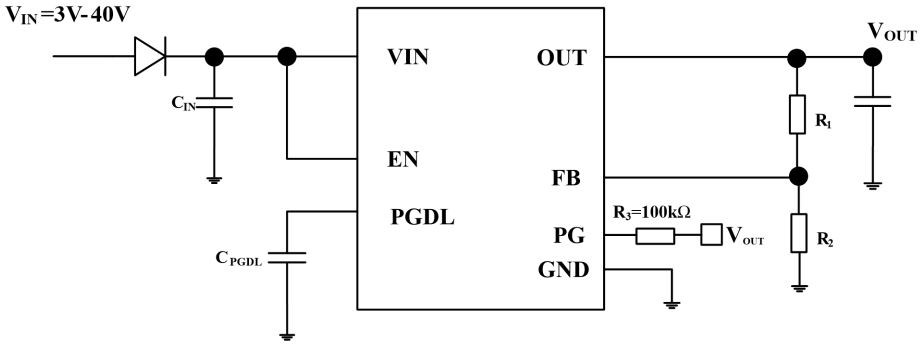


Figure 5 Application diagram of SIT14AJ3QT/P

Note:

1） When the VIN voltage is low, it is not recommended to use an input rectifier diode, as this will reduce the minimum operating voltage range of VIN.

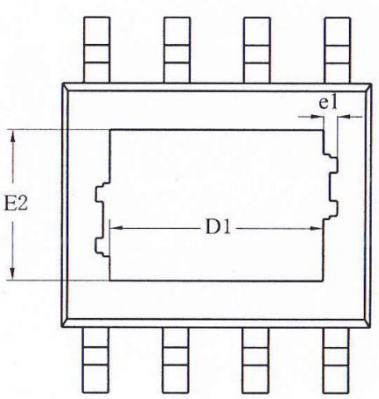
2） The output voltage in the figure is determined by the following formula: $V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) \times V_{FB}$. For the lower feedback resistor R2, we recommend using a 100kΩ resistor with tolerance ≤1% and temperature coefficient <100ppm/℃.

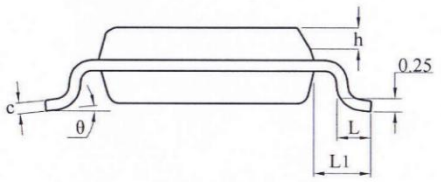
3） When VOUT rises to $V_{(PG\text{-}RISE)}$, the PG signal transitions to high after a delay of $t_{(DLY)}$). The delay time $t_{(DLY)}$ is determined by the capacitance C_{PGDL} connected between the PGDL pin and ground, calculated as: $C_{PGDL} = \frac{I_{(CHARGE)} \times t_{(DLY)}}{V_{(RISE)}}$。

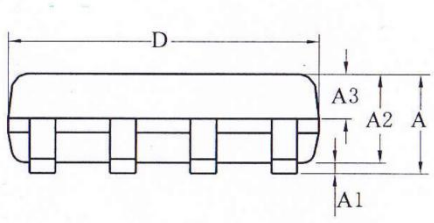
ESOP8 DIMENSIONS

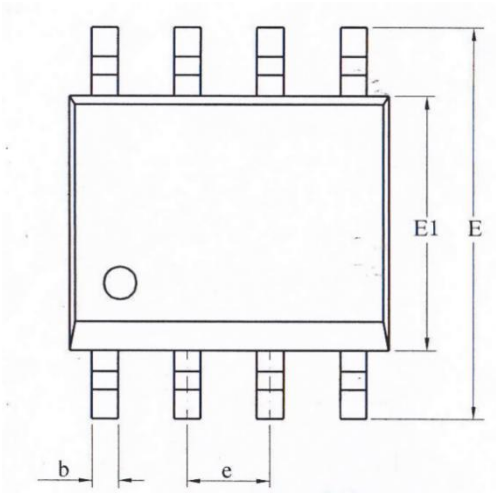
PACKAGE SIZE

SYMBOL	Min/mm	Nom/mm	Max/mm
A	-	-	1.65
A1	0.05	-	0.15
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
c	0.20	-	0.24
D	4.80	4.90	5.00
D1		2.09REF	
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2		2.09REF	
e		1.27BSC	
e1		0.16REF	
h	0.25	-	0.50
L	0.50	0.60	0.80
L1		1.05REF	
θ	0°	-	8°

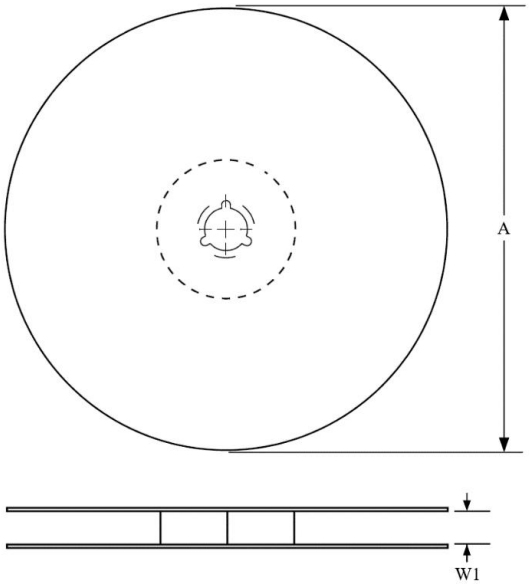




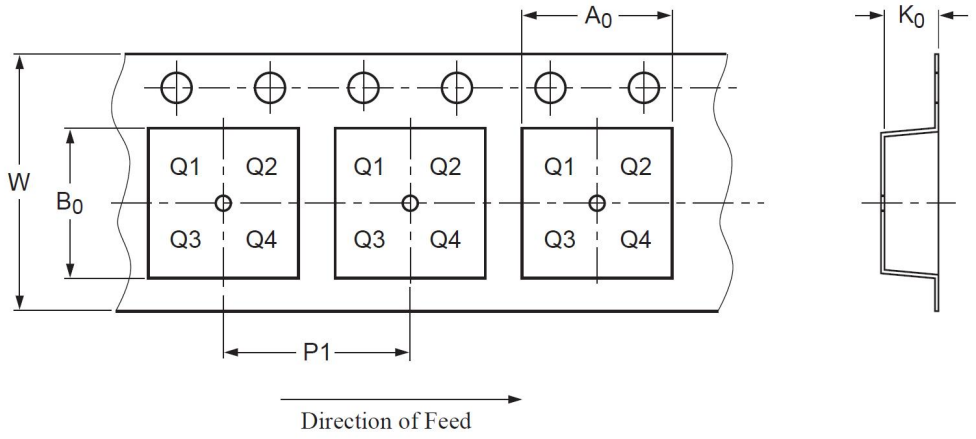




TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



PIN1 is in quadrant 1

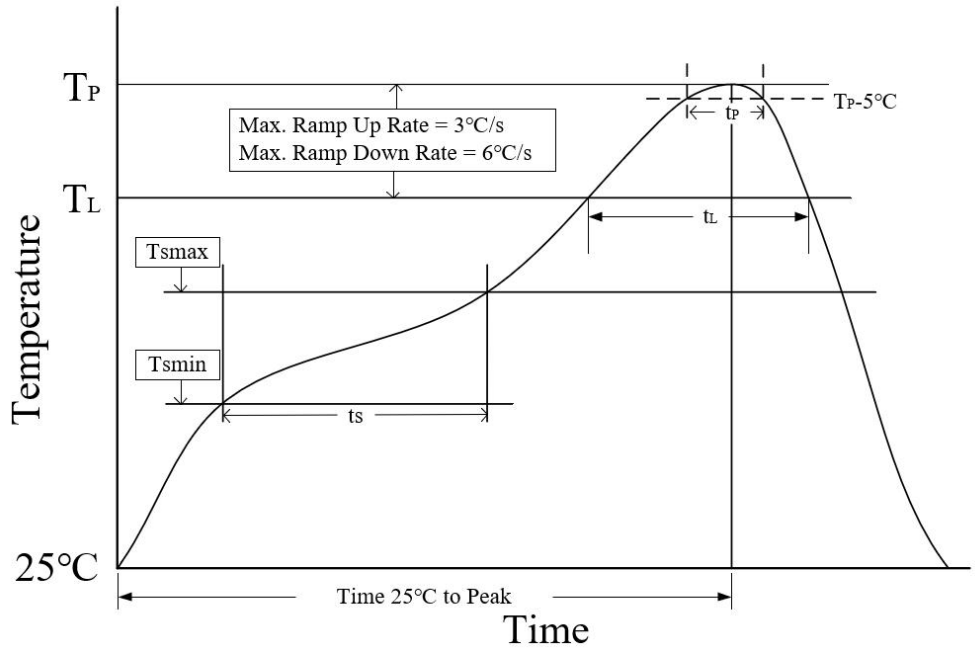
Package Type	Reel Diameter A (mm)	Tape Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
ESOP8	330±1	12.4	6.60±0.1	5.30±0.10	1.90±0.1	8.00±0.1	12.00±0.1

ORDERING INFORMATION

Type number	Output voltage	Output current	Package	MSL	Packing
SIT14503QT/P	5V	300mA	ESOP8	MSL 3	Tape and reel
SIT14333QT/P	3.3V	300mA	ESOP8	MSL 3	Tape and reel
SIT14AJ3QT/P	Adjustable	300mA	ESOP8	MSL 3	Tape and reel

2500 pieces/disc in taped packages.

REFLOW SOLDERING



Parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	3 °C/second max
Preheat time ts (T_{smin}=150 °C to T_{smax}=200 °C)	60-120 seconds
Melting time t_L (T_L=217 °C)	60-150 seconds
Peak temp T_P	260-265 °C
5 °C below peak temperature t_P	30 seconds
Ave cooling rate (T_P to T_L)	6 °C/second max
Normal temperature 25°Cto peak temperature T_P time	8 minutes max

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Datasheet status	Revision date
V1.0	Initial version.	April 2025
V1.1	Added maximum Cout and updated minimum value for improved stability; Adjusted the lower limit of the adjustable output version to support lower voltage applications; Refined package dimensions D1, E2, and e1 for the ESOP8 package.	August 2025
V1.2	Added “AEC-Q100 Grade 1 qualified”.	March 2026