DESCRIPTION

SIT1043Q is an interface chip designed to connect CAN protocol controllers with the physical bus. They are suitable for applications in automotive and industrial control fields, supporting 5Mbps flexible data-rate CAN FD. These chips enable differential signal transmission between the bus and the CAN protocol controller, and are fully compliant with the "ISO 11898" standard.

TYPICAL APPLICATIONS

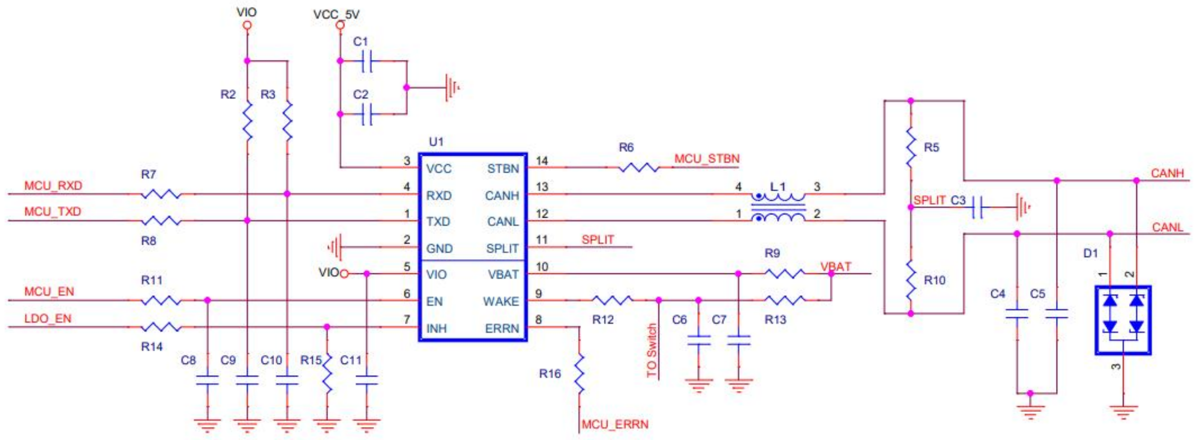

Figure 1-1

The peripheral circuit design for SIT1043Q is shown in Figure 1-1

1. VBAT is the input source; a series resistor R9 (1kΩ) is used to limit the input current to the transceiver during overvoltage events, and a 100nF capacitor (C7) helps filter out high-frequency noise in the line. These components should be placed close to the chip pins.

2. VCC is the input source, supplied with 5V; a 10μF capacitor (C1) is used to smooth voltage fluctuations, and a 100nF capacitor (C2) helps filter out high-frequency noise. These capacitors should be placed close to the chip pins.

3. VIO is the input source, supplied with 3.3V or 5V, shared with the MCU; a 100nF capacitor (C6) helps filter out high-frequency noise in the line. This capacitor should also be placed close to the chip pins.

4. Bus Termination: Figure 1-1 shows a split termination configuration. Split resistors R5 and R10 form the termination, with their midpoint connected to ground through capacitor C3. The split termination provides common-mode filtering for the bus. When an ECU acts as a bus termination node and is actively participating on the bus, extra care must be taken to ensure that the termination node is not removed from the bus, preventing the loss of termination.

5. Pin WAKE: To Switch to GND to enable local WAKE events. A series resistor R12 (33kΩ) is required to prevent overcurrent conditions and limit current into the WAKE pin. A pull-up resistor R13 (3.3kΩ) must provide sufficient current to ensure reliable wake-up event detection.

6. STBN is the standby control pin, active high. It is connected to the microcontroller through a series resistor R6 (10Ω~1kΩ).

7. EN is the enable control pin, active high. It is connected to the microcontroller through a series resistor R11 (10Ω~1kΩ), which helps limit current on the digital line during overvoltage faults. A grounding capacitor C8 (100nF~1μF) can be placed near the transceiver's input pin to assist in noise filtering.

8. INH is used to control the operating state of an external voltage regulator and is driven high upon a wake-up event. It is connected to the microcontroller through a series resistor R14 (10Ω~1kΩ) to limit overvoltage current. R15 (10kΩ~100kΩ) is a pull-down resistor from INH to GND; whether to include R15 and its specific value should be determined based on the state requirement of the enable pin of the external power supply IC.

9. ERRN is an error indication and power-on status output port, active low.

10. SPLIT is the common-mode stabilization output pin.

11. For the RXD pin, it is recommended to add an external pull-up resistor R3 with a value between 2.4kΩ and 10kΩ. Additionally, a series resistor R7 (10Ω~1kΩ) can be placed to limit input current to the transceiver during overvoltage conditions.

12. The TXD pin receives input signals from the controller to the transceiver. It is recommended to add an external pull-up resistor R2 with a value between 2.4kΩ and 10kΩ. A series resistor R8 (10Ω~1kΩ) can be added to limit input current during overvoltage events.

13. Protection and filtering components should be placed as close as possible to the bus connector to prevent transients, ESD, and noise propagation onto the PCB. As shown in Figure 1-1, a transient voltage suppressor (TVS) device D1 is used for enhanced protection, along with bus filter capacitors C4 and C5. Additionally, a common-mode choke (CMC) L1 can further improve EMC performance. Components should be arranged according to the signal path direction to ensure transient currents flow naturally toward protection devices without being forced off-path.

TVS Selection Guidelines:

1） ESD protection capability must meet the required level;

2） Maximum reverse working voltage (V_{RWM}) is 24V;

3） Junction capacitance (C_j) must comply with the signal transmission rate requirements of the system.

Recommended models for CAN communication rates of 250kbps and 500kbps: SITNE24V2BNQ-3/TR (SOT-23);

Recommended models for CAN communication rates of 2Mbps and 5Mbps: SITLE24V2BNQ-3/TR (SOT-23).

Recommended value for bus filter capacitors: 10pF to 100pF.

Recommended models for common-mode choke (CMC):

For CAN communication rates of 250kbps and 500kbps: ACT45B-101-2P;

For CAN communication rates of 2Mbps and 5Mbps: ACT1210R-101-2P.

PCB LAYOUT

To ensure optimal performance when applying the SIT1043Q, the following PCB layout guidelines should be observed:

❖ The length of the bus signal traces should not exceed 10cm.

❖ ESD protection devices should be placed close to the bus connection terminals of the ECU connector.

❖ Place decoupling capacitors for VBAT, VCC, VIO, STB, TXD, and RXD as close as possible to the transceiver pins, minimizing trace length.

❖ The routing distance between the communication controller and the transceiver should be minimized.

❖ Communication controller and transceiver should have as low grounding impedance as possible.

❖ Do not place filtering components between the grounds of the communication controller and the transceiver; their ground references must be the same.

❖ Avoid routing other signal lines parallel to CANH and CANL to prevent noise coupling into the CAN bus, which may disrupt communication.

❖ The layout beneath the CAN transmission line should not cross with other traces. It is recommended to place a ground plane underneath the trace whenever possible, with a minimum ground width of 1.5 to 2 times the spacing between CANH and CANL.

❖ CANH and CANL PCB traces should avoid vias as much as possible to minimize the inductive impact of vias on signal integrity.

❖ Surround surface-layer traces with grounding. Surface routing allows better impedance control and facilitates component addition or modification during later debugging stages.

❖ If longer routing is unavoidable, use 45-degree angled bends, which help reduce electromagnetic radiation. For high-speed differential traces, this routing method can improve radiation performance by more than 3dB.

❖ At least two vias should be used for decoupling capacitors and chip ground connections to reduce trace and via inductance.

REVISION HISTORY

Version Number	Revision Content	Revision Date
V1.0	Initial version.	April 2024
V1.1	Removed the pull-up resistor R4 for STBN and the pull-up resistor R1 for EN in Figure 1-1. Updated the explanation for item 6.	April 2025
V1.2	Added revision history.	March 2026