FEATURES

- Compatible with the ISO 11898-2:2024, SAE J2284-1 to SAE J2284-5 and SAE J1939-14 standard;
- Thermally protected;
- ±58V BUS protection;
- ±30V bus common mode voltage;
- Driver (TXD) and standby bus (BUS) dominant timeout function;
- Low-power standby mode with wake-up function;
- SIT1042GT/3 and SIT1042GTK/3 I/O can be interfaced directly to microcontrollers with supply voltages 1.8V, 3.3V and 5V;
- Undervoltage protection on VCC and VIO power supply pins;
- High-speed CAN, supporting the optimized 8Mbps Flexible Data-Rate (CAN FD);
- High Electro-Magnetic Immunity (EMI) and Low Electro-Magnetic Emission (EME);
- Unpowered state disengages from the bus;
- Available in SOP8 and leadless DFN3*3-8 packages.

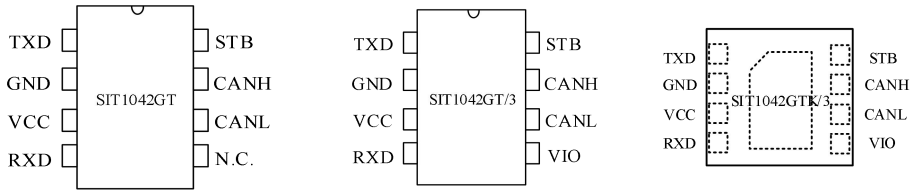
DESCRIPTION

SIT1042G is an interface chip used between the CAN protocol controller and the physical bus. It can be used for industrial control and other fields. It supports 8Mbps (CAN FD), and has the ability to perform differential signal transmission between bus and the CAN protocol controller.

The SIT1042G is fully compatible with the SIT1042, SIT1042A, and other family products. The SIT1042G is an upgraded version with improved EMC performance and lower electromagnetic radiation performance. In addition, the SIT1042G can support 1.8V MCU.

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Bus supply voltage	VCC	4.5	5.5	V
MCU side port supply voltage	VIO	1.7	5.5	V
CANH/CANL input or output voltage	V_{can}	-58	+58	V
Bus differential voltage	V_{diff}	1.5	3.0	V
Virtual junction temperature	T_j	-40	150	℃

PIN CONFIGURATION

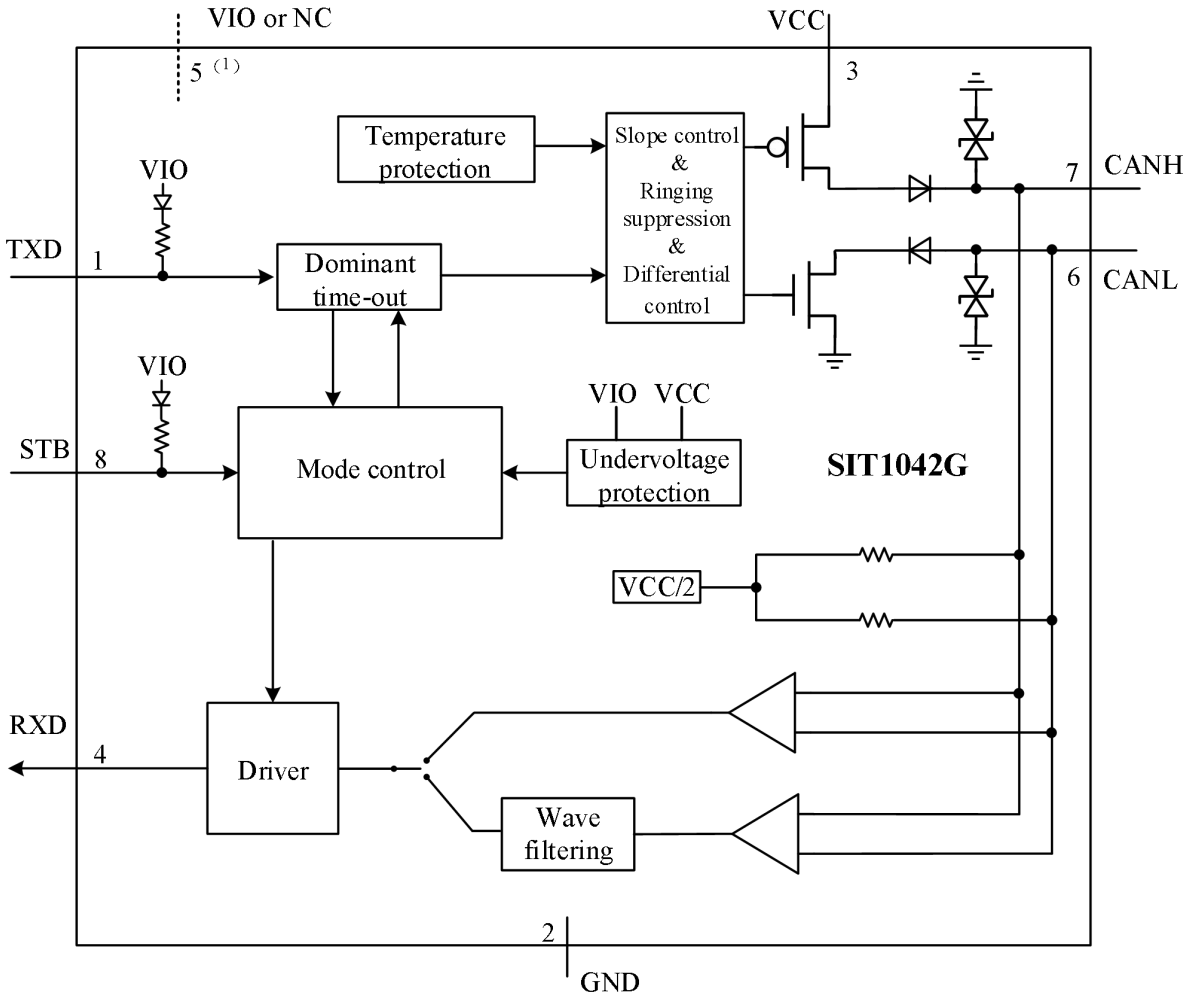


PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	TXD	transmit data input
2	GND	ground
3	VCC	supply voltage
4	RXD	receive data output
5	VIO	transceiver I/O level conversion power supply voltage (SIT1042GT/3 and SIT1042GTK/3 version)
5	NC	Not connected in SIT1042GT version
6	CANL	LOW-level CAN-bus line
7	CANH	HIGH-level CAN-bus line
8	STB	standby mode control input, low level is high speed mode

Note: The metal pad on the back of the DFN3*3-8 package is recommended to be grounded.

INTERNAL CIRCUIT BLOCK DIAGRAM



(1) VIO is only available in SIT1042GT/3 and SIT1042GTK/3 version, pin 5 is not connected in SIT1042GT version.

LIMITING VALUES

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
Supply voltage	V_{CC}, V_{IO}	pins VCC, VIO	-0.3~+7	V
MCU side port	V_{TXD}, V_{RXD}, V_{STB}	pins TXD, RXD, STB	-0.3~+7	V
Bus side input voltage	V_{CANH}，V_{CANL}	pins CANH, CANL	-58~+58	V
Bus differential breakdown voltage	$V_{CANH-CANL}$		-58~+58	V
Electrostatic discharge voltage	V_{ESD}	IEC 61000-4-2: on pins CANH, CANL	±10	kV
		Human-body model (HBM), per AEC Q100-002: all pins	±4	kV
		Human-body model (HBM), per AEC Q100-002: pins CANH and CANL with respect to GND	±6	kV
		Charged Device Model (CDM): all pins	±2000	V
Transient voltage	V_{trt}	Pulse 1	-100	V
		Pulse 2a	75	V
		Pulse 3a	-150	V
		Pulse 3b	100	V
Storage temperature	T_{stg}		-55~150	℃
Virtual junction temperature	T_j		-40~150	℃

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	SOP8	95	℃/W
		DFN3*3-8	65	℃/W
$R_{\theta JC}$	Junction-to-case thermal resistance	SOP8	46	℃/W
		DFN3*3-8	35	℃/W

DRIVER ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CANH dominant output voltage	$V_{OH(D)}$	Normal mode, V_{TXD}=0V, R_L=50Ω to 65Ω	2.75	3.5	4.5	V
CANL dominant output voltage	$V_{OL(D)}$		0.5	1.5	2.25	V
Bus dominant differential output voltage	$V_{OD(D)}$	Normal mode, V_{TXD}=0V, R_L=50Ω to 65Ω	1.5	-	3	V
		Normal mode, V_{TXD}=0V, R_L=45Ω to 70Ω	1.4	-	3.3	V
		Normal mode, V_{TXD}=0V, R_L=2240Ω	1.5	-	5	V
Bus recessive output voltage	$V_{O(R)}$	Normal mode, V_{TXD}=V_{IO}, No load	2	0.5V_{CC}	3	V
		Normal mode, V_{TXD}=V_{IO}, R_L=60Ω	2.2	0.5V_{CC}	2.8	V
Bus recessive differential output voltage	$V_{OD(R)}$	Normal mode, V_{TXD}=V_{IO}, No load	-50	-	50	mV
		Normal mode, V_{TXD}=V_{IO}, R_L=60Ω	-50	-	50	mV
Bus output voltage (Bus is biased to ground)	$V_{O(S)}$	Standby mode, No load	-0.1	-	0.1	V
Bus differential output voltage (Bus is biased to ground)	$V_{OD(S)}$	Standby mode, No load	-0.2	-	0.2	V
Transmitter dominant voltage symmetry	$V_{dom(TX)sym}$	$V_{dom(TX)sym}$=V_{CC}- V_{CANH} - V_{CANL}	-400	-	400	mV
Transmitter voltage symmetry	V_{TXsym} (1)	V_{TXsym}=V_{CANH} + V_{CANL}, R_L=60Ω, C_{SPLIT}=4.7Nf, f_{TXD}=250kHz, 1MHz, 2.5MHz **Figure 5**	0.9V_{CC}	-	1.1V_{CC}	V
Dominant-recessive common-mode output voltage difference	$V_{cm(step)}$	**Figure 3** & **Figure 5**	-150	-	150	mV
Dominant-recessive common-mode peak-to-peak	$V_{cm(p-p)}$ (1)	**Figure 3** & **Figure 5**	-300	-	300	mV

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Dominant Short-circuit output current	$I_{O(SC)DOM}$	Normal mode, V_{TXD}=0V, V_{CANH}=-15V to 40V	-100	-	-	mA
		Normal mode, V_{TXD}=0V, V_{CANL}=-15V to 40V	-	-	100	mA
Recessive Short-circuit output current	$I_{O(SC)REC}$	Normal mode, V_{TXD}=V_{IO}, V_{CANH}=V_{CANL}=-27V to 32V	-3	-	3	mA

Unless otherwise stated, all typical values are measured at 25°C, supply voltage V_{CC}=5V, V_{IO}=5V (if applicable), R_L=60Ω.

(1) Not tested in production, guaranteed by design.

DRIVER SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Propagation delay time, low-to-high level output	$t_{d(TXD-busdom)}$	Normal mode, **Figure 1 & Figure 4**	-	-	80	ns
Propagation delay time, high-to-low level output	$t_{d(TXD-busrec)}$	Normal mode, **Figure 1 & Figure 4**	-	-	80	ns
Differential output signal rise time	$t_{r(BUS)}$		-	30	-	ns
Differential output signal fall time	$t_{f(BUS)}$		-	30	-	ns

Unless otherwise stated, all typical values are measured at 25°C, supply voltage V_{CC}=5V, V_{IO}=5V (if applicable), R_L=60Ω.

RECEIVER ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiver threshold voltage	$V_{th(RX)dif}$	Normal mode, -30V<V_{CM}< 30V	0.5	-	0.9	V
		Standby mode, -12V<V_{CM}< 12V	0.4	-	1.1	V
Receiver threshold voltage hysteresis range	$V_{hys(RX)dif}$	Normal mode, -30V<V_{CM}< 30V	-	80	-	mV
Receiver recessive voltage range	$V_{rec(RX)}$	Normal mode, -30V<V_{CM}< 30V	-3	-	0.5	V
		Standby mode, -12V<V_{CM}< 12V	-3	-	0.4	V

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiver dominant voltage range	$V_{dom(RX)}$	Normal mode, -30V<V_{CM}< 30V	0.9	-	8	V
		Standby mode, -12V<V_{CM}< 12V	1.1	-	8	V
Bus leakage current	I_L	V_{CC}=V_{IO}=0V, V_{CANH}=V_{CANL}=5V, T_{amb}<105°C	-10	-	10	μA
CANH, CANL input resistance	R_{IN}	-2V≤V_{CANH}≤7V -2V≤V_{CANL}≤7V	25	40	50	kΩ
CANH, CANL differential-input resistance	R_{ID}	-2V≤V_{CANH}≤7V -2V≤V_{CANL}≤7V	50	80	100	kΩ
CANH, CANL input resistance mismatch	$\triangle R_{IN}$	0V≤V_{CANH}≤5V 0V≤V_{CANL}≤5V	-2	-	2	%
CANH, CANL input capacitance to ground	C_{IN} (1)	V_{TXD}=V_{IO}	-	-	40	pF
CANH, CANL differential-input capacitance	C_{ID} (1)	V_{TXD}=V_{IO}	-	-	20	pF
Slew Rate	SR (1)	**Figure 4**	-	-	70	V/μs

Unless otherwise stated, all typical values are measured at 25°C, supply voltage V_{CC}=5V, V_{IO}=5V (if applicable), R_L=60Ω.

(1) Not tested in production, guaranteed by design.

RECEIVER SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Propagation delay time, low-to-high level output	$t_{d(busdom-RXD)}$	Normal mode, **Figure 1 & Figure 4**	-	-	110	ns
Propagation delay time, low-to-high level output	$t_{d(busrec-RXD)}$	Normal mode, **Figure 1 & Figure 4**	-	-	110	ns
RXD signal rise time	$t_{r(RXD)}$		-	8	-	ns
RXD signal fall time	$t_{f(RXD)}$		-	8	-	ns

Unless otherwise stated, all typical values are measured at 25°C, supply voltage V_{CC}=5V, V_{IO}=5V (if applicable), R_L=60Ω.

DEVICE SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Loop delay 1, TXD falling edge to RXD falling edge	t_{loop1}	Normal mode, **Figure 1** & **Figure 4**	40	-	190	ns
Loop delay 2, TXD rising edge to RXD rising edge	t_{loop2}	Normal mode, **Figure 1** & **Figure 4**	40	-	190	ns
Transmitted recessive bit width deviation	$\Delta t_{bit(BUS)}$	According to ISO 11898-2:2024 set B, **Figure 2** & **Figure 4**				
		$\Delta t_{bit(BUS)}= t_{bit(BUS)} - t_{bit(TXD)}$	-45	-	10	ns
		According to ISO 11898-2:2024 set C, **Figure 2** & **Figure 4**				
		$\Delta t_{bit(BUS)}= t_{bit(BUS)} - t_{bit(TXD)}$	-10	-	10	ns
Receiver timing symmetry	Δt_{rec}	According to ISO 11898-2:2024 set B, **Figure 2** & **Figure 4**				
		$\Delta t_{rec}= t_{bit(RXD)} - t_{bit(BUS)}$	-45	-	15	ns
		According to ISO 11898-2:2024 set C, **Figure 2** & **Figure 4**				
		$\Delta t_{rec}= t_{bit(RXD)} - t_{bit(BUS)}$	-20	-	15	ns
Received recessive bit width deviation	$\Delta t_{bit(RXD)}$	According to ISO 11898-2:2024 set C, **Figure 2** & **Figure 4**				
		$\Delta t_{bit(RXD)}= t_{bit(RXD)} - t_{bit(TXD)}$	-80	-	20	ns
		According to ISO 11898-2:2024 set B, **Figure 2** & **Figure 4**				
		$\Delta t_{bit(RXD)}= t_{bit(RXD)} - t_{bit(TXD)}$	-30	-	20	ns
TXD dominant timeout	$t_{dom(TXD)}$		0.8	2	6	ms
BUS dominant timeout	$t_{dom(BUS)}$		0.8	2	6	ms
Enable time from standby mode to normal mode	t_{mode}		-	-	10	µs
Bus dominant wake-up filter time	$t_{wake(dom)}$		0.5	-	1.8	µs
Bus recessive wake-up filter time	$t_{wake(rec)}$		0.5	-	1.8	µs

Unless otherwise stated, all typical values are measured at 25°C, supply voltage V_{CC}=5V, V_{IO}=5V (if applicable), R_L=60Ω.

(1) Not tested in production, guaranteed by design.

TXD PIN CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Leakage current of TXD without power	$I_O(off)$	V_{CC}=V_{IO}=0V, V_{TXD}=5.5V	-1	-	1	µA

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HIGH-level input voltage	V_{IH}	SIT1042GT/3 SIT1042GTK/3	$0.7V_{IO}$	-	V_{IO}+0.3	V
LOW-level input voltage	V_{IL}	SIT1042GT/3 SIT1042GTK/3	-0.3	-	$0.3V_{IO}$	V
HIGH-level input voltage	V_{IH}	SIT1042GT	2	-	V_{CC}+0.3	V
LOW-level input voltage	V_{IL}	SIT1042GT	-0.3	-	0.8	V
Pull-up resistance	R_{pu}	$2.8V<V_{IO}<5.5V$	20	-	80	kΩ
Open voltage on TXD pin	TXD_O		H			logic

Unless otherwise stated, all typical values are measured at 25°C, supply voltage V_{CC}=5V, V_{IO}=5V (if applicable), R_L=60Ω.

STB PIN CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Leakage current of STB without power	I_O(off)	$V_{CC}=V_{IO}$=0V， V_{STB}=5.5V	-1	-	1	μA
HIGH-level input voltage	V_{IH}	SIT1042GT/3 SIT1042GTK/3	$0.7V_{IO}$	-	V_{IO}+0.3	V
LOW-level input voltage	V_{IL}	SIT1042GT/3 SIT1042GTK/3	-0.3	-	$0.3V_{IO}$	V
HIGH-level input voltage	V_{IH}	SIT1042GT	2	-	V_{CC}+0.3	V
LOW-level input voltage	V_{IL}	SIT1042GT	-0.3	-	0.8	V
Pull-up resistance	R_{pu}	$2.8V<V_{IO}<5.5V$	20	-	80	kΩ
Open voltage on STB pin	STB_O		H			logic

Unless otherwise stated, all typical values are measured at 25°C, supply voltage V_{CC}=5V, V_{IO}=5V (if applicable), R_L=60Ω.

RXD PIN CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HIGH-level output current	I_{OH}(RXD)	$V_{RXD}=V_{IO}$-0.4V, Bus recessive	-10	-5	-1	mA
LOW-level output current	I_{OL}(RXD)	V_{RXD}=0.4V, Bus dominant	1	5	10	mA
Leakage current of RXD without power	I_O(off)	$V_{CC}=V_{IO}$=0V, V_{RXD}=5.5V	-5	-	5	μA

Unless otherwise stated, all typical values are measured at 25°C, supply voltage V_{CC}=5V, V_{IO}=5V (if applicable), R_L=60Ω.

SUPPLY CURRENT

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VCC supply current	I_{CC_DOM}	Normal mode, dominant	-	42	70	mA
	I_{CC_REC}	Normal mode, recessive	-	5	10	mA
	$I_{CC\_DOM\_S}$	Dominant; short circuit on bus lines; -3V<(V_{CANH}=V_{CANL})<40V	-	-	109	mA
	I_{CC_STB}	Standby mode, V_{STB}=V_{TXD}=V_{IO}, (SIT1042GT/3 and SIT1042GTK/3)	-	-	4	μA
	I_{CC_STB}	Standby mode, V_{STB}=V_{TXD}=V_{CC}, (SIT1042GT)	-	-	26	μA
VIO supply current	I_{IO_DOM}	Normal mode, dominant	-	240	420	μA
	I_{IO_REC}	Normal mode, recessive	-	120	240	μA
	I_{IO_STB}	Standby mode, V_{STB}=V_{TXD}=V_{IO}	-	12	24	μA

Unless otherwise stated, all typical values are measured at 25°C, supply voltage V_{CC}=5V, V_{IO}=5V (if applicable), R_L=60Ω.

OVER TEMPERATURE PROTECTION

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Shutdown junction temperature	$T_{j(sd)}$ (1)		-	190	-	℃

Unless otherwise stated, all typical values are measured at 25°C, supply voltage V_{CC}=5V, V_{IO}=5V (if applicable), R_L=60Ω.

(1) Not tested in production, guaranteed by design.

UNDERVOLTAGE PROTECTION

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VCC undervoltage protection	V_{UVD_VCC}		3.7	-	4.3	V
VIO undervoltage protection	V_{UVD_VIO}		1.4	-	1.65	V

Unless otherwise stated, all typical values are measured at 25°C, supply voltage V_{CC}=5V, V_{IO}=5V (if applicable), R_L=60Ω.

FUNCTION TABLE

Table 1 CAN TRANSCEIVER TRUTH TABLE

TXD (1)	STB (1)	CANH (1)	CANL (1)	BUS STATE	RXD (1)
L	L	H	L	Dominate	L
H or Open	L	$0.5V_{CC}$	$0.5V_{CC}$	Recessive	H
X	H or Open	GND	GND	Recessive	H

(1) H=high level; L=low level; X=irrelevant.

Table 2 RECEIVER FUNCTION TABLE

OPERATING MODE	$V_{ID}=V_{CANH}-V_{CANL}$	BUS STATE	RXD (1)
Normal mode	$V_{ID}\geq 0.9V$	Dominate	L
	$0.5<V_{ID}<0.9V$	?	?
	$V_{ID}\leq 0.5V$	Recessive	H
Standby mode	$V_{ID}\geq 1.1V$	Dominate	L
	$0.4<V_{ID}<1.1V$	?	?
	$V_{ID}\leq 0.4V$	Recessive	H

(1) H=high level; L=low level; ?=uncertain.

Table 3 UNDERVOLTAGE PROTECTION STATUS TABLE

VCC	VIO (1)	BUS STATE	BUS OUTPUT (2)	RXD (2)
$V_{CC}>V_{uvd\_VCC}$	$V_{IO}>V_{uvd\_VIO}$	Normal	According to STB and TXD	Follow the bus
$V_{CC}<V_{uvd\_VCC}$	$V_{IO}>V_{uvd\_VIO}$	Protected status	GND	H
$V_{CC}>V_{uvd\_VCC}$	$V_{IO}<V_{uvd\_VIO}$	Protected status	Z	Z
$V_{CC}<V_{uvd\_VCC}$	$V_{IO}<V_{uvd\_VIO}$	Protected status	Z	Z

(1) SIT1042GT/3 and SIT1042GTK/3 version only;

(2) H=high level; Z=high ohmic.

TIMING WAVEFORM

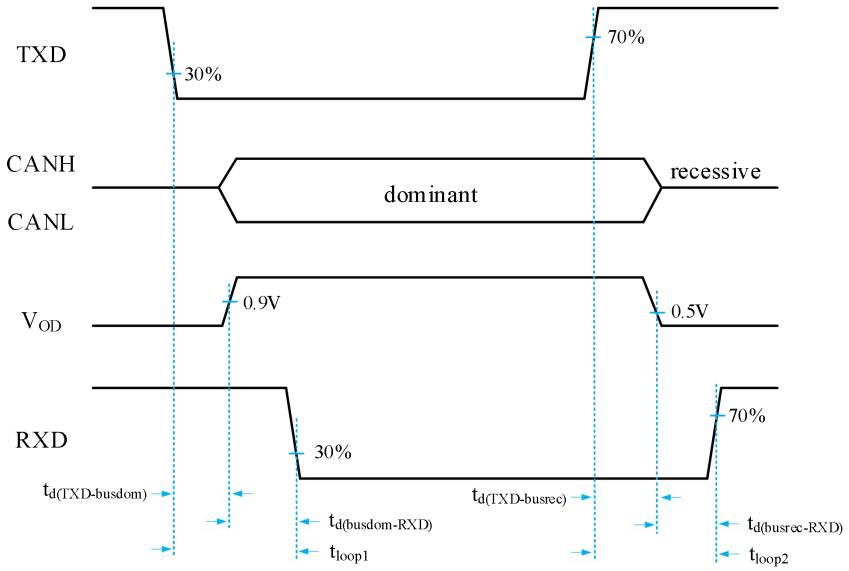


Figure 1 Transceiver transmission delay

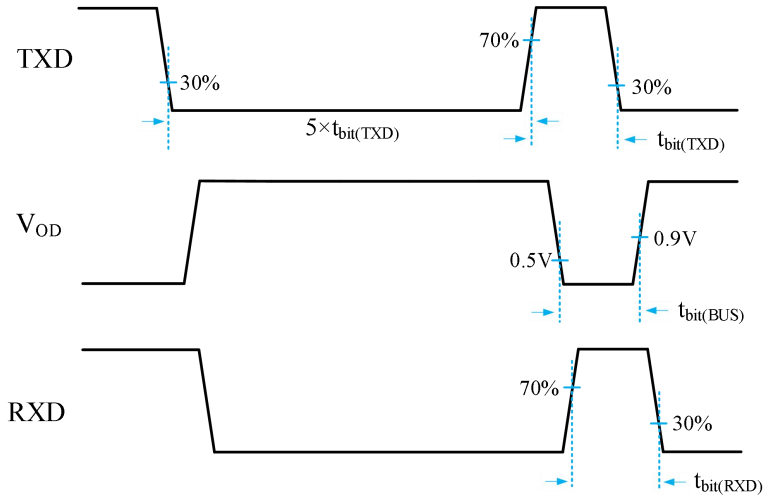


Figure 2 t_{bit} delay

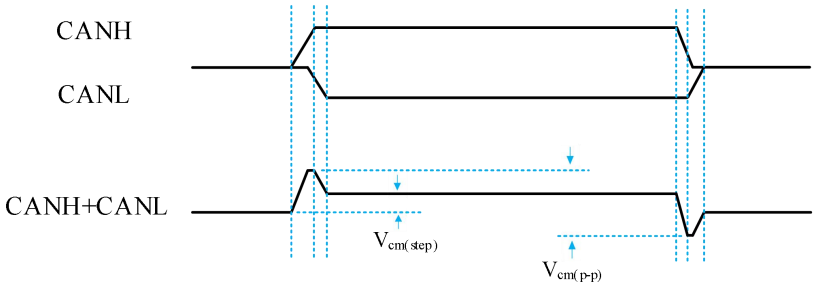


Figure 3 Bus common-mode voltage (SAE 1939-14)

TEST CIRCUIT

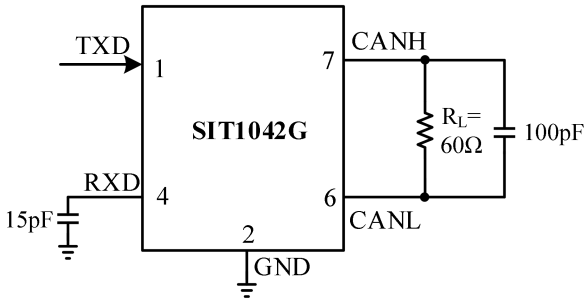


Figure 4 Transceiver timing sequence test circuit

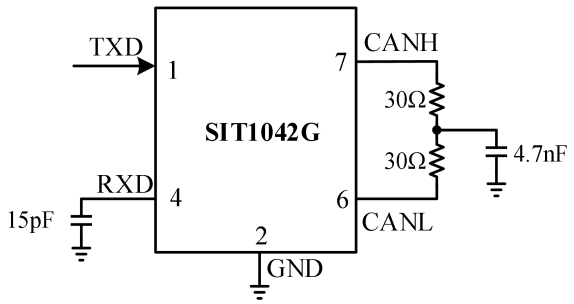


Figure 5 Transceiver bus symmetry test circuit

TYPICAL APPLICATION DIAGRAM

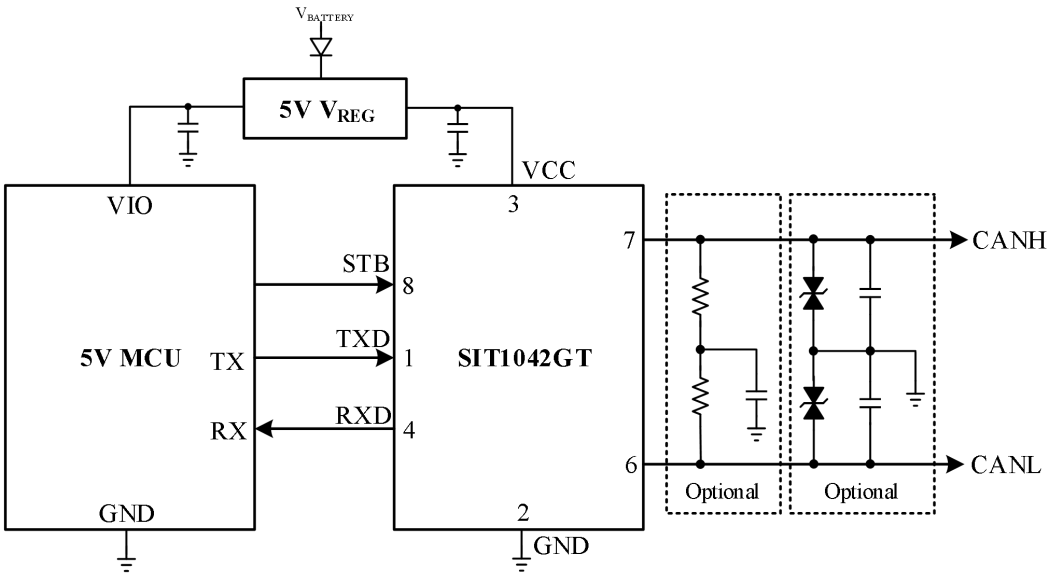


Figure 6 SIT1042GT and 5V MCU typical application diagram

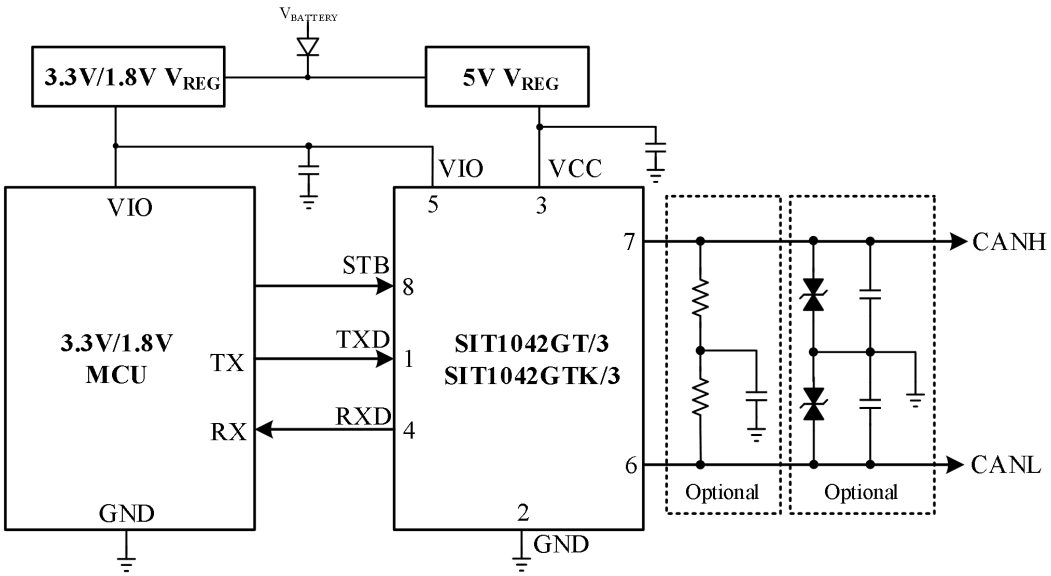


Figure 7 SIT1042GT/3, SIT1042GTK/3 and 1.8V/3.3V MCU typical application diagram

ADDITIONAL DESCRIPTION

1 Sketch

SIT1042G is an interface chip applied between the CAN protocol controller and the physical bus. It can be used for industrial control and other fields. It supports 8Mbps flexible data rate (CAN FD) and has the ability to transmit differential signals between the bus and the CAN protocol controller. Fully compatible with ISO 11898-2:2024 standard.

2 Short-circuit protection

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

3 Over temperature protection

The SIT1042G features over-temperature protection functionality. When triggered, the current at the driver stage will be reduced since the driver transistor is the primary power-consuming component. This current reduction helps decrease power consumption and consequently lowers the chip temperature. Meanwhile, all other sections of the chip remain fully operational.

4 Undervoltage protection

The SIT1042G power supply pin has an undervoltage detection function, which can put the device in a protected mode. This protects the bus when V_{CC} is lower than $Vuvd\_{VCC}$ or V_{IO} is lower than $Vuvd\_{VIO}$ (if applicable).

5 Control mode

The SIT1042G provides two modes of operation which are selectable via pin STB: High-speed mode and standby mode.

High-speed mode is the normal operating mode, selected by grounding the STB pin. Both the CAN driver and receiver operate fully normally, enabling bidirectional CAN communication.

Set pin STB to high level or floating to activate low-power standby mode. Both CAN driver and receiver are shut down to reduce system power consumption. Standby mode activates a low-power receiver and wake-up filter; once the low-power receiver detects a dominant bus level exceeding t_{wake}, pin RXD will follow the bus. (In SIT1042GT/3 and SIT1042GTK/3 the low-power receiver can still detect dominant/recessive levels on the bus even when V_{CC} is undervoltage or floating, as long as V_{IO} is normally powered.)

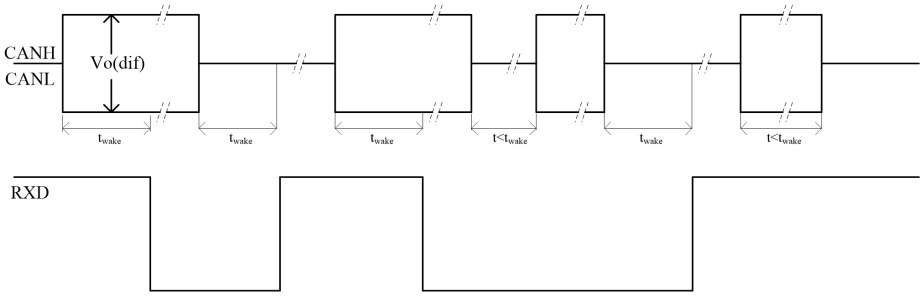


Figure 8 Wake-up timing

6 TXD dominant time-out function

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a falling edge on pin TXD.

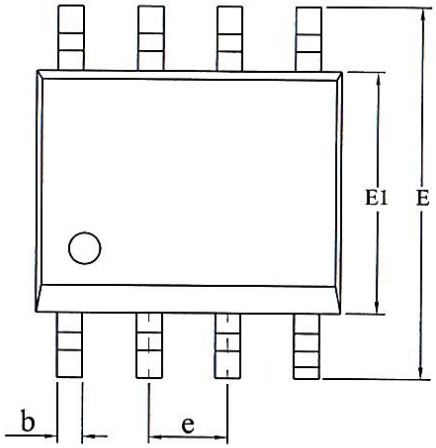
If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{dom}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a rising edge on pin TXD.

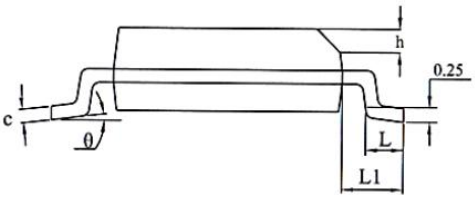
In standby mode, the pin RXD is forced to high if the bus becomes dominant and lasts longer than (t_{dom_BUS}), which can prevent permanent wakeup due to a short circuit in the bus or the failure of another node on the network. It can be reset when the bus changes from dominant to recessive.

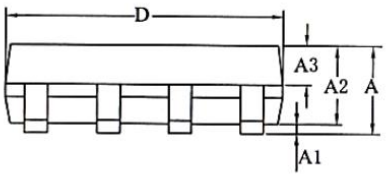
SOP8 DIMENSIONS

PACKAGE SIZE

SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	1.40	-	1.80
A1	0.10	-	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.38	-	0.51
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.40	0.60	0.80
L1	1.05REF		
c	0.20	-	0.25
θ	0°	-	8°



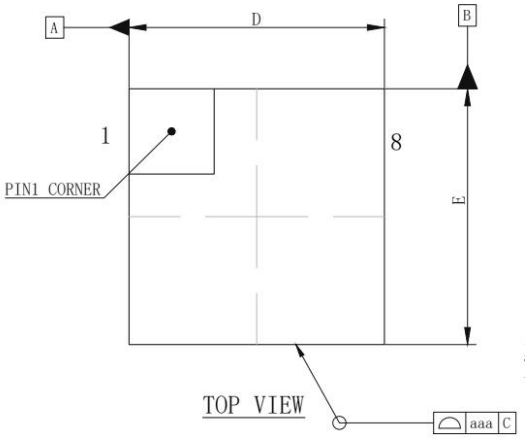


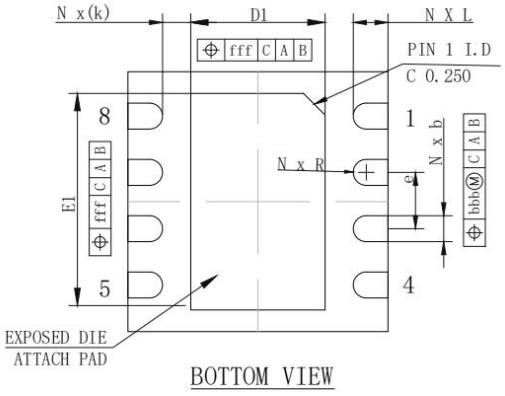


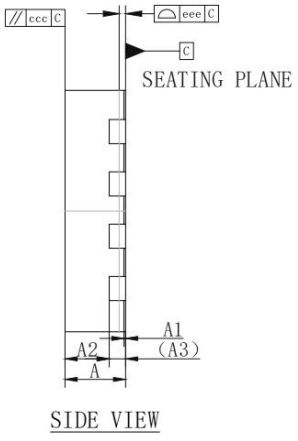
DFN3*3-8 DIMENSIONS

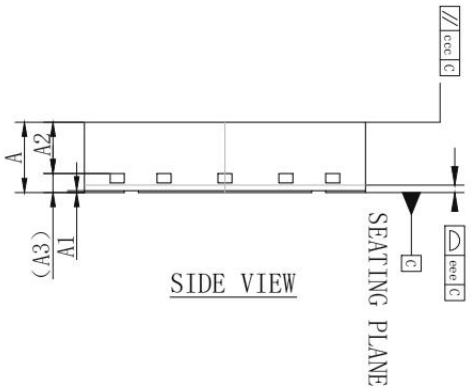
PACKAGE SIZE

SYMBOL	MIN/mm	TYP /mm	MAX/mm
D	2.900	3.000	3.100
E	2.900	3.000	3.100
E1	1.450	1.550	1.650
D1	2.400	2.500	2.600
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A2	0.497	0.547	0.597
A3	0.203 REF		
b	0.250	0.300	0.350
e	0.65 BSC		
k	0.325 REF		
L	0.350	0.400	0.450
aaa	0.100		
ccc	0.100		
eee	0.080		
bbb	0.070		
fff	0.100		

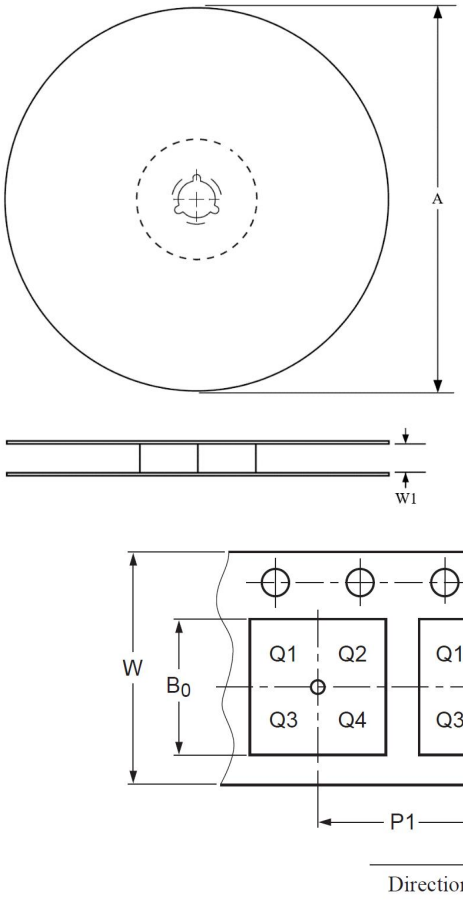








TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

PIN1 is in quadrant 1

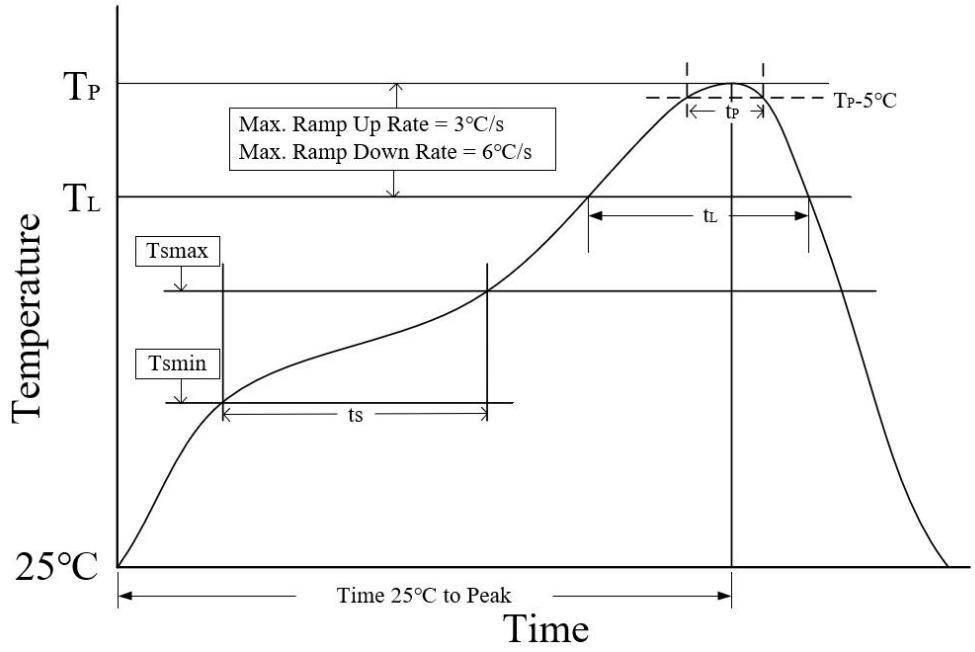
Package Type	Reel Diameter A (mm)	Tape Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
SOP8	330±1	12.4	6.60±0.1	5.30±0.10	1.90±0.1	8.00±0.1	12.00±0.1
DFN3*3-8	329±1	12.4	3.30±0.1	3.30±0.1	1.10±0.1	8.00±0.1	12.00±0.3

ORDERING INFORMATION

Type number	Package	MSL	Packing
SIT1042GT	SOP8	MSL3	Tape and reel
SIT1042GT/3	SOP8	MSL3	Tape and reel
SIT1042GTK/3	DFN3*3-8, small shape, no leads, 8 terminals	MSL3	Tape and reel

SOP8 is packed with 2500 pieces/disc in braided packaging. Leadless DFN3*3-8 is packed with 6000 pieces/disc in braided packaging.

REFLOW SOLDERING



Parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	3 °C/second max
Preheat time ts (T_{smin}=150 °C to T_{smax}=200 °C)	60-120 seconds
Melting time t_L (T_L=217 °C)	60-150 seconds
Peak temp T_P	260-265 °C
5°C below peak temperature t_P	30 seconds
Ave cooling rate (T_P to T_L)	6 °C/second max
Normal temperature 25°C to peak temperature T_P time	8 minutes max

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Data sheet status	Revision Date
V1.0	Initial version.	April 2026
V1.1	Optimized Flexible Data-Rate; Added the parameter of Slew Rate; Deleted $t_{bit(BUS)}$, $t_{bit(RXD)}$; Added CAN FD timing characteristic specifications that meet ISO 11898-2:2024 set C requirements; Deleted the type number SIT1042GTK.	August 2026