FEATURES

- ISO 11898-2:2024, SAE J2284-1 to SAE J2284-5 and SAE J1939-14 compliant
- Low power Sleep mode and Standby mode
- Remote wake-up function and local wake-up function
- ±58V BUS protection
- ±30V receiver common mode input voltage
- IO pins support 1.8V, 3.3V or 5V MCU
- Driver (TXD) dominant timeout function
- Undervoltage protection on VBAT, VCC and VIO pins
- High-speed CAN, support 5Mbps CAN With Flexible Data-Rate
- Sleep mode INH output pin with power disable function
- -40℃ to 150℃ junction temperature range with overtemperature protection
- High Electro-Magnetic Immunity (EMI) and Low Electro-Magnetic Emission (EME)
- Unpowered state disengages from the bus
- Available in SOP14 and Leadless DFN4.5×3.0-14 packages; DFN4.5×3.0-14 with improved Automated Optical Inspection (AOI) capability

DESCRIPTION

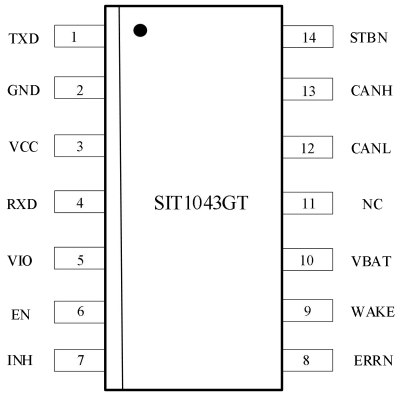
SIT1043G is an interface chip applied between CAN protocol controller and physical bus, supports 5Mbps Flexible Data-Rate, and has the capability of differential signal transmission between bus and CAN protocol controller. SIT1043G applied for 12 V or 24V application system, which features a CAN bus fault protection from -58V to +58V, and the receiver common mode input voltage can reach -30V to +30V. The SIT1043G is powered by multiple power supplies and has multiple system protection and diagnostic functions to improve the stability of the device and CAN. In addition, SIT1043G has five working modes: normal mode, silent mode, standby mode, go-to-sleep mode and sleep mode. It supports local wake-up and remote wake-up in low power mode. The provided low power mode management can greatly save the power of CAN bus application system.

SIT1043G is compatible with the SIT1043 and other family products, which supports 1.8V MCU, and features improved bus signal symmetry and lower electromagnetic radiation performance.

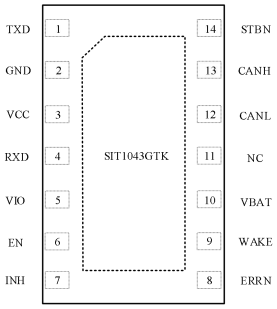
Applications: Automotive and Transport

- Body control
- Automotive Gateway
- ADAS
- Information and entertainment

PIN CONFIGURATION



SOP14



DFN4.5×3.0-14

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	TXD	Transmit data input.
2	GND	Ground.
3	VCC	5V bus power supply.
4	RXD	Receive data output.
5	VIO	I/O port power supply.
6	EN	Enable control input.
7	INH	Used to control the working state of the external voltage regulator, set to high after a wake-up event.
8	ERRN	Error indication output.
9	WAKE	Local wake-up input.
10	VBAT	Battery power supply.
11	NC	No connection.
12	CANL	Low-level CAN bus input and output.
13	CANH	High-level CAN bus input and output.
14	STBN	Standby mode control input

Note: The metal pad on the back of the DFN4.5*3.0-14 package is recommended to be grounded.

BLOCK DIAGRAM

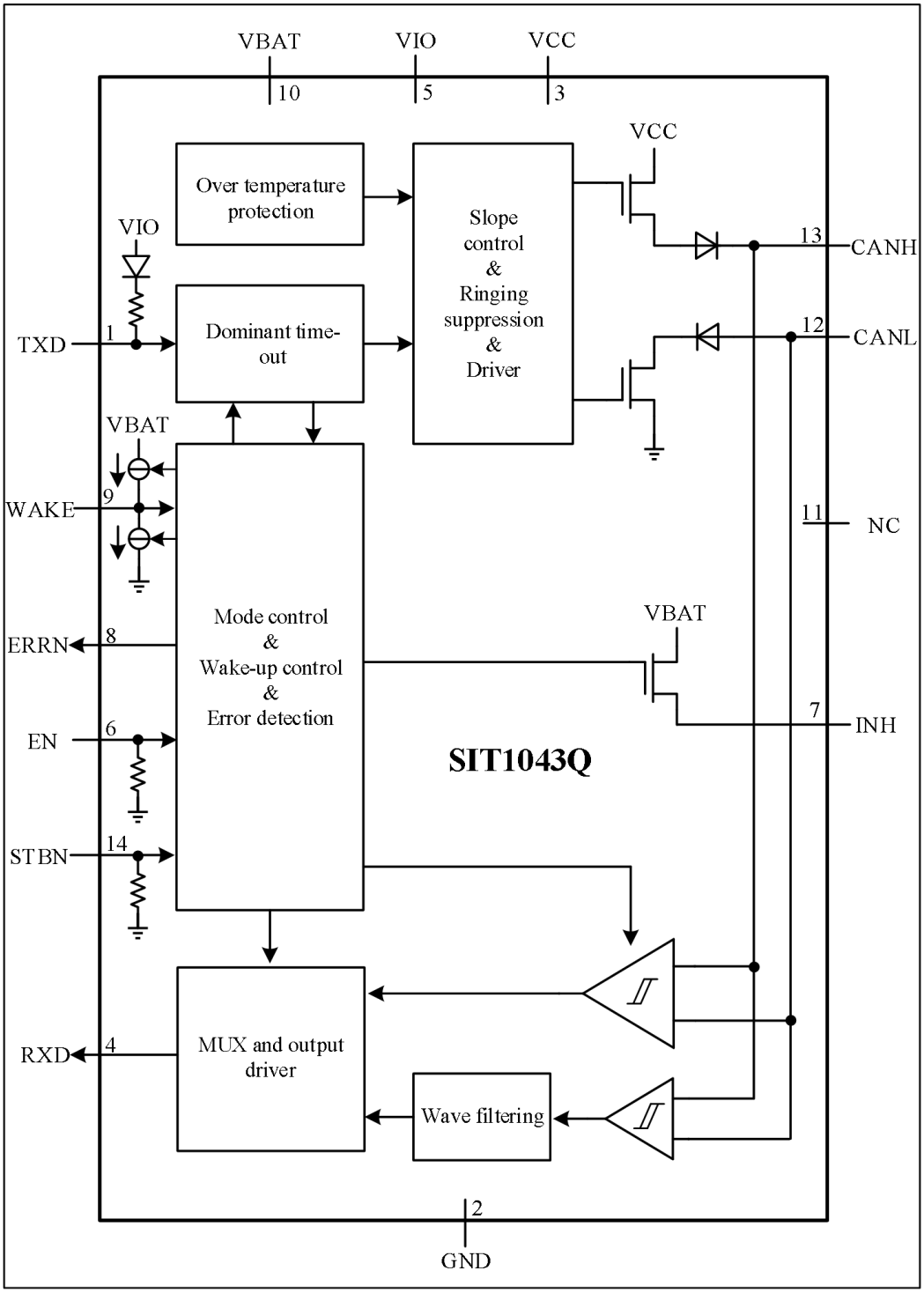


Fig 1 block diagram

RECOMMENDED WORK STATUS

PARAMETER	SYMBOL	VALUE	UNIT
VBAT supply voltage	VBAT	4.5~40	V
VCC supply voltage	VCC	4.5~5.5	V
VIO supply voltage	VIO	1.7~5.5	V
Logic output pin high level output current (RXD&ERRN)	$I_{OH(LOGIC)}$	>-2	mA
Logic output pin high level output current (RXD&ERRN)	$I_{OL(LOGIC)}$	<2	mA
INH output current	$I_{O(INH)}$	<1	mA
Ambient temperature	T_{amb}	-40~125	℃

LIMITING VALUES

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
Battery power supply	VBAT		-0.3~+58	V
Local wake-up port	WAKE		-18~VBAT+0.3	V
Inhibit output	INH		-0.3~VBAT+0.3	V
Bus power supply	VCC		-0.3~+7	V
MCU side port	TXD, RXD, EN, STBN, VIO, ERRN		-0.3~+7	V
Bus side input voltage	CANH, CANL		-58~+58	V
Bus differential breakdown voltage	$V_{(CANH-CANL)}$		-58~+58	V
Contact discharge model (IEC) (1)	VESD_IEC	pins CANH, CANL	±10	kV
		VBAT pin (with 10nF capacitor); WAKE pin (with 33kΩ resistor)	±8	kV
Human body model (HBM) (2)	VESD_HBM	all pins	±6	kV
		pins CANH and CANL to GND	±8	kV
Charged device model (CDM) (3)	VESD_CDM	all pins	±2000	V
Transient voltage (4)	V_{trt}	pulse 1	-100	V
		pulse 2a	75	V
		pulse 3a	-150	V
		pulse 3b	100	V
Storage temperature	T_{stg}		-55~150	℃
Virtual junction temperature	T_j		-40~150	℃

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

(1) According to IEC 61000-4-2;

(2) According to AEC-Q100-002;

(3) According to AEC-Q100-011;

(4) According to ISO7637-2: pins CANH,CANL,VBAT,WAKE to GND.

THERMAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	SOP14	91	°C/W
		DFN4.5×3.0-14	36	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	SOP14	42	°C/W
		DFN4.5×3.0-14	32	°C/W

MODE TRANSITIONS

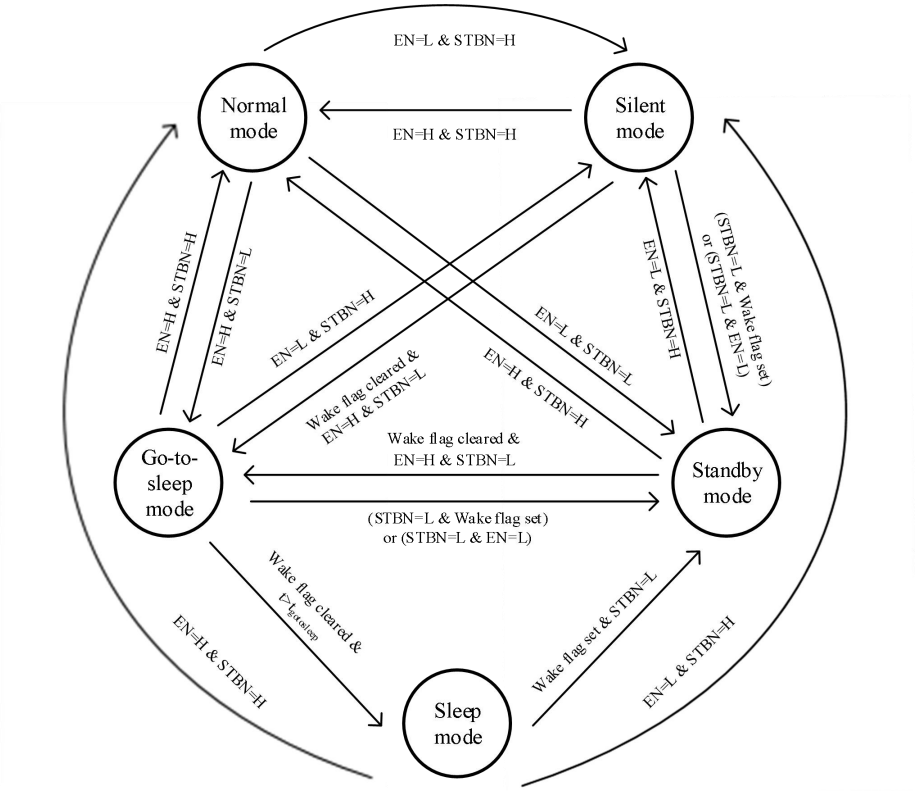


Fig 2 Mode transitions

Note: Valid VCC, VIO and VBAT voltages are present.

SYSTEM OPERATING MODES

Normal mode
The power supply is valid, both EN and STBN are set to high level, the device will enter the normal mode. In normal mode, the driver and high-speed receiver are enabled, the driver converts the digital input signal on the TXD to the bus analog level, while the receiver monitors the bus level and reacts it to the RXD. INH will be pulled high in normal mode.
Silent mode
The power supply is valid, setting EN to low level and STBN to high level, the device enters silent mode. The silent mode may also be referred to as a listen-only mode or a receive-only mode. In this mode, the driver is disabled, the high-speed receiver is enabled, the dominant and recessive signals of CANH and CANL are reflected to the RXD through the receiver. The bus will be biased to 0.5VCC, and INH will be pulled high.
Standby mode
The power supply is valid, and both EN and STBN are set to low level, and the device enters standby mode. Standby mode is a low-power mode in which the driver and high-speed receiver are disabled, INH is pulled high, and the device can still detect local wake-up and remote wake-up events.
Go-to-sleep mode
The power supply is valid, EN is set high, and STBN is set low. When $t<t_{go\text{-}to\text{-}sleep}$, the device will enter go-to-sleep mode. Go-to-sleep mode is a transition mode that jumps to sleep mode. The working state of the device is consistent with the standby mode, the driver and high-speed receiver are disabled, and INH is pulled high. When the time in this mode exceeds $t_{go\text{-}to\text{-}sleep}$, it switches to sleep mode, and INH will go to a high-impedance state.
Sleep mode
The power supply is valid, EN is set high, STBN is set low, when $t>t_{go\text{-}to\text{-}sleep}$ can enter sleep mode. Sleep mode is a working mode with the lowest power consumption. In sleep mode, the driver and high-speed receiver are disabled, and the output port INH is in a high-impedance state, which can instruct to turn off the external voltage regulator, and the VCC power supply of the transceiver and MCU will not be available. In this state, SIT1043G maintains power supply through the battery pin VBAT, so as to ensure the monitoring work of local wake-up and remote wake-up. In addition, when the power supply VCC or VIO is under-voltage and the under-voltage duration is longer than t_{DETUVD} (or floating), the device will also enter sleep mode, INH is in a high-impedance state, and a local wake-up or remote wake-up event can cause INH to be pulled high.

FUNCTION MODE TABLE

VCC	VIO	VBAT	EN	STBN	Wake flag	Mode	Driver	High-speed Receiver	Low-power Receiver	RXD	BUS State	INH
normal	normal	normal	**H**	**H**	X	normal	enable	enable	disable	Follow the bus	VCC/2	H
normal	normal	normal	**L**	**H**	X	silent	disable	enable	disable	Follow the bus	VCC/2	H
normal	normal	normal	**H**	**L**	**Clear**	Go-to-sleep	disable	disable	enable	H	GND	H
normal	normal	normal	**H**	**L**	**Clear**	sleep	disable	disable	enable	H	GND	Z
normal	normal	normal	**H**	**L**	**Set up**	standby	disable	disable	enable	L	GND	H
normal	normal	normal	**L**	**L**	**Clear**	standby	disable	disable	enable	H	GND	H
normal	normal	normal	**L**	**L**	**Set up**	standby	disable	disable	enable	L	GND	H
UV	normal	normal	X	X	X	sleep	disable	disable	enable	H	GND	Z
normal	**UV**	normal	X	X	X	sleep	disable	disable	enable	Z	GND	Z
normal	normal	**UV**	X	X	X	standby	disable	disable	disable	Z	Z	Z

Note: H=high level; L=low level; Z=high ohmic; X=irrelevant.

DRIVE STATUS TABLE

MODE	TXD INPUT	BUS OUTPUT		BUS STATE
		CANH	CANL	
Normal mode	L	H	L	Dominant
	H or Open	Z	Z	Bus biased to VCC/2
Silent mode	X	Z	Z	Bus biased to VCC/2
Standby mode	X	Z	Z	Bus biased to GND
Go-to-sleep mode	X	Z	Z	Bus biased to GND
Sleep mode	X	Z	Z	Bus biased to GND

Note: H=high level; L=low level; Z=high ohmic; X=irrelevant.

RECEIVER FUNCTION TABLE

Mode	BUS DIFFERENTIAL INPUT V_{OD}=CANH-CANL	BUS STATE	RXD OUT
Normal mode and Silent mode	$V_{OD}\geq 0.9V$	Dominant	L
	$0.9V>V_{OD}>0.5V$	?	X
	$V_{OD}\leq 0.5V$	Recessive	H
Standby mode, Go-to-sleep mode and Sleep mode	$V_{OD}\geq 1.1V$	Dominant	H, L when the wake-up flag set
	$1.1V>V_{OD}>0.4V$	?	
	$V_{OD}\leq 0.4V$	Recessive	

Note: H=high level; L=low level; ?=uncertain; Valid VCC, VIO and VBAT voltages are present.

INTERNAL FLAG SIGNAL

FLAG SIGNAL	REASON FOR APPEARING	EXTERNAL INDICATION	FLAG SIGNAL CLEAR	NOTE
Power-on flag	VBAT power-on	Enter silent mode (from standby mode, Go-to-sleep mode, sleep mode) ERRN=L	Enter normal mode	
Wake-up request flag	Remote wake-up, local wake-up, initial power-on	Enter standby mode, Go-to-sleep mode, sleep mode ERRN=RXD=L	Enter normal mode, VCC or VIO undervoltage	
Wake-up source flag (1)	Remote wake-up, local wake-up, initial power-on	Enter normal mode: ERRN=L indicates local wake-up, ERRN=H indicates remote wake-up	TXD transitions (2) in normal mode, leaving normal operating mode, VCC or VIO undervoltage	The establishment of the power-up flag sets the wake-up source flag
UVD_{NOM} undervoltage flag	VCC undervoltage	No external indication	VCC recovers, the wake-up request flag appears	
	VIO undervoltage	No external indication	VIO recovers, the wake-up request flag appears	
UVD_{VBAT} undervoltage flag	VBAT undervoltage	No external indication	VBAT recovers	
Local error flag	TXD dominant timeout	When entering silent mode from normal mode ERRN=L	RXD=L&TXD=H; enter normal mode	Once a TXD dominant timeout occurs, the drive will be disabled
	TXD shorted to RXD			A short circuit of TXD to RXD occurs, the driver will be disabled
	Bus dominant timeout		RXD= H; enter normal mode	A bus timeout occurred and the drive is still enabled
	Over temperature protection		The junction temperature returns to normal and RXD=L&TXD=H; the junction temperature returns to normal and jumps back to normal operation mode	In the event of an overtemperature condition, the driver will be disabled

(1) The wake-up source flag will only identify the first wake-up request signal;

(2) There are 4 dominant-recessive transitions of TXD, and each dominant-recessive period of this transition is at least 4μs;

The device carries out system diagnosis through the above series of flag signals and indicates the cause of the failure. The MCU can judge the internal working state of the system or the cause of the fault through some mode switching and the indication of the transceiver chip ERRN and RXD pins.

Power-on flag

The power-on flag refers specifically to the power-on event of the battery power supply VBAT. The power-on flag is set when VBAT returns to normal operating voltage from a voltage lower than $V_{UVDVBAT}$. Once the device enters silent mode from standby or sleep mode, ERRN is pulled low to indicate that the power-on flag is set. When entering normal operating mode, the power-on flag will be cleared. The power-on flag clears the UVD_{NOM} undervoltage flag and sets the wake-up request flag and wake-up source flag.

Wake-up request flag

SIT1043G can realize low-power wake-up function in two ways: local wake-up and remote wake-up.

Local wake-up

SIT1043G realizes the function of local wake-up through the WAKE port. In standby mode or sleep mode, as long as there is a valid rising or falling edge on the WAKE pin, it will be detected as a local wake-up event.

A valid rising edge means that the voltage of the WAKE port jumps from a voltage lower than $V_{th(WAKE)}$ to a voltage higher than $V_{th(WAKE)}$, and the duration of this jump is longer than $t_{wake(local)}$, which can be considered as a valid rising edge, as shown in **Fig 3**; a valid falling edge is when the voltage at the WAKE port transitions from a voltage above $V_{th(WAKE)}$ to a voltage below $V_{th(WAKE)}$, and the duration of this transition is greater than $t_{wake(local)}$, which can be considered as a valid falling edge, as shown in **Fig 4**. Any transitions of duration less than $t_{wake(local)}$ and transitions that do not cross the threshold voltage $V_{th(WAKE)}$ will be filtered out.

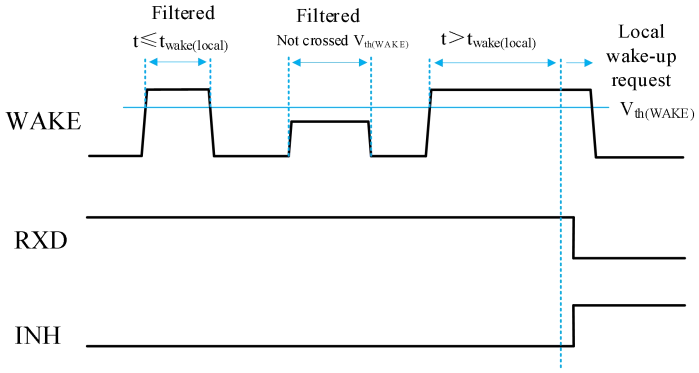


Fig 3 Local wake-up for WAKE rising edge

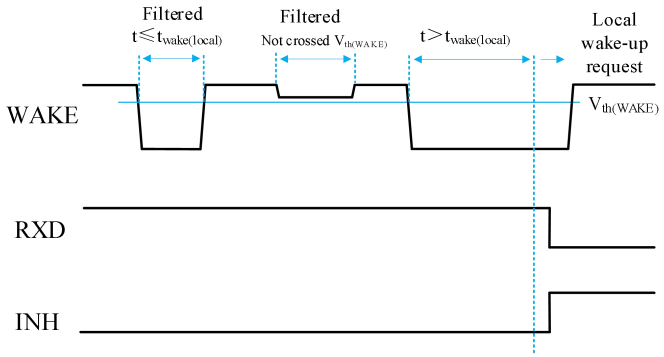


Fig 4 Local wake-up for WAKE falling edge

Remote wake-up

The SIT1043G implements a remote wake-up function through a low-power receiver to inform the MCU that the bus has been activated and the node should resume normal operation. In sleep mode, when a valid

remote wake-up pattern (WUP) appears, the device will wake up and jump to standby mode, RXD will be pulled low and INH will be pulled high.

According to ISO11898-2, the complete WUP consists of: a filtered dominant level (duration greater than $t_{wake(dom)}$), a filtered recessive level (duration greater than $t_{wake(rec)}$) and another filtered dominant level flat (duration greater than $t_{wake(dom)}$). This dominant-recessive-dominant level signal must appear within $t_{wake(timeout)}$ time, otherwise the internal wake-up logic will be reset and restart the monitoring of the bus.

The RXD pin will remain high until the wake-up event is triggered. The above mentioned dominant and recessive levels will be ignored (filtered out) if the duration is lower than $t_{wake(busdom)}$ and $t_{wake(busrec)}$. A wake-up event will not be responded when any of the following events occurs while a valid wakeup pattern is received:

(1) The device switches to the normal working mode;

(2) The complete wake-up request frame is not received within the $t_{wake(timeout)}$;

(3) VCC or VIO undervoltage is detected (UVD_{NOM} flag signal is set).

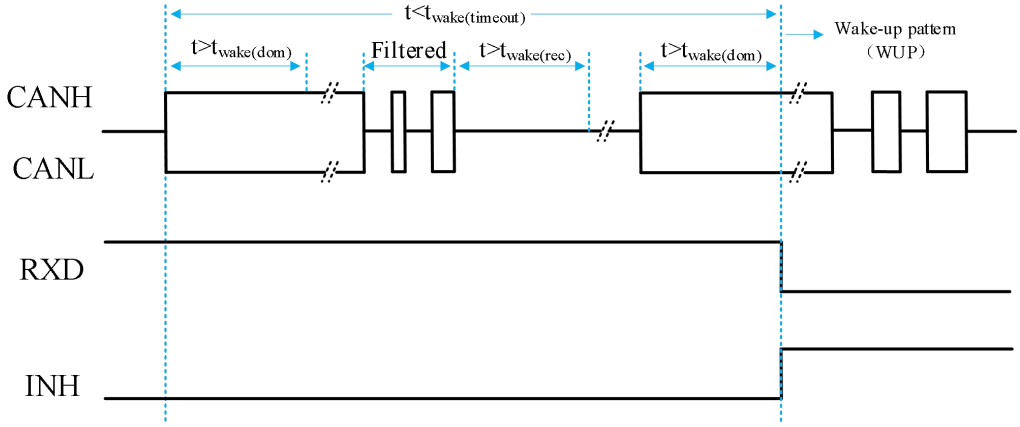


Fig 5 Remote wake-up diagram

Wake-up source flag

SIT1043G can identify the wake-up source through the wake-up source flag, and the wake-up source flag can be represented by the level of the ERRN pin when the chip enters the normal mode. If the wake-up flag is generated by the local wake-up request given by the WAKE pin, the ERRN pin is low level after jumping to the normal operating mode. Conversely, if the ERRN pin is high, it can indicate the remote wake-up signal given by the CAN bus. The chip leaving the normal operating mode also clears the wake-up source flag. This flag is also generated on initial power-on.

UVD_{NOM} undervoltage flag

The SIT1043G has an undervoltage detection function on the power supply VCC and VIO, which can set the UVD_{NOM} undervoltage flag and place the device in a protected state. When VCC is lower than its undervoltage threshold V_{UVDVCC} and the undervoltage time is longer than t_{DETUVD} or VIO is lower than its undervoltage threshold V_{UVDVIO} and the undervoltage time is longer than t_{DETUVD}, by setting the UVD_{NOM} undervoltage flag, the device will be forced to enter sleep mode and wake up locally and with remote wake-up are still normal. INH is high impedance and further instructs the external regulator to shut down, which saves unnecessary power consumption and avoids the bus from being disturbed. The UVD_{NOM} undervoltage flag is cleared when VCC is higher than V_{UVDVCC} and the recovery time is longer than t_{RECUVD}

or VIO is higher than V_{UVDVIO} and the recovery time is longer than t_{DETUVD}. At the same time, the establishment of the wake-up request flag and the power-up flag and the low-to-high transition of STBN will clear the UVD_{NOM} undervoltage flag.

UVD_{VBAT} undervoltage flag

The battery power VBAT of the SIT1043G also has an undervoltage detection function. When VBAT is lower than $V_{UVDVBAT}$, the $UVDV_{BAT}$ undervoltage flag is set, and the transceiver will be disconnected from the bus (zero load). When the voltage at pin VBAT is restored, the $UVDV_{BAT}$ undervoltage flag is cleared and the transceiver will switch to the operating mode indicated by the logic levels on the STBN and EN pins.

Local error flag

SIT1043G can detect four kinds of local error events: TXD dominant timeout, TXD and RXD short circuit, bus dominant timeout, over temperature protection. Whenever any of these events occur, a local error flag is generated, and when the device transitions from normal mode to silent mode, ERRN is pulled low, indicating that a local error flag has been set.

TXD dominant timeout

In normal mode, if a low level voltage on pin TXD lasts longer than the internal timer value $t_{dom(TXD)}$, the transmitter will be disabled, driving the bus into a recessive state. This prevents the bus line from being driven to a permanent dominant state (blocking all network traffic) due to a hardware or software application failure on pin TXD being forced permanently low.

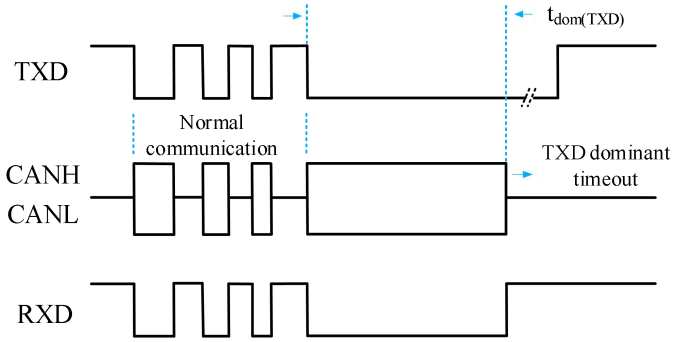


Fig 6 TXD dominant timeout diagram

TXD and RXD short circuit

SIT1043G has the protection function of short circuit between TXD and RXD, which can avoid the periodic deadlock situation of the local device. In normal mode or silent mode, if a short circuit occurs between the TXD and RXD of the device, and the duration of the short circuit exceeds $t_{dom(TXD)}$, the device will consider that a short circuit between TXD and RXD has occurred, the local error flag is established, and the driver will be disabled.

Bus dominant timeout

When the bus is short-circuited, if the bus has a dominant level whose duration is longer than the internal timer value $t_{dom(BUS)}$, it will be regarded as a bus dominant timeout event and a local error flag will be established.

Over temperature protection

SIT1043G has an over temperature protection function. If the junction temperature of the device exceeds the

over temperature shutdown temperature $T_{j(sd)}$, the bus driver circuit will be shut down, thereby blocking the transmission path from TXD to the bus, so during thermal shutdown the level is biased in a recessive state while the rest of the chip remains functional. Because the driver tube is the main energy consuming component, turning off the driver tube can reduce the power consumption and thus reduce the chip temperature.

DC PARAMETERS

Tested under recommended operating conditions: VBAT=4.5V to 40V, VCC=4.5V to 5.5V, VIO=1.7V to 5.5V, T_j=-40°C to 150°C. Unless otherwise stated, all typical values are measured at T_{amb}=25°C, supply voltage VBAT=12V, VCC =5V, VIO=5V, R_L=60Ω.

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Power supply characteristics						
VBAT supply current	I_{BAT}	Normal or Silent mode		45	100	μA
		Standby mode, INH= VBAT, WAKE=0V		18	32	μA
		Sleep mode, WAKE=0V, T_j=-40°C to 125°C		16	30	μA
VCC supply current	I_{CC}	Normal mode: dominant		42	65	mA
		Normal mode: recessive; Silent mode		5	9	mA
		Standby or Sleep mode		1	4	μA
		Normal mode; dominant bus short circuit, -3V<(CANH=CANL)<+18V			109	mA
VIO supply current	I_{IO}	Normal mode; dominant, TXD=0V		100	250	μA
		Normal recessive or Silent mode, TXD=VIO		1	4	μA
		Standby or Sleep mode		1	4	μA
VBAT undervoltage detection	$V_{UVDVBAT}$		3.5		4.3	V
VCC undervoltage detection	V_{UVDVCC}	VBAT>4.5V	3.5		4.3	V
VIO undervoltage detection	V_{UVDVIO}	VBAT>4.5V	1.4		1.65	V
TXD Pin Characteristics						
HIGH-level input current	$I_{IH(TXD)}$	TXD=VIO	-1	0	1	μA
LOW-level input current	$I_{IL(TXD)}$	TXD=0V	-150		-20	μA
Pull-up resistor	R_{pu}		20		80	kΩ
Leakage current when TXD is unpowered	$I_{off(TXD)}$	VIO=0V, TXD=5.5V	-1		1	μA
HIGH-level input voltage	V_{IH}		0.7VIO		VIO+0.3	V

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
LOW-level input voltage	V_{IL}		-0.3		0.3VIO	V
RXD Pin Characteristics						
RXD HIGH-level output current	$I_{OH(RXD)}$	RXD=VIO-0.4V	-10	-5	-1	mA
RXD LOW-level output current	$I_{OL(RXD)}$	RXD=0.4V, bus dominant	1	5	10	mA
STBN Pin Characteristics						
STBN HIGH-level input current	$I_{IH(STBN)}$	STBN=VIO	20		150	μA
STBN LOW-level input current	$I_{IL(STBN)}$	STBN=0V	-1		1	μA
Pull-down resistor	R_{pd}		20		80	kΩ
Leakage current when STBN is unpowered	$I_{off(STBN)}$	VIO=0V, STBN=5.5V	-1		1	μA
HIGH-level input voltage	V_{IH}		0.7VIO		VIO+0.3	V
LOW-level input voltage	V_{IL}		-0.3		0.3VIO	V
EN Pin Characteristics						
EN HIGH-level input current	$I_{IH(EN)}$	EN=VIO	20		150	μA
EN LOW-level input current	$I_{IL(EN)}$	EN=0V	-1		1	μA
Pull-down resistor	R_{pd}		20		80	kΩ
Leakage current when EN is unpowered	$I_{off(EN)}$	VIO=0V, EN=5.5V	-1		1	μA
HIGH-level input voltage	V_{IH}		0.7VIO		VIO+0.3	V
LOW-level input voltage	V_{IL}		-0.3		0.3VIO	V
ERRN Pin Characteristics						
ERRN HIGH-level output current	$I_{OH(ERRN)}$	ERRN=VIO-0.4V	-50	-20	-4	μA
ERRN LOW-level input current	$I_{OL(ERRN)}$	ERRN=0.4V	0.1	0.5	2	mA
INH Pin Characteristics						
INH HIGH-level voltage drop	$\triangle V_H$	I_{INH}=-1mA	0		1	V
		I_{INH}=-2mA	0		2	V
INH leakage current	I_L	Sleep mode	-2	0	2	μA
Short circuit output	$I_{O(sc)}$	V_{INH}=0V	-15			mA

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
current						
WAKE Pin Characteristics						
WAKE HIGH-level input current	$I_{IH(WAKE)}$	WAKE＞2.6V	-8	-4		μA
WAKE LOW-level input current	$I_{IL(WAKE)}$	WAKE＜1.8V		4	8	μA
WAKE threshold voltage	$V_{th(WAKE)}$	STBN=0	1.8		2.6	V
Temperature detection						
shutdown junction temperature (1)	$T_{j(sd)}$			190		℃
Bus Driver DC Characteristics						
CANH dominant output voltage	$V_{OH(D)}$	Normal mode, TXD=0V, R_L=50Ω to 65Ω	2.75	3.5	4.5	V
CANL dominant output voltage	$V_{OL(D)}$		0.5	1.5	2.25	V
Bus dominant differential output voltage	$V_{OD(D)}$	Normal mode, TXD=0V, R_L=50Ω to 65Ω	1.5		3	V
		Normal mode, TXD=0V, R_L=45Ω to 70Ω	1.4		3.3	V
		Normal mode, TXD=0V, R_L=2240Ω	1.5		5	V
Bus recessive output voltage	$V_{O(R)}$	Normal or Silent mode, TXD=VIO, no load	2	0.5VCC	3	V
		Normal or Silent mode, TXD=VIO, R_L=60Ω	2.2	0.5VCC	2.8	V
Bus recessive differential output voltage	$V_{OD(R)}$	Normal or Silent mode, TXD=VIO, no load	-50		50	mV
		Normal or Silent mode, TXD=VIO, R_L=60Ω	-50		50	mV
Bus output voltage (bus biased to ground)	$V_{O(S)}$	Standby or Sleep mode, no load	-0.1		0.1	V
Bus differential output voltage (bus biased to ground)	$V_{OD(S)}$	Standby or Sleep mode, no load	-0.2		0.2	V
Transmitter dominant voltage symmetry	$V_{dom(TX)sym}$	$V_{dom(TX)sym}$=VCC- CANH - CANL	-400		400	mV
Transmitter voltage symmetry (1)	V_{TXsym}	V_{TXsym}= CANH + CANL, R_L=60Ω, C_{SPLIT}=4.7nF, f_{TXD}=250kHz, 1MHz or	0.9V_{CC}		1.1V_{CC}	V

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
		2.5MHz **Fig 11**				
Common mode voltage step (1)	$V_{cm(step)}$	**Fig 9**, **Fig 11**	-150		150	mV
Peak-to-peak common mode voltage (1)	$V_{cm(p-p)}$	**Fig 9**, **Fig 11**	-300		300	mV
dominant short-circuit output current	$I_{O(SC)DOM}$	Normal mode, TXD=0V, CANH=-15V to 40V	-100			mA
		Normal mode, TXD=0V, CANL=-15V to 40V			100	mA
recessive short-circuit output current	$I_{O(SC)REC}$	Normal mode, TXD=VIO, CANH=CANL=-27V to 32V	-3		3	mA
Bus Receiver DC Characteristics						
receiver threshold voltage	$V_{th(RX)dif}$	Normal or Silent mode, -30V<V_{CM}<30V	0.5		0.9	V
		Standby or Sleep mode, -12V<V_{CM}<12V	0.4		1.1	V
differential receiver hysteresis voltage	$V_{hys(RX)dif}$	Normal or Silent mode, -30V<V_{CM}<30V		80		mV
receiver recessive voltage	$V_{rec(RX)}$	Normal or Silent mode, -30V<V_{CM}<30V	-3		0.5	V
		Standby or Sleep mode, -12V<V_{CM}< 12V	-3		0.4	V
receiver dominant voltage	$V_{dom(RX)}$	Normal or Silent mode, -30V<V_{CM}<30V	0.9		8	V
		Standby or Sleep mode, -12V<V_{CM}<12V	1.1		8	V
leakage current	I_L	VCC=VIO=VBAT=0V, CANH=CANL=5V	-10		10	μA
CANH and CANL input resistance	R_{IN}	-2V≤CANH≤7V -2V≤CANL≤7V	25	40	50	kΩ
CANH, CANL differential input resistance	R_{ID}	-2V≤CANH≤7V -2V≤CANL≤7V	50	80	100	kΩ
CANH, CANL input resistance deviation	$\triangle R_{IN}$	0V≤CANH≤5V 0V≤CANL≤5V	-3		3	%
CANH and CANL input capacitance to ground (1)	C_{IN}	TXD=VIO			40	pF
CANH, CANL differential input	C_{ID}	TXD=VIO			20	pF

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
capacitance (1)						

AC PARAMETER

Unless otherwise stated, all typical values are measured at T_{amb}=25°C, supply voltage VBAT=12V, VCC =5V, VIO=5V, R_L=60Ω, C_{BUS}=100pF, C_{RXD}=15pF.

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Driver AC Characteristics						
delay time from TXD to bus dominant	$t_{d(TXD-busdom)}$	Normal mode, **Fig 7**, **Fig 10**			80	ns
delay time from TXD to bus recessive	$t_{d(TXD-busrec)}$	Normal mode, **Fig 7**, **Fig 10**			80	ns
Differential output signal rise time	$t_{r(BUS)}$	Normal mode, **Fig 7**, **Fig 10**		35		ns
Differential output signal fall time	$t_{f(BUS)}$	Normal mode, **Fig 7**, **Fig 10**		35		ns
TXD dominant time-out	$t_{dom(TXD)}$	TXD=0, **Fig 6**	0.3	0.6	1.2	ms
Receiver AC Characteristics						
delay time from bus dominant to RXD	$t_{d(busdom-RXD)}$	Normal or Silent mode, **Fig 7**, **Fig 10**			110	ns
delay time from bus recessive to RXD	$t_{d(busrec-RXD)}$	Normal or Silent mode, **Fig 7**, **Fig 10**			110	ns
RXD signal rise time	$t_{r(RXD)}$	Normal or Silent mode, **Fig 7**, **Fig 10**		8		ns
RXD signal fall time	$t_{f(RXD)}$	Normal or Silent mode, **Fig 7**, **Fig 10**		8		ns
bus dominant time-out time	$t_{dom(BUS)}$	V_{OD}>0.9V	0.3	0.6	1.2	ms
TXD to RXD loop delay						
delay time from TXD LOW to RXD LOW	t_{loop1}	Normal mode, **Fig 7**, **Fig 10**	40		190	ns
delay time from TXD HIGH to RXD HIGH	t_{loop2}	Normal mode, **Fig 7**, **Fig 10**	40		190	ns
CAN FD Bit time						
Bit time of BUS output pin	$t_{bit(BUS)}$	$t_{bit(TXD)}$=500ns, **Fig 8**	455		510	ns
		$t_{bit(TXD)}$=200ns, **Fig 8**	155		210	ns
Bit time of RXD output pin	$t_{bit(RXD)}$	$t_{bit(TXD)}$=500ns, **Fig 8**	420		520	ns
		$t_{bit(TXD)}$=200ns, **Fig 8**	120		220	ns
BUS output bit width deviation	$\Delta t_{bit(BUS)}$	$\Delta t_{bit(BUS)}=t_{bit(BUS)}-t_{bit(TXD)}$	-45		10	ns

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
RXD output bit width deviation	$\Delta t_{bit(RXD)}$	$\Delta t_{bit(RXD)}=t_{bit(RXD)}-t_{bit(TXD)}$	-80		20	ns
BUS and RXD output bit time difference	Δt_{rec}	$\Delta t_{rec}=t_{bit(RXD)}-t_{bit(BUS)}$	-45		15	ns
Device Switching Characteristics						
hold time	$t_{go\_to\_sleep}$	EN=VIO, STBN=0	20		60	μs
bus dominant wake-up time	$t_{wake(dom)}$	Standby or Sleep mode	0.5		1.8	μs
bus recessive wake-up time	$t_{wake(rec)}$	Standby or Sleep mode	0.5		1.8	μs
bus wake-up time-out time (1)	$t_{wake(timeout)}$		0.5		2	ms
local wake-up time	$t_{wake(local)}$	Standby or Sleep mode	5		50	μs
undervoltage detection time (1)	t_{DETUVD}		100		350	ms
undervoltage recovery time (1)	t_{RECUVD}		1		5	ms
STBN and EN pin filter time (1)	t_{filter_IO}		1		10	μs

(1) Guaranteed by design, not tested by production.

TIMING WAVEFORM

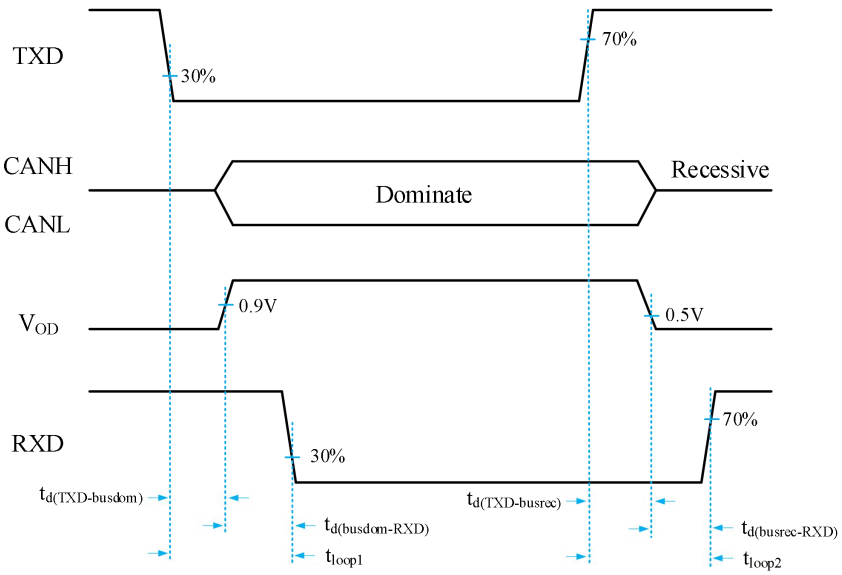


Fig 7 CAN transceiver timing diagram

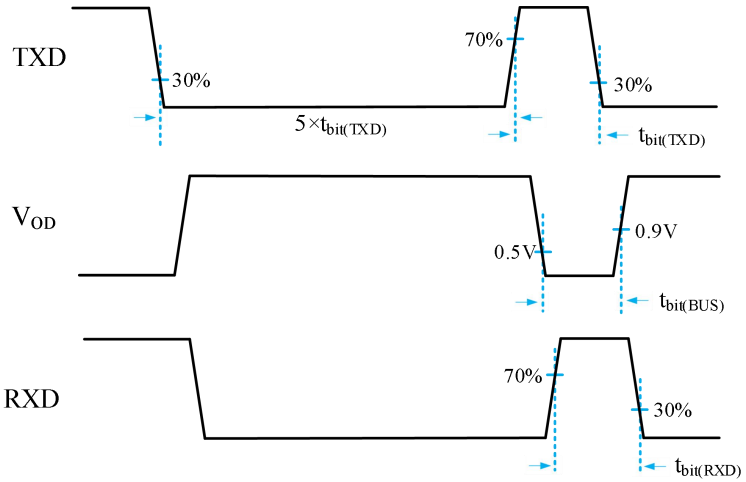


Fig 8 t_{bit} timing diagram

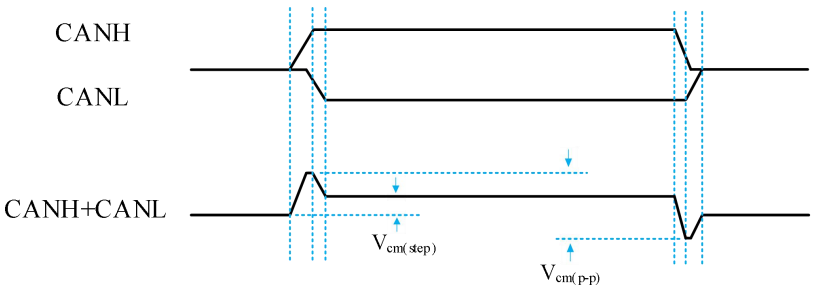


Fig 9 CAN bus common-mode voltage (according to SAE 1939-14)

TRANSCEIVER TEST CIRCUIT

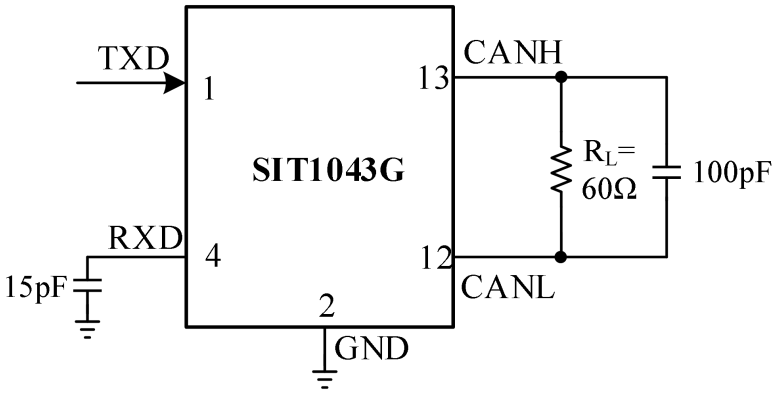


Fig 10 Transceiver timing sequence test circuit

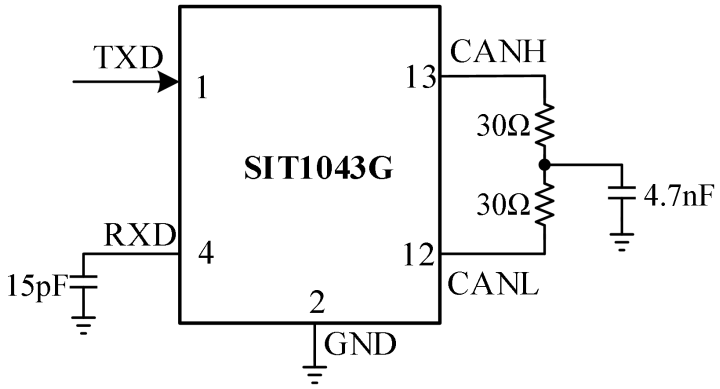


Fig 11 Transceiver bus symmetry test circuit

TYPICAL APPLICATION CIRCUIT

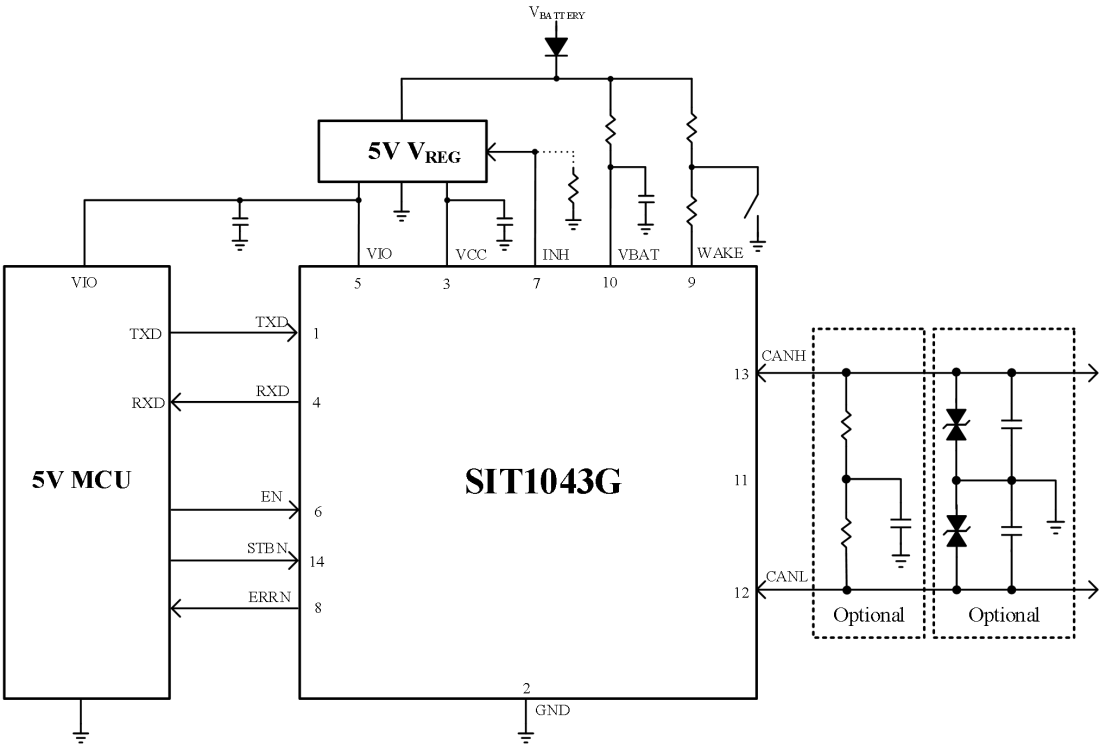


Fig 12 Typical application with 5V MCU

Note:

1. The pull-down resistor (10kΩ~100kΩ) from INH to GND should be added and its value selected based on the status of the EN pin of the external power supply chip.
2. PIN8 (ERRN) outputs a reference to VIO. This pin should be connected to the MCU. The MCU can judge the internal operating status or the cause of a fault by switching modes and monitoring the indications between the transceiver chip's ERRN and RXD pins, thereby further controlling the transceiver chip.

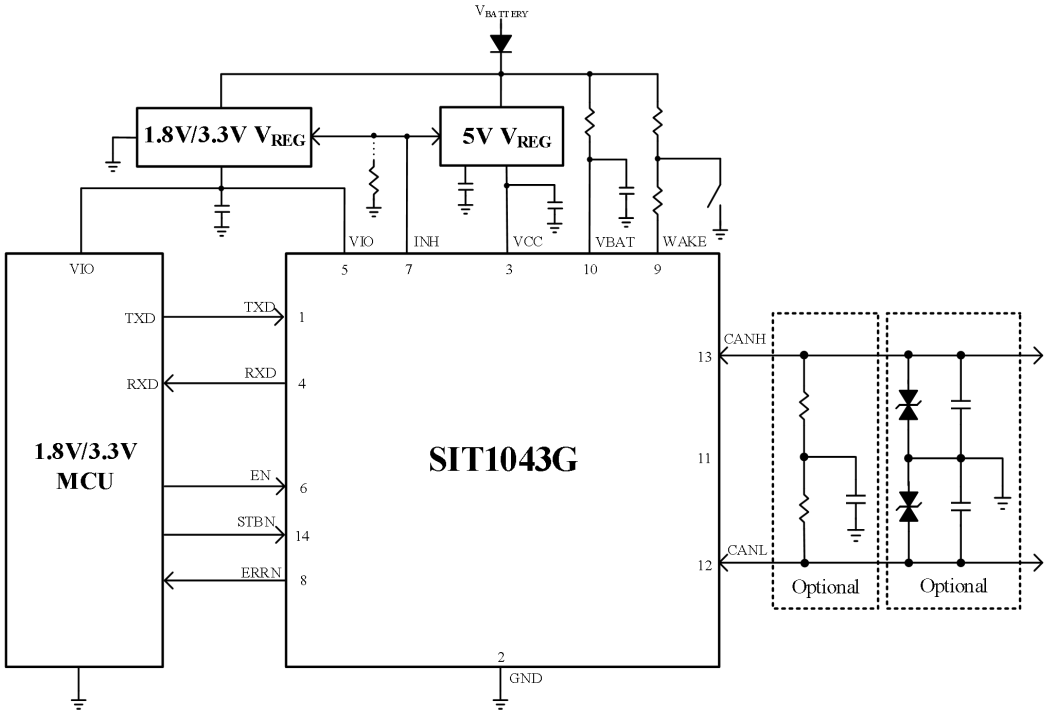


Fig 13 Typical application with 1.8V/3.3V MCU

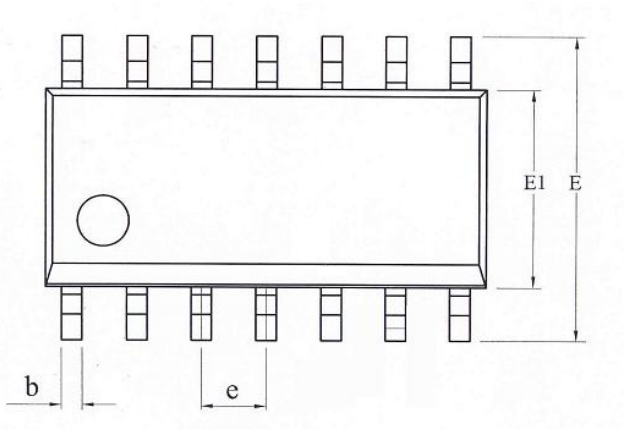
Note:

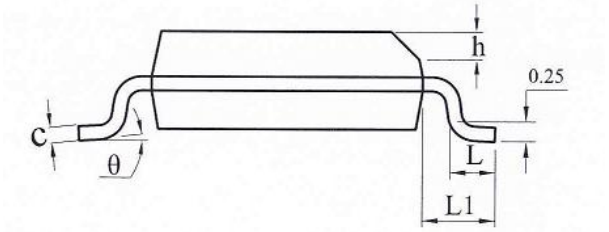
1. The pull-down resistor (10kΩ~100kΩ) from INH to GND should be added and its value selected based on the status of the EN pin of the external power supply chip.
2. PIN8 (ERRN) outputs a reference to VIO. This pin should be connected to the MCU. The MCU can judge the internal operating status or the cause of a fault by switching modes and monitoring the indications between the transceiver chip's ERRN and RXD pins, thereby further controlling the transceiver chip.

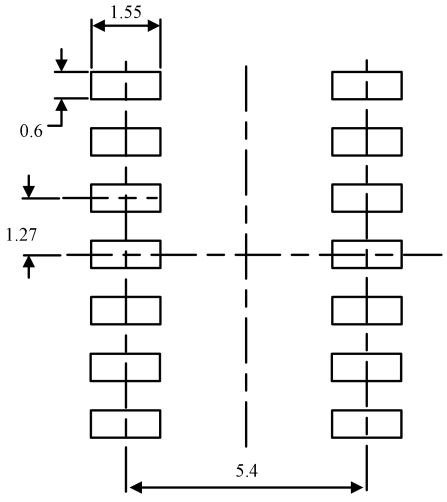
SOP14 DIMENSIONS

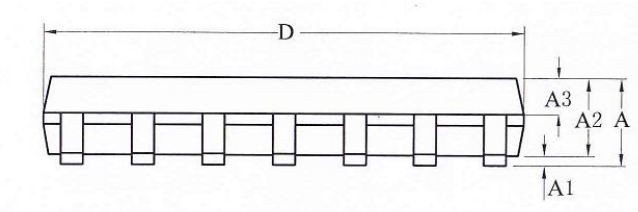
PACKAGE SIZE

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.05	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°







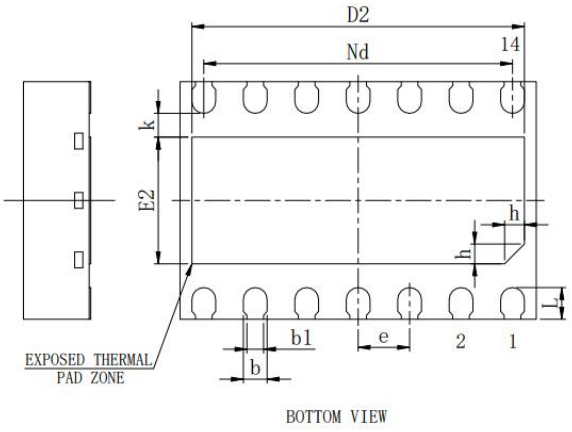


LAND PATTERN EXAMPLE (Unit: mm)

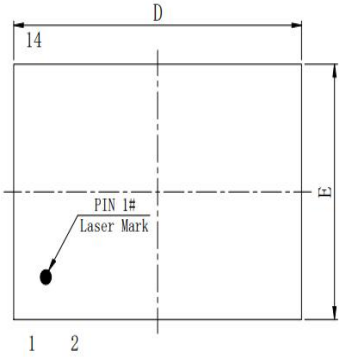
DFN4.5×3.0-14 DIMENSIONS

PACKAGE SIZE

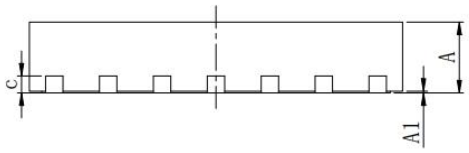
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.25	0.30	0.35
b1		0.21REF	
c		0.203REF	
D	4.40	4.50	4.60
D2	4.10	4.20	4.30
e		0.65BSC	
Nd		3.90BSC	
E	2.90	3.00	3.10
E2	1.50	1.60	1.70
L	0.35	0.40	0.45
h	0.20	0.25	0.30
K		0.30REF	



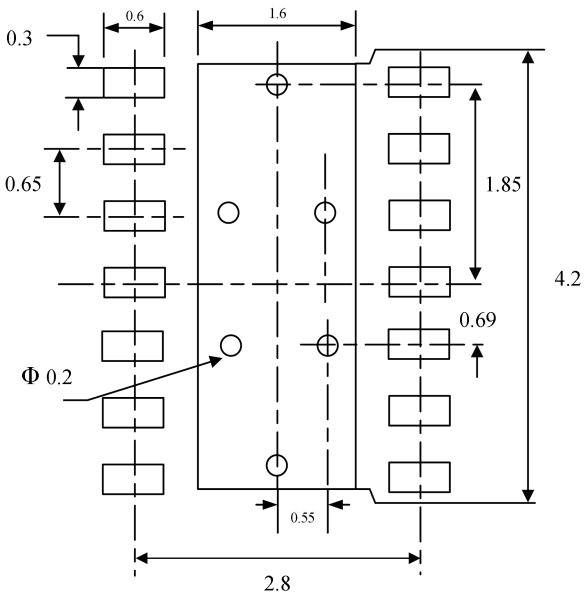
BOTTOM VIEW



TOP VIEW

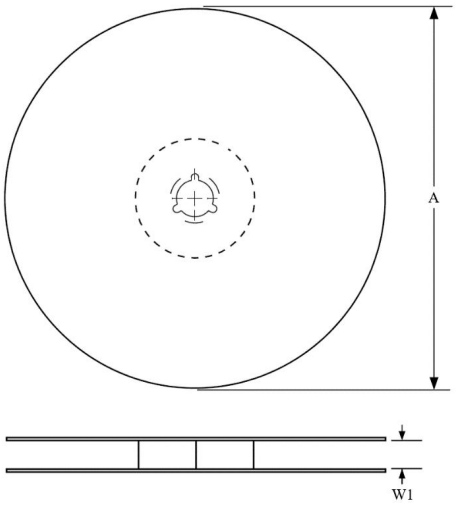


SIDE VIEW

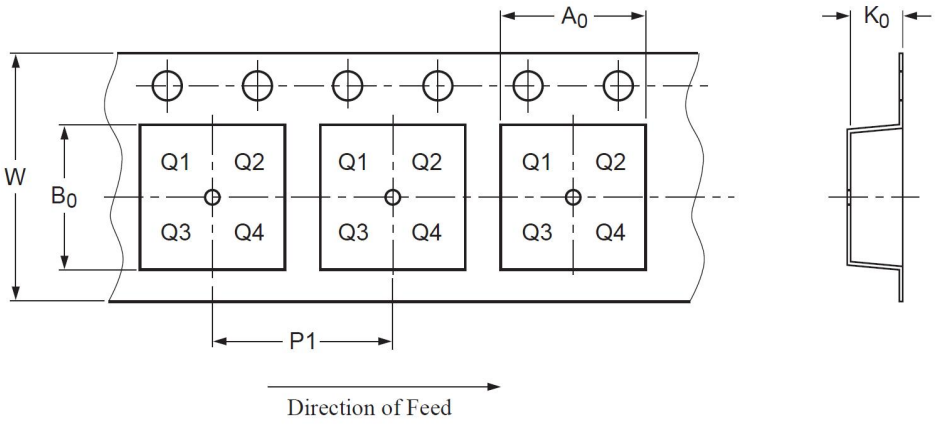


LAND PATTERN EXAMPLE (Unit: mm)

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



PIN1 is in quadrant 1

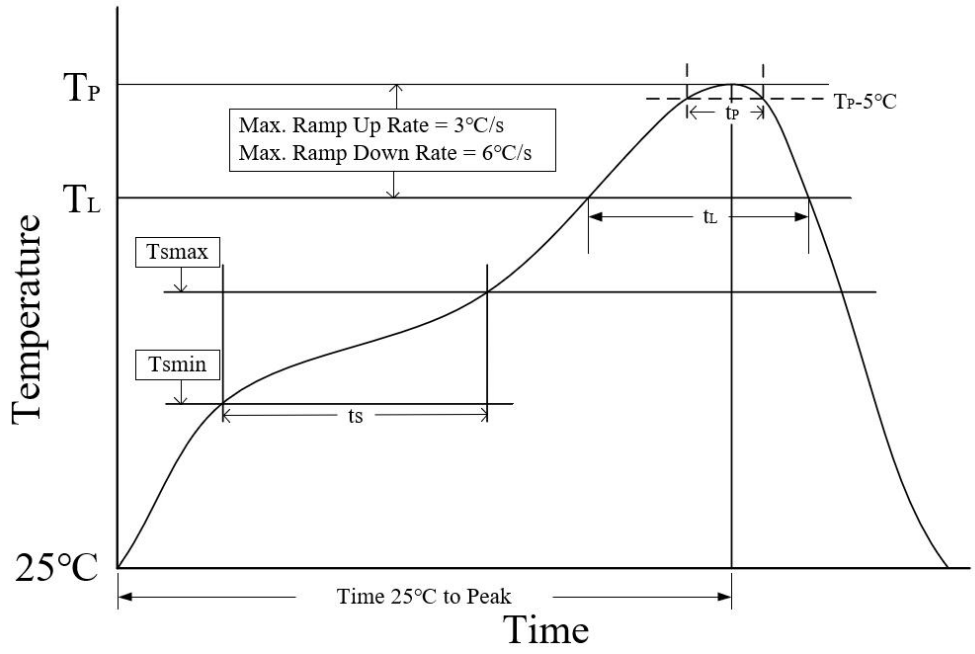
Package Type	Reel Diameter A (mm)	Tape Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
SOP14	330±1	12.4	$6.50^{+0.20}_{-0.1}$	$9.30^{+0.20}_{-0.1}$	2.0±0.10	8.00±0.1	16.00±0.10
DFN4.5×3.0-14	329±1	12.4	3.75±0.1	4.25±0.1	1.00±0.1	8.00±0.1	12.00±0.3

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	MSL	PACKING
SIT1043GT	SOP14	MSL 3	Tape and reel
SIT1043GTK	DFN4.5×3.0-14	MSL 3	Tape and reel

SOP14 is packed with 2500 pieces/disc in braided packaging; Leadless DFN4.5×3.0-14 is packed with 3000 pieces/disc in braided packaging.

REFLOW SOLDERING



Parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	3 °C/second max
Preheat time ts (T_{smin}=150 °C to T_{smax}=200 °C)	60-120 seconds
Melting time t_L (T_L=217 °C)	60-150 seconds
Peak temp T_P	260-265 °C
5 °C below peak temperature t_P	30 seconds
Ave cooling rate (T_P to T_L)	6 °C/second max
Normal temperature 25°C to peak temperature TP time	8 minutes max

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Data sheet status	Revision date
V1.0	Initial version.	June 2026