FEATURES

- Compliant with ISO 11898-2:2024 and SAE J2284-1 to SAE J2284-5
- AEC-Q100 Grade 1 qualified
- Very low power consumption in Standby and Sleep modes
- Support the remote wake-up of standard CAN wake-up frame, compatible with ISO 11898-2:2024 standard of selective wake-up frame remote wake-up.
- Wake-up source recognition
- ±58V BUS protection
- ±30V receiver common mode input voltage
- VIO input allows for 1.8V, 3.3V to 5V MCU
- Driver (TXD) dominant timeout function
- Undervoltage detection on pins VBAT, VCC and VIO
- Timing guaranteed for data rates up to 8Mbit/s in the CAN FD fast phase
- Sleep mode INH output pin with power disable function
- -40°C to 150°C junction temperature range with over temperature protection
- Low ElectroMagnetic Emissions (EME)
- Unpowered nodes don’t interfere with the bus
- Autonomous bus biasing
- Available in SOP14 and leadless DFN4.5×3.0-14 packages. DFN4.5×3.0-14 with improved Automated Optical Inspection (AOI) capability

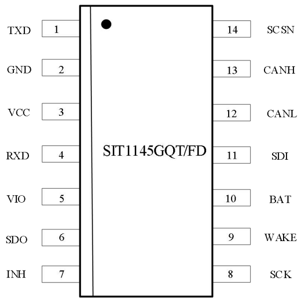
DESCRIPTION

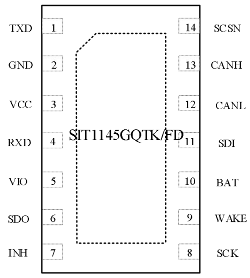
The SIT1145GQ is an interface chip applied between CAN protocol controller and physical bus, supports 8Mbps Flexible Data-Rate, and has the capability of differential signal transmission between bus and CAN protocol controller. The SIT1145GQ features very low power consumption in Standby and Sleep modes and supports ISO 11898-2:2024 compliant CAN Partial Networking by means of a selective wake-up function.

Partial Networking function has been embedded into the SIT1145GQ/FD. This function is called “FD-passive”, which can ignore CAN FD frames while waiting for a valid wake-up frame in Sleep/Standby mode. This additional feature of partial networking is the perfect fit for networks that support both CAN FD and standard CAN 2.0 communications. It allows normal CAN controllers that do not need to communicate CAN FD messages to remain in partial networking Sleep/Standby mode during CAN FD communication without generating bus errors.

The SIT1145GQ is suitable for use in 12V and 24V system. SIT1145GQ supports ±58V BUS protection function. The SIT1145GQ uses advanced power management to adjust the power supply of the entire node and supports local and remote wake up functions. The I/O levels are automatically adjusted to the I/O levels of the controller, allowing the SIT1145GQ to interface directly with 1.8V to 5V microcontrollers. An SPI interface is provided for transceiver control and status information retrieval. The bus connections are truly floating when power is off.

PIN CONFIGURATION





PINNING INFORMATION

Pin	Symbol	Description
1	TXD	transmit data input
2	GND	ground
3	VCC	5V CAN transceiver supply voltage
4	RXD	receive data output; reads out data from the bus lines
5	VIO	supply voltage for I/O level adaptor
6	SDO	SPI data output
7	INH	inhibit output for switching external voltage regulators
8	SCK	SPI clock input
9	WAKE	local wake-up input
10	BAT	batter supply voltage
11	SDI	SPI data input
12	CANL	LOW-level CAN bus line
13	CANH	HIGH-level CAN bus line
14	SCSN	SPI chip select input

NOTE: The exposed pad of the DFN4.5×3.0-14 package is internal connected to the GND pin of the chip. For enhanced thermal performance, the exposed pad of the DFN4.5×3.0-14 package could be soldered to board ground.

BLOCK DIAGRAM

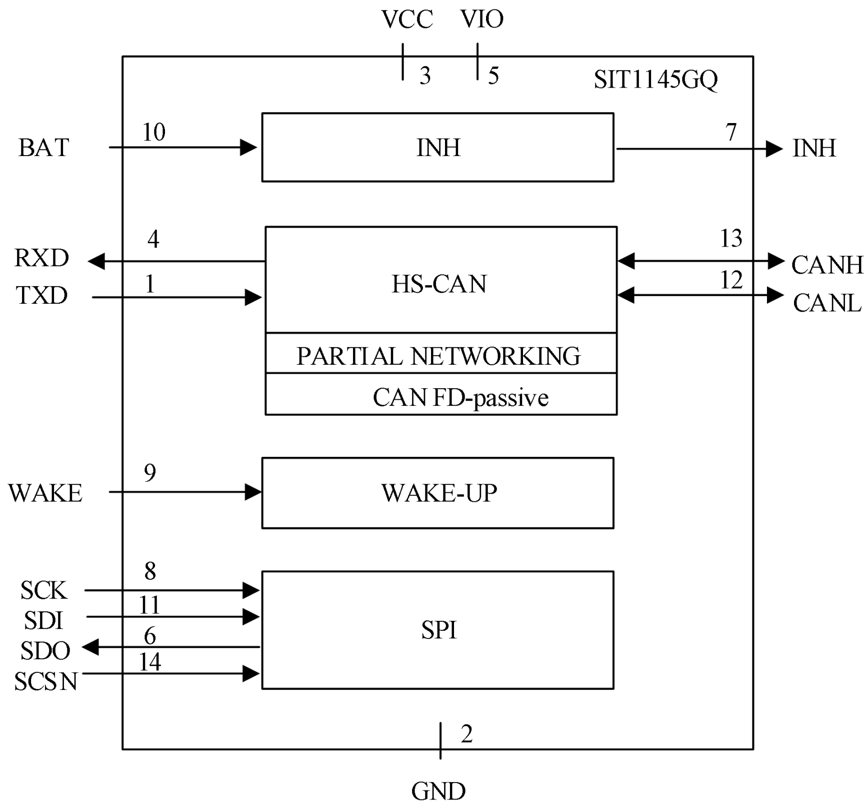


Fig 2 Block diagram

RECOMMENDED WORK STATUS

Parameter	Symbol	Value	Unit
Battery supply voltage	V_{BAT}	4.5~40	V
Supply voltage	V_{CC}	4.5~5.5	V
Supply voltage on pin VIO	V_{IO}	1.7~5.5	V
Power-off detection threshold voltage	$V_{th(det)poff}$	2.8~3.3	V
Undervoltage detection voltage on pin VCC	$V_{uvd(VCC)}$	4.0~4.5	V
Undervoltage detection voltage on pin VIO	$V_{uvd(VIO)}$	1.5~1.7	V
Voltage on pin CANH	V_{CANH}	-58~58	V
Voltage on pin CANL	V_{CANL}	-58~58	V
Operating temperature	T_A	-40~125	℃

LIMITING VALUES

Parameter	Symbol	Conditions	Value	Unit
Battery supply voltage	V_{BAT}		-0.3~+58	V
Supply voltage	V_{CC}, V_{IO}		-0.3~+6	V
Voltage on pin WAKE, INH	V_{WAKE}, W_{INH}		-18~+58	V
MCU side port voltage	V_{TXD}, V_{RXD}, V_{SDI}, V_{SDO}, V_{SCK}, V_{SCSN}		-0.3~+6	V
Bus side input voltage	V_{CANH}, V_{CANL}		-58~+58	V
Bus differential breakdown voltage	$V_{(CANH-CANL)}$		-58~+58	V
Contact discharge model (IEC) (1)	V_{ESD_IEC}	pins CANH, CANL	±8	kV
		VBAT pin (with 10nF capacitor); WAKE pin (with 33kΩ resistor)	±8	kV
Human body model (HBM) (2)	V_{ESD_HBM}	all pins	±4	kV
		pins CANH and CANL to GND	±8	kV
Charged device model (CDM) (3)	V_{ESD_CDM}	all pins	±2000	V
Transient voltage (4)	V_{trt}	pulse 1	-100	V
		pulse 2a	75	V
		pulse 3a	-150	V
		pulse 3b	100	V
Storage temperature	T_{stg}		-55~150	℃

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

(1) According to IEC 61000-4-2;
(2) According to AEC-Q100-002;
(3) According to AEC-Q100-011;
(4) According to ISO7637-2: pins CANH, CANL, BAT, WAKE.

THERMAL CHARACTERISTICS

Symbol	Parameter	Condition	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	SOP14	91	°C/W
		DFN4.5*3-14	36	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	SOP14	42	°C/W
		DFN4.5*3-14	32	°C/W

MODE TRANSITIONS

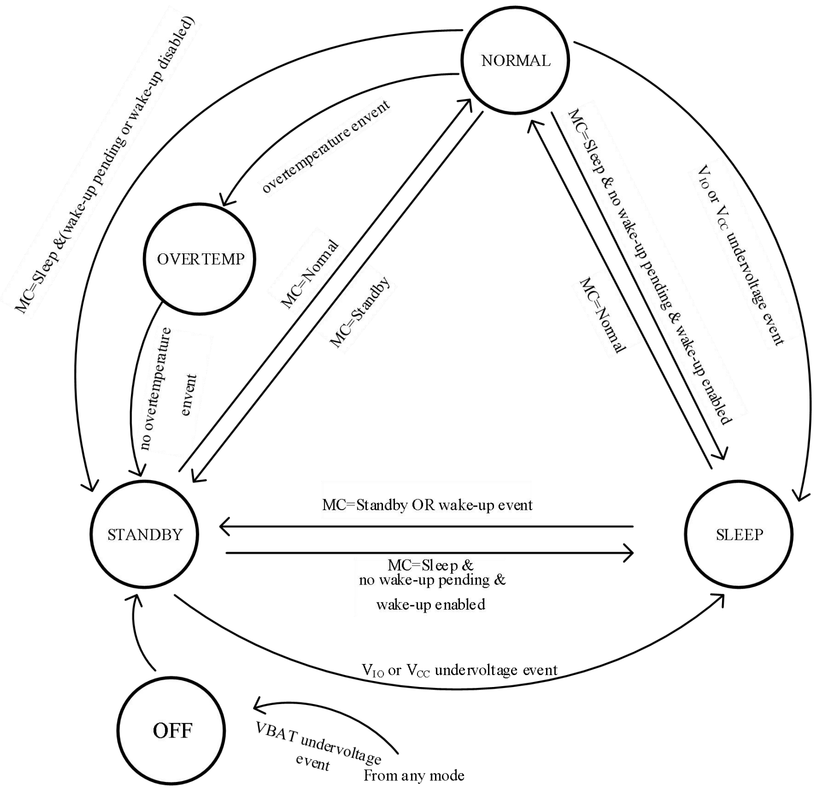


Fig 3 system controller state diagram

FUNCTIONAL DESCRIPTION

System controller

The SIT1145GQ is a stand-alone high-speed CAN transceiver, which combines the functions of SIT1043G with ISO 11898-2:2024 CAN Partial Networking and autonomous bus bias. The transceiver has a variety of integrating fault safety and diagnosis functions with enhanced system reliability and advanced power management.

The system controller manages register configuration and controls the internal functions of the SIT1145GQ. Detailed device status information is collected and made available to the microcontroller.

The system controller contains a state machine that supports five operating modes: Normal, Standby, Sleep, Overtemp and Off. The state transitions are shown in Fig 3.

Normal mode

Normal mode is the active operating mode. In this mode, the SIT1145GQ is fully operational and all device hardware is available and can be activated (see Table 1).

Through the SPI command (MC = 111), normal mode can be selected from Standby or Sleep mode.

Standby mode

Standby mode is the first-level power-saving mode of the SIT1145GQ, featuring low current consumption. In Standby mode, the transceiver can't transmit or receive data, but the INH pin remains active, so voltage regulators controlled by this pin will be active.

If remote CAN wake-up is enabled (CWE = 1; Table 19), the receiver receives a wake-up request by monitoring the bus activity. The bus pins are biased to GND when the bus is inactive and at approximately 2.5V when there is activity on the bus (autonomous biasing). CAN wake-up can be performed in standard wake-up or via a selective wake-up frame (selective wake-up is enabled when CPNC = PNCOK = 1; Otherwise, standard wake-up is enabled).

Pin RXD is forced LOW when any enabled wake-up or interrupt events is detected. (see "wake-up and interrupt event diagnosis via pin RXD")

The SIT1145GQ switches to Standby mode:

- From Off mode if the battery voltage rises above the power-on detection threshold, $V_{th(det)pon}$.
- From Overtemp mode if the chip temperature falls below the overtemperature protection release threshold, $T_{th(rel)otp}$.
- From Sleep mode on the occurrence of a wake-up or interrupt event. (see "wake-up and interrupt event diagnosis via pin RXD")
- From Normal or Sleep mode is selected via an SPI command (MC = 001) while a wake-up event is pending or all wake-up sources are disabled.

Sleep mode

Sleep mode is the second-level power saving mode of the SIT1145GQ. In Sleep mode, the transceiver behaves as in Standby mode with the exception that pin INH is set to a high-ohmic state. The voltage regulator controlled by the INH pin will be turned off and the current flowing into the BAT pin will be minimized.

Any enabled wake-up or interrupt event (except SPIF), or an SPI command (provided a valid V_{IO} voltage is connected), will wake up the transceiver from Sleep mode.

Through an SPI command (MC = 001), Sleep mode can be selected from Normal or Standby mode. The SIT1145GQ will switch to Sleep mode on receipt of this command, provided there are no pending wake-up events and at least one regular wake-up source (CAN bus or WAKE pin; see "wake-up and interrupt event diagnosis via pin RXD") is enabled. When one of these conditions has not been met, any attempt to enter Sleep mode will cause the SIT1145GQ to switch to Standby mode.

The SIT1145GQ will also be forced to switch to Sleep mode after $t_{d(uvd-sleep)}$ if a V_{CC} of V_{IO} undervoltage event is detected ($V_{CC}/V_{IO} < V_{uvd(VCC)}/V_{uvd(VIO)}$ for longer than $t_{det(uv)(VCC)}/t_{det(uv)(VIO)}$). In this event, all pending wake-up events will be cleared. CAN wake-up (CWE = 1) and local wake-up via the WAKE pin (WPFE = WPRE = 1) are enabled in order to avoid a system deadlock (see "VCC/VIO undervoltage protection") and selective wake-up is disabled (CPNC = 0).

The status bit FSMS in the main status register (Table 3) indicates whether the sleep mode is selected by the SPI command (FSMS = 0) or enforced by the VCC or VIO undervoltage event (FSMS = 1). This bit can be read after the SIT1145GQ wakes up from Sleep mode to allow the settings of CWE, WPFE, WPRE and CPNC to be re-adjusted if an undervoltage event forced the transition to Sleep mode (FSMS = 1).

Off mode

The SIT1145GQ will be in Off mode when the battery voltage is too low to supply the IC. This is the default mode when the battery is first connected. The SIT1145GQ will switch to Off mode from any mode if the battery voltage drops below the power-off threshold ($V_{th(det)poff}$). In Off mode, the CAN pins and INH pin are in a high-ohmic state.

When the battery supply voltage rises above the power-on threshold ($V_{th(det)pon}$), the SIT1145GQ starts to boot up, triggering an initialization procedure. The SIT1145GQ will switch to Standby mode after $t_{startup}$.

Overtemp mode

Overtemp mode is provided to prevent SIT1145GQ from being damaged by excessive temperatures. The SIT1145GQ switches immediately to Overtemp mode from Normal mode when the global chip temperature rises above the overtemperature protection activation threshold, $T_{th(act)otp}$.

To prevent data loss caused by overtemperature, SIT1145GQ issues a warning when the IC temperature rises above the overtemperature warning threshold ($T_{th(warn)otp}$). When this happens, the status bit OTWS is set to

1, and if enabled (OTWE = 1), an overtemperature interrupt (OTW = 1) occurs.

In Overtemp mode, the CAN transmitter and receiver are disabled and the CAN pins are in a high-ohmic state. Wake-up events will not be detected, but a pending wake-up will still be signaled by a LOW level on pin RXD, which will persist after the overtemperature event has been cleared.

The SIT1145GQ exits Overtemp mode:

- and switches to Standby mode if the chip temperature falls below the overtemperature protection release threshold, $T_{th(rel)otp}$
- if the device is forced to switch to Off mode ($V_{BAT} < V_{th(det)poff}$)

Table 1 Hardware characterization by functional block

Block	Operating mode				
	Off	**Standby**	**Normal**	**Sleep**	**Overtemp**
SPI	Disabled	Active	Active	Active if VIO supplied	Disabled
INH	High-ohmic	V_{BAT} level	V_{BAT} level	High-ohmic	V_{BAT} level
CAN	Off	Offline	Active/ Offline/ Listen-only (determined by bits CMC; see Table 4)	Offline	Off
RXD	V_{IO} level	V_{IO} level/LOW if wake-up event detected	CAN bit stream if CMC = 01/10/11; otherwise, same as Standby/Sleep	V_{IO} level/LOW if wake-up event detected	V_{IO} level/LOW if wake-up pending

SYSTEM CONTROL REGISTERS

The operating mode is selected via bits MC in the Mode control register. The Mode control register is accessed via SPI address 0x01.

Table 2 Mode control register (address 01h)

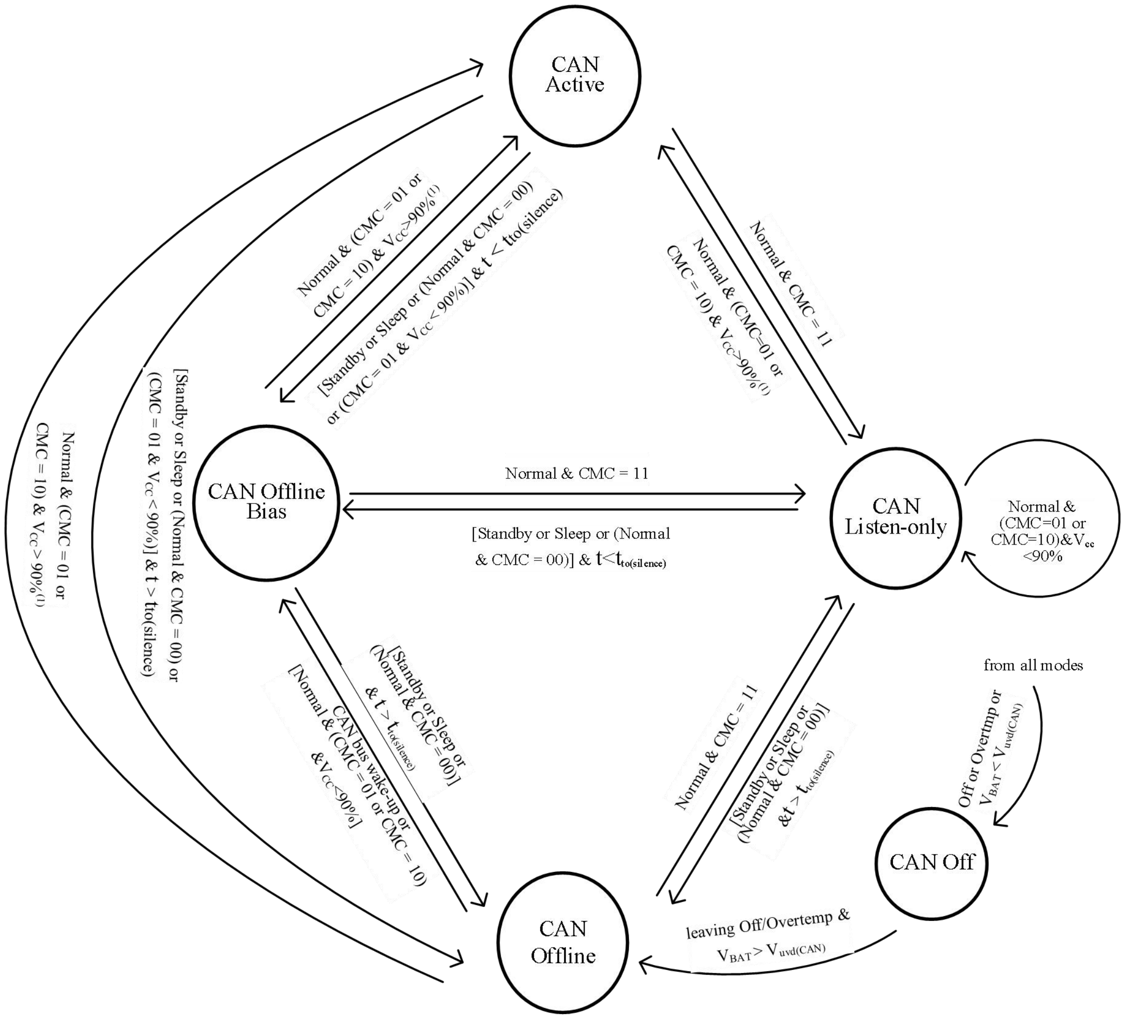
Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2:0	MC	R/W		mode control:
			001	Sleep mode
			100	Standby mode
			111	Normal mode

The Main status register can be accessed to monitor the status of the overtemperature warning flag and to determine whether the SIT1145GQ has entered Normal mode after initial power-up. Bit FSMS indicates whether the most recent transition to Sleep mode was triggered by an undervoltage event or by an SPI command.

Table 3 Main status register (address 03h)

Bit	Symbol	Access	Value	Description
7	FSMS	R		Sleep mode transition status:
			0	transition to Sleep mode triggered by an SPI command
			1	an undervoltage on VCC and/or VIO forced a transition to Sleep mode
6	OTWS	R		overtemperature warning status:
			0	IC temperature below overtemperature warning threshold
			1	IC temperature above overtemperature warning threshold
5	NMS	R		Normal mode status:
			0	SIT1145GQ has entered Normal mode (after power-up)
			1	SIT1145GQ has powered up but has not yet switched to Normal mode
4:0	reserved	R	-	

CAN TRANSCEIVER STATE MACHINE



(1) To prevent the bus lines being driven to a permanent dominant state, the transceiver will not switch to CAN Active mode if pin TXD is held LOW (e.g. by a short-circuit to GND)

Fig 4 CAN transceiver state machine

CAN FUNCTIONAL DESCRIPTION

CAN controller

The integrated high-speed CAN transceiver is designed for active communication at bit rates up to 1 Mbit/s, providing differential transmit and receive capability to a CAN protocol controller. The transceiver is compliant with ISO 11898-2:2024 (defining high-speed CAN with selective wake-up functionality and autonomous bus biasing). The CAN transmitter is supplied via pin VCC while the CAN receiver is supplied via pin BAT. The SIT1145GQ includes additional timing parameters on loop delay symmetry to ensure reliable communication in fast phase at data rates up to 8 Mbit/s, as used in CAN FD networks.

The CAN transceiver supports autonomous CAN biasing, which helps to minimize RF emissions. CANH and CANL are always biased to 2.5 V when the transceiver is in Active or Listen-only modes (CMC = 01/10/11).

Autonomous biasing is active in CAN Offline mode - to 2.5 V if there is activity on the bus (CAN Offline Bias mode) and to GND if there is no activity on the bus for $t > t_{to(silence)}$ (CAN Offline mode).

This is useful when the node is disabled due to a malfunction in the microcontroller or when CAN partial networking is enabled. The SIT1145GQ ensures that the CAN bus is correctly to avoid interfering with ongoing communications between other nodes. The autonomous CAN bias voltage is derived directly from V_{BAT}.

The integrated CAN transceiver supports four operating modes: Active, Listen-only, Offline and Offline Bias (see Fig 3). The CAN transceiver operating mode depends on the SIT1145GQ operating mode and on the setting of bits CMC in the CAN control register (Table 4).

When the SIT1145GQ is in Normal mode, the CAN transceiver operating mode (Offline, Active or Listen-only) can be selected via bits CMC in the CAN control register (Table 4).

When the SIT1145GQ is in Standby or Sleep modes, the transceiver is forced to Offline or Offline Bias mode (depending on bus activity).

CAN Active mode

In CAN Active mode, the transceiver can transmit and receive data via CANH and CANL. The differential receiver converts the analog data on the bus lines into digital data, which is output on pin RXD. The transmitter converts digital data generated by the CAN controller (input on pin TXD) into analog signals suitable for transmission over the CANH and CANL bus lines.

CAN Active mode is selected when CMC = 01 or 10. When CMC = 01, VCC undervoltage detection is enabled and the transceiver switches to CAN Offline or CAN Offline Bias mode when the voltage on VCC drops below $V_{uvd(VCC)}$. When CMC = 10, VCC undervoltage detection is disabled. The transmitter will remain active until the SIT1145GQ is forced into Sleep mode by the VCC undervoltage event; the transceiver will then switch to CAN Offline or CAN Offline Bias mode.

The CAN transceiver is in Active mode when:

- SIT1145GQ is in Normal mode (MC = 111) and the CAN transceiver has been enabled by setting bits CMC in the CAN control register to 01 or 10 (see Tabel 4) and:
- if CMC = 01, the voltage on pin VCC is above the V_{CC} undervoltage detection threshold ($V_{uvd(VCC)}$)

If pin TXD is held LOW (e.g. by a short-circuit to GND) when CAN Active mode is selected via bits CMC, the transceiver will not enter CAN Active mode but will switch to or remain in CAN Listen-only mode. It will remain in Listen-only mode until pin TXD goes HIGH in order to prevent a hardware and/or software application failure from driving the bus lines to an unwanted dominant state.

In CAN Active mode, the CAN bias voltage is derived from VCC.

The application can determine whether the CAN transceiver is ready to transmit/receive data or is disabled by reading the CAN Transceiver Status (CTS) bit in the Transceiver Status Register (Table 5).

CAN Listen-only mode

CAN Listen-only mode allows the SIT1145GQ to monitor bus activity while the transceiver is inactive, without influencing bus levels. This facility could be used by development tools that need to listen to the bus but do not need to transmit or receive data or for software-driven selective wake-up. Dedicated microcontrollers could be used for selective wake-up, providing an embedded low-power CAN engine designed to monitor the bus for potential wake-up events.

In Listen-only mode the CAN transmitter is disabled, reducing current consumption. The CAN receiver and CAN biasing remain active. This enables the host microcontroller to switch to a low-power mode in which an embedded CAN protocol controller remains active, waiting for a signal to wake up the microcontroller.

The CAN transceiver is in Listen-only mode when:

- the SIT1145GQ is in Normal mode and CMC = 11

The CAN transceiver will not leave Listen-only mode while TXD is LOW or CAN Active mode is selected with CMC = 01 or 10 while the voltage on VCC is below the undervoltage threshold, $V_{uvd(VCC)}$.

CAN Offline and Offline Bias modes

In CAN Offline mode, the transceiver monitors the CAN bus for a wake-up event, provided CAN wake-up detection is enabled (CWE = 1). CANH and CANL are biased to GND.

CAN Offline Bias mode is the same as CAN Offline mode, with the exception that the CAN bus is biased to 2.5V. This mode is activated automatically when activity is detected on the CAN bus while the transceiver is in CAN Offline mode. The transceiver will return to CAN Offline mode if the CAN bus is silent (no CAN bus edges) for longer than $t_{to(silence)}$.

The CAN transceiver switches to CAN Offline mode from CAN Active mode or CAN Listen-only mode if:

- the SIT1145GQ switches to Standby or Sleep mode or
- the SIT1145GQ is in Normal mode and CMC = 00

provided the CAN-bus has been inactive for at least $t_{to(silence)}$. If the CAN-bus has been inactive for less than $t_{to(silence)}$, the CAN transceiver switches first to CAN Offline Bias mode and then to CAN Offline mode once the bus has been silent for $t_{to(silence)}$.

The CAN transceiver switches to CAN Offline/Offline Bias mode from CAN Active mode if CMC = 01 and the voltage on VCC drops below the undervoltage threshold or if CMC = 10 and the SIT1145GQ switches to Sleep mode in response to a VCC undervoltage event.

The CAN transceiver switches to CAN Offline mode:

- from CAN Offline Bias mode if no activity is detected on the bus (no CAN edges) for $t > t_{to(silence)}$ or
- when the SIT1145GQ switches from Off or Overtemp mode to Standby mode

The CAN transceiver switches from CAN Offline mode to CAN Offline Bias mode if:

- a standard wake-up pattern is detected on the CAN bus or
- the CAN transceiver is in Normal mode, CMC = 01 or 10 and VCC < 90 %

CAN Off mode

The CAN transceiver is switched off completely with the bus lines floating when:

- the SIT1145GQ switches to Off or Overtemp mode or
- V_{BAT} falls below the CAN receiver undervoltage detection threshold, $V_{uvd(CAN)}$

It will be switched on again on entering CAN Offline mode when V_{BAT} rises above the undervoltage recovery threshold ($V_{uvr(CAN)}$) and the CAN transceiver is no longer in Off/Overtemp mode. CAN Off mode prevents reverse currents flowing from the bus when the battery supply to the CAN transceiver is lost.

CAN standard wake-up (partial networking not enabled)

If the CAN transceiver is in Offline mode and CAN wake-up is enabled (CWE = 1), but CAN selective wake-up is disabled (CPNC = 0 or PNCOK = 0), the SIT1145GQ will monitor the bus for a standard wake-up pattern.

A filter at the receiver input prevents unwanted wake-up events occurring due to automotive transients or EMI. This filtering helps avoid spurious wake-up events. A spurious wake-up sequence could be triggered by, for example, a dominant clamped bus or by dominant phases due to noise or spikes on the bus.

The SIT1145GQ wakes up from Standby or Sleep mode when a dedicated wake-up pattern (specified in ISO 11898-2:2024) is detected on the bus.

The wake-up pattern consists of:

- a dominant phase of at least $t_{wake(busdom)}$ followed by
- a recessive phase of at least $t_{wake(busrec)}$ followed by
- a dominant phase of at least $t_{wake(busdom)}$

Dominant or recessive bits between the above-mentioned phases that are shorter than $t_{wake(busdom)}$ and $t_{wake(busrec)}$ respectively are ignored.

The complete dominant-recessive-dominant pattern must be received within $t_{to(wake)}$bus to be recognized as a valid wake-up pattern (see Fig 5). Otherwise, the internal wake-up logic is reset. The complete wake-up pattern will then need to be retransmitted to trigger a wake-up event. Pin RXD remains HIGH until the wake-up event has been triggered.

When a valid CAN wake-up pattern is detected on the bus, wake-up bit CW in the Transceiver event status register is set (see Table 16) and pin RXD is driven LOW. If the SIT1145GQ was in Sleep mode when the wake-up pattern was detected, it will switch pin INH to VBAT to activate external voltage regulators (e.g. for supplying VCC and VIO) and enter Standby mode.

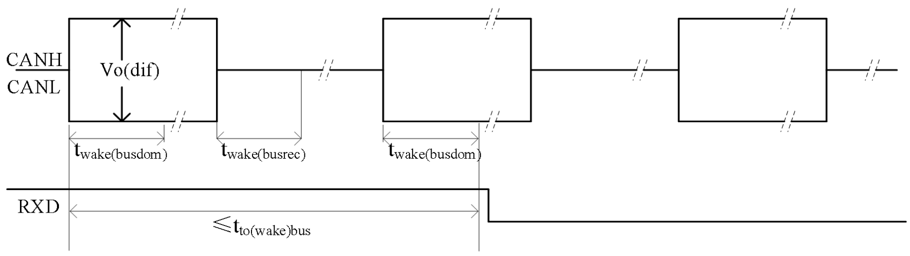


Fig 5 CAN wake-up timing

CAN CONTROL AND TRANSCEIVER STATUS REGISTERS

Table 4 CAN control register (address 20h)

Bit	Symbol	Access	Value	Description
7	reserved	R	-	
6	CFDC	R/W		CAN FD tolerance
			0	CAN FD tolerance disabled
			1	CAN FD tolerance enabled
5	PNCOK	R/W		CAN partial networking configuration:
			0	partial networking register configuration invalid (wake-up via standard wake-up pattern only)
			1	partial networking registers configured successfully
4	CPNC	R/W		CAN selective wake-up; when enabled, node is part of a partial network:
			0	disable CAN selective wake-up
			1	enable CAN selective wake-up
3:2	reserved	R	-	
1:0	CMC	R/W		CAN transceiver operating mode selection:
			00	Offline mode
			01	Active mode (while SIT1145GQ is in Normal mode); V_{CC} undervoltage detection active; transition to Active mode, and remaining in Active mode, requires V_{CC} above undervoltage threshold
			10	Active mode (while SIT1145GQ is in Normal mode); V_{CC} undervoltage detection inactive; transition to Active mode requires V_{CC} above undervoltage threshold
			11	Listen-only mode

Table 5 Transceiver status register (address 22h)

Bit	Symbol	Access	Value	Description
7	CTS	R		CAN transceiver status:
			0	CAN transceiver not in Active mode
			1	CAN transceiver in Active mode
6	CPNERR	R		CAN partial networking error status:
			0	no CAN partial networking error detected (PNFDE = 0 and PNCOK = 1)
			1	CAN partial networking error detected (PNFDE = 1 or

				PNCOK = 0); wake-up via standard wake-up pattern only
5	CPNS	R		CAN partial networking status:
			0	CAN partial networking configuration error detected (PNCOK = 0)
			1	CAN partial networking configuration OK (PNCOK = 1)
4	COSCS	R		CAN oscillator status:
			0	CAN partial networking oscillator not running at target frequency
			1	CAN partial networking oscillator running at target frequency
3	CBSS	R		CAN bus silence status:
			0	CAN bus active (communication detected on bus)
			-	CAN bus inactive (for longer than $t_{to(silence)}$)
2	reserved	R	-	
1	VCS(1)	R		VCC supply voltage status:
			0	V_{CC} is above the undervoltage detection threshold ($V_{uvd(VCC)}$)
			1	V_{CC} is below the undervoltage detection threshold ($V_{uvd(VCC)}$)
0	CFS	R		CAN failure status:
			0	no TXD dominant time-out event detected
			1	CAN transmitter disabled due to a TXD dominant time-out event

(1) Only active when CMC = 01.

CAN PARTIAL NETWORKING

Partial networking allows nodes in a CAN network to be selectively activated in response to dedicated wake-up frames (WUF). Only nodes that are functionally required are active on the bus while the other nodes remain in a low-power mode until needed.

If CAN wake-up (CWE = 1) and CAN selective wake-up (CPNC = 1) are both enabled, and the partial networking registers are configured correctly (PNCOK = 1), the transceiver monitors the bus for dedicated CAN wake-up frames.

WAKE-UP FRAME (WUF)

According to ISO 11898-1:2024, CAN wake-up frame is composed of an identifier field (ID), a Data Length Code (DLC), a data field and a Cyclic Redundancy Check (CRC) code including the CRC delimiter.

The wake-up frame format, standard (11-bit) or extended (29-bit) identifier, is selected via bit IDE in the Frame control register (Table 9).

A valid WUF identifier is defined and stored in the ID registers (Table 7). An ID mask can be defined to allow a group of identifiers to be recognized as valid by an individual node. The identifier mask is defined in the mask registers (Table 8), where a 1 means "don't care ".

In the example of the standard frame format shown in Fig 6, based on the standard frame format, the 11-bit identifier definition is 0x1A0. The identifier is stored in ID registers 2 (0x29) and 3 (0x2A). The three least significant bits of the ID mask, bits 2 to 4 of Mask register 2 (0x2D) are set to 1, which means that the corresponding identifier bits are "don't care". This means that any of the eight different identifiers in the received WUF (from 0x1A0 to 0x1A7) will be recognized as a valid wake-up frame.

SIT1145GQ SPI Settings

11-bit Identifier field: 0x1A0 stored in ID registers 2 and 3	0	0	1	1	0	1	0	0	0	0	0
ID mask: 0x007 stored in Mask registers 2 and 3	0	0	0	0	0	0	0	0	1	1	1
Valid wake-up Identifiers: 0x1A0 to 0x1A7	0	0	1	1	0	1	0	0	x	x	x

Fig 6 Evaluating the ID field in a selective wake-up frame

The data field indicates which nodes are to be woken up. Within the data field, groups of nodes can be pre-defined and associated with bits in a data mask. By comparing the incoming data field with the data mask, multiple groups of nodes can be woken up simultaneously with a single wake-up message.

The data length code (bits DLC in the Frame control register; Table 9) determines the number of data bytes (between 0 and 8) expected in the data field of a CAN wake-up frame. If one or more data bytes are expected (DLC ≠ 0000), the field of the wake-up frame received by at least one bit in the data field must be set to 1 and at least one equivalent bit in the relevant data mask register in the transceiver (see Table 10) must also be set to 1 for a successful wake-up. Each matching pair of 1s indicates a group of nodes to be activated (since the data field is up to 8 byes long, up to 64 groups of nodes can be defined).

If DLC = 0000, if the WUF contains a valid identifier and the received data length code is 0000, a node will wake up regardless of the values stored in the data mask. If DLC ≠ 0000 and all data mask bits are set to 0, the device cannot be woken up through the CAN bus (Note: by default, all data mask bits are set to 1; see Table Table 28). If a WUF contains a valid ID but the DLCs (in the Frame control register and the WUF) don't match, the data field is ignored and no nodes are woken up.

In the example shown in Fig 7, the data field consists of a single byte (DLC = 1). This means that the data field in the incoming wake-up frame is evaluated against data mask 7 (stored at address 6Fh; see Table 10 and Fig 8). In the example, data mask 7 is defined as 10101000. This means that up to three groups of nodes could be woken up (group 1, 3 and 5) if the respective bits in the data frame are also set to 1.

The received message shown in Fig 7 could, potentially, wake up three groups of nodes: groups 3, 4 and 5. Two matches are found (groups 3 and 5) when the message data bits are compared with the configured data mask (DM7).

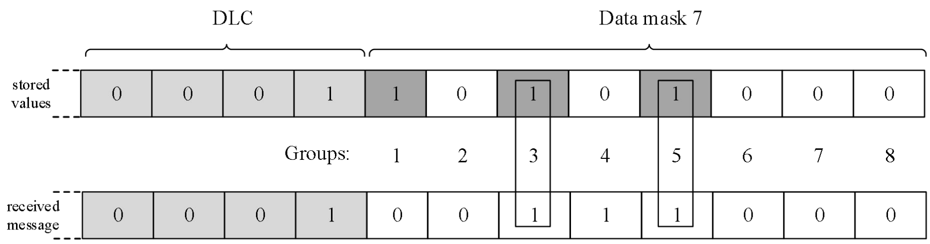


Fig 7 Evaluating the Data field in a selective wake-up frame

Optionally, the data length code and the data field can be excluded from the evaluation of the wake-up frame. If bit PNDM = 0, only the identifier field is evaluated to determine if the frame contains a valid wake-up message. If PNDM = 1 (the default value), the data field is included in the wake-up filtering.

When PNDM = 0, a valid wake-up message is detected and a wake-up event is captured (and CW is set to 1) when:

- the identifier field in the received wake-up frame matches the pattern in the ID registers after filtering and
- the CRC field in the received frame (including a recessive CRC delimiter) was received without error

When PNDM = 1, a valid wake-up message is detected when:

- the identifier field in the received wake-up frame matches the pattern in the ID registers after filtering and
- the frame is not a Remote frame and
- the data length code in the received message matches the configured data length code (bits DLC) and
- if the data length code is greater than 0, at least one bit in the data field of the received frame is set and the corresponding bit in the associated data mask register is also set and
- the CRC field in the received frame (including a recessive CRC delimiter) was received without error.

If the SIT1145GQ receives a CAN message containing errors (e.g. a “stuffing” error) transmitted in advance of the ACK field, an internal error counter is incremented. If a CAN message is received without any errors appearing in front of the ACK field, the counter is decremented. Data received after the CRC delimiter and before the next SOF is ignored by the partial networking module. If the counter overflows (counter > 31), a frame detect error is captured (PNFDE = 1) and the device wakes up; the counter is reset to zero when the bias is switched off and partial networking is re-enabled.

Partial networking is assumed to be configured correctly when PNCOK is set to 1 by the application software. The SIT1145GQ clears PNCOK after a write access to any of the CAN partial networking configuration registers.

If selective wake-up is disabled (CPNC = 0) or partial networking is not configured correctly (PNCOK = 0), and the CAN transceiver is in Offline mode with wake-up enabled (CWE = 1), then any valid wake-up pattern (according to ISO 11898-2:2024) will trigger a wake-up event.

If the CAN transceiver is not in Offline mode (CMC ≠ 00) or CAN wake-up is disabled (CWE = 0), all wake-up patterns on the bus will be ignored.

CAN bit rates of 50 kbit/s, 100 kbit/s, 125 kbit/s, 250 kbit/s, 500 kbit/s and 1 Mbit/s are supported during selective wake-up. The bit rate is selected via bits CDR (see table 6).

CAN FD FRAMES

CAN FD stands for “CAN with Flexible Data-Rate”. It is based on the CAN protocol as specified in ISO 11898-1:2024.

CAN FD is being gradually introduced into the automotive market. In time, all CAN controllers will be required to comply with the new standard (enabling “FD-active” nodes) or at least to tolerate CAN FD communication (enabling “FD-passive” nodes). The SIT1145GQ/FD variants support FD-passive features by means of a dedicated implementation of the partial networking protocol.

These variants can be configured to recognize CAN FD frames as valid frames. When CFDC = 1, the error counter is decremented every time the control field of a CAN FD frame is received. The SIT1145GQ/FD remains in low-power mode (“CAN FD-passive”) with partial networking enabled. CAN FD frames are never recognized as valid wake-up frames, even if PNDM = 0 and the frame contains a valid ID. After receiving the control field of a CAN FD frame, the SIT1145GQ/FD ignores further bus signals until idle is again detected.

CAN FD passive is supported up to a ratio of one-to-eight between arbitration and data bit rates, without unwanted wake-ups. The CAN FD filter parameter defined in ISO 11898-2:2024 and SAE J2284 is supported up to a ratio of one-to-four, with a maximum supported bit data bit rate of 2 Mbit/s and a maximum arbitration speed of 500 kbit/s.

CAN FD frames are interpreted as frames with errors by the partial networking module when CFDC = 0. So the error counter is incremented when a CAN FD frame is received. If the ratio of CAN FD frames to valid CAN frames exceeds the threshold that triggers error counter overflow, bit PNFDE is set to 1 and the device wakes up.

CAN PARTIAL NETWORKING CONFIGURATION REGISTERS

Dedicated registers are provided for configuring CAN partial networking.

Table 6 Data rate register (address 26h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2:0	CDR	R/W		CAN data rate selection:
			000	50kbit/s
			001	100kbit/s
			010	125kbit/s
			011	250kbit/s
			100	reserved (intended for future use; currently selects 500 kbit/s)
			101	500kbit/s
			110	reserved (intended for future use; currently selects 500 kbit/s)
			111	1000kbit/s

Table 7 ID registers 0 to 3 (addresses 27h to 2Ah)

Addr.	Bit	Symbol	Access	Value	Description
27h	7:0	ID7:ID0	R/W	-	bits ID7 to ID0 of the extended frame format
28h	7:0	ID15:ID08	R/W	-	bits ID15 to ID8 of the extended frame format
29h	7:2	ID23:ID18	R/W	-	bits ID23 to ID18 of the extended frame format bits ID5 to ID0 of the standard frame format
	1:0	ID17:ID16	R/W	-	bits ID17 to ID16 of the extended frame format
2Ah	7:5	reserved	R	-	
	4:0	ID28:ID24	R/W	-	bits ID28 to ID24 of the extended frame format bits ID10 to ID6 of the standard frame format

Table 8 ID mask registers 0 to 3 (addresses 2Bh to 2Eh)

Addr.	Bit	Symbol	Access	Value	Description
2Bh	7:0	M7:M0	R/W	-	ID mask bits 7 to 0 of extended frame format
2Ch	7:0	M15:M8	R/W	-	ID mask bits 15 to 8 of extended frame format

Addr.	Bit	Symbol	Access	Value	Description
2Dh	7:2	M23:M18	R/W	-	ID mask bits 23 to 18 of extended frame format ID mask bits 5 to 0 of standard frame format
	1:0	M17:M16	R/W	-	ID mask bits 17 to 16 of extended frame format
2Eh	7:5	reserved	R	-	
	4:0	M28:M24	R/W	-	ID mask bits 28 to 24 of extended frame format ID mask bits 10 to 6 of standard frame format

Table 9 Frame control register (address 2Fh)

Bit	Symbol	Access	Value	Description
7	IDE	R/W	-	identifier format:
			0	standard frame format (11-bit)
			1	extended frame format (29-bit)
6	PNDM	R/W	-	partial networking data mask:
			0	data length code and data field are 'don't care' for wake-up
			1	data length code and data field are evaluated at wake-up
5:4	reserved	R	-	
3:0	DLC	W/R		number of data bytes expected in a CAN frame:
			0000	0
			0001	1
			0010	2
			0011	3
			0100	4
			0101	5
			0110	6
			0111	7
			1000	8
			1001 to 1111	tolerated, 8 bytes expected

Table 10 Data mask registers (addresses 68h to 6Fh)

Addr.	Bit	Symbol	Access	Value	Description
68h	7:0	DM0	W/R	-	data mask 0 configuration
69h	7:0	DM1	W/R	-	data mask 1configuration
6Ah	7:0	DM2	W/R	-	data mask 2 configuration

Addr.	Bit	Symbol	Access	Value	Description
6Bh	7:0	DM3	W/R	-	data mask 3 configuration
6Ch	7:0	DM4	W/R	-	data mask 4 configuration
6Dh	7:0	DM5	W/R	-	data mask 5configuration
6Eh	7:0	DM6	W/R	-	data mask 6 configuration
6Fh	7:0	DM7	W/R	-	data mask 7 configuration

DLC > 8	DM0	DM1	DM2	DM3	DM4	DM5	DM6	DM7
DLC = 8	DM0	DM1	DM2	DM3	DM4	DM5	DM6	DM7
DLC = 7		DM1	DM2	DM3	DM4	DM5	DM6	DM7
DLC = 6			DM2	DM3	DM4	DM5	DM6	DM7
DLC = 5				DM3	DM4	DM5	DM6	DM7
DLC = 4					DM4	DM5	DM6	DM7
DLC = 3						DM5	DM6	DM7
DLC = 2							DM6	DM7
DLC = 1								DM7

Fig 8 Data mask register usage for different values of DLC

FAIL-SAFE FEATURES

TXD dominant time-out

A TXD dominant time-out timer is started when pin TXD is forced LOW while the transceiver is in Active Mode. If pin TXD persists in the low state for longer than the TXD dominant time-out time ($t_{to(dom)TXD}$), the transmitter is disabled and the bus lines is released to recessive state. These features prevent a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD goes HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 15 kbit/s.

A CAN failure interrupt is generated (CF = 1; see Table 16), if enabled (CFE = 1; see Table 19), a CAN failure interrupt will be generated after the TXD dominant time-out time is exceeded. In addition, the status of the TXD dominant time-out can be read by the CFS bit in the transceiver status register (Table 5) and bit CTS is set to 0.

Pull-up on TXD pin

Pin TXD has an internal pull-up towards VIO to ensure that the recessive driver state is safely defined while the pin is left floating.

VCC undervoltage event

Assuming CAN failure detection is enabled (CFE = 1), and status bit VCS is set to 1, a CAN failure event is captured (CF = 1) when CMC = 01 and the supply to the CAN transceiver (V_{CC}) drops below $V_{uvd(VCC)}$,

Loss of power at pin BAT

A loss of power at pin BAT has no effect on the bus lines or on the microcontroller. No reverse currents will flow out of the bus.

Local wake-up via WAKE pin

Local wake-up is enabled via bits WPRE and WPFE in the WAKE pin event capture enable register (see Table 20). A wake-up event is triggered by a LOW-to-HIGH (if WPRE = 1) and/or a HIGH-to-LOW (if WPFE = 1) transition on the WAKE pin. This configuration allows for maximum flexibility when designing a local wake-up circuit. In applications that don’t make use of the local wake-up facility, local wake-up should be disabled and the WAKE pin connected to GND to ensure optimal EMI performance.

Table 11 WAKE status register (address 4Bh)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	
1	WPVS	R		WAKE pin status:
			0	voltage on WAKE pin below switching threshold ($V_{th(sw)}$)
			1	voltage on WAKE pin above switching threshold ($V_{th(sw)}$)

0	reserved	R		

When SIT1145GQ is in normal mode, the voltage state on the WAKE pin can always be read via the WPVS bit. Otherwise, WPVS is only valid when local wake-up is enabled (WPRE = 1 and/or WPFE = 1).

Wake-up and interrupt event diagnosis via pin RXD

Wake-up and interrupt event diagnosis in the SIT1145GQ is designed to provide the microcontroller with information about the status of a range of features and functions. This information is stored in the event status registers (Table 15 to Table 17) and is signaled on pin RXD pin, if enabled.

A distinction is made between regular wake-up events and interrupt events (at least one regular wake-up source must be enabled to allow the SIT1145GQ to switch to Sleep mode).

Table 12 Regular wake-up events

Symbol	Event	Power-on	Description
CW	CAN wake-up	disabled	a CAN wake-up event was detected while the transceiver was in CAN Offline mode.
WPR	rising edge on WAKE pin	disabled	a rising-edge wake-up was detected on pin WAKE.
WPF	falling edge on WAKE pin	disabled	a falling-edge wake-up was detected on pin WAKE.

Table 13 Interrupt events

Symbol	Event	Power-on	Description
PO	power-on	always enabled	The SIT1145GQ has exited Off mode (after battery power has been restored/connected)
OTW	overtemperature warning	disabled	the IC temperature has exceeded the overtemperature warning threshold (only detected in Normal mode)
SPIF	SPI failure	disabled	SPI clock count error (only 16-, 24- and 32-bit commands are valid), illegal MC code or attempted write access to locked register (an SPI failure event will not wake-up the SIT1145GQ from Sleep mode)
PNFDE	PN frame detection error	always enabled	partial networking frame detection error
CBS	CAN bus silence	disabled	no activity on CAN-bus for $t_{o(silence)}$ (detected only when CBSE = 1 while bus active)
CF	CAN failure	disabled	one of the following CAN failure events detected (not is Sleep mode): - CAN transceiver deactivated due to a dominant clamped TXD - CAN transceiver deactivated due to a V_{CC} undervoltage event (if CMC = 01)

PO and PNFDE interrupts are always captured. Wake-up and interrupt detection can be enabled/disabled for the remaining events individually via the event capture enable registers (Table 18 to Table 20).

If an event occurs while the associated event capture function is enabled, the relevant event status bit is set. If the transceiver is in CAN Offline mode, pin RXD is forced LOW to indicate that a wake-up or interrupt event has been detected. If the SIT1145GQ is in Sleep mode when an event (other than a SPIF interrupt) occurs, pin INH is forced HIGH and the SIT1145GQ switches to Standby mode. If the SIT1145GQ is in Standby mode when the event occurs, pin RXD is forced LOW to flag an interrupt/wake-up event. The detection of any enabled wake-up or interrupt event will trigger a wake-up in Standby mode. The detection of any enabled wake-up or interrupt event other than a SPIF interrupt will trigger a wake-up in Sleep mode. The microcontroller can monitor events via the event status registers. An extra status register, the Global event status register (Table 14), is provided to help speed up software polling routines. By polling the Global event status register, the microcontroller can quickly determine the type of event captured (system, transceiver or WAKE) and then query the relevant table (Table 15, Table 16, Table 17).

After the event source has been identified, the status flag should be cleared (set to 0) by writing 1 to the relevant bit (writing 1 will have no effect). A number of status bits can be cleared in a single write operation by writing 1 to all relevant bits. It is strongly recommended to clear only the status bits that were set to 1 when the status registers were last read. This precaution ensures that events triggered just before the write access are not lost.

Interrupt/wake-up delay

If interrupt or wake-up events occur very frequently while the transceiver is in CAN Offline mode, they can have a significant impact on the software processing time (because pin RXD is repeatedly driven LOW, requiring the microcontroller to respond each time an interrupt/wake-up is generated). The SIT1145GQ incorporates an interrupt/wake-up delay timer to limit interference with the software.

When one of the event capture status bits is cleared, pin RXD is released (HIGH) and a timer is started. If further events occur while the timer is running, the relevant status bits are set. If the timer expires after $t_{d(event)}$ with one or more events pending, pin RXD goes LOW again to alert the microcontroller.

In this way, the microcontroller is interrupted once to process multiple events instead of processing individual events multiple times. If all active event capture bits have been cleared (by the microcontroller) when the timer expires after $t_{d(event)}$, pin RXD remains HIGH (because there are no pending events). The event capture registers can be read at any time.

Sleep mode protection

When the SIT1145GQ switches to Sleep mode, it is very important to configure event detection configured correctly to ensure that it will respond to a wake-up event. Therefore, to avoid potential system deadlocks, at least one regular wake-up event must be enabled and all event status bits must be cleared before the SIT1145GQ switches to Sleep mode. Otherwise, the SIT1145GQ will respond to a go-to-sleep command (MC = 001) to switch to Standby mode.

EVENT STATUS AND EVENT CAPTURE REGISTERS

After an event source has been identified, the status flag should be cleared (set to by writing 1 to the relevant status bit (writing 0 will have no effect).

Table 14 Global event status register (address 60h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	
3	WPE	R		WAKE pin event:
			0	no pending WAKE pin event
			1	WAKE pin event pending at address 0x64
2	TRXE	R		transceiver event:
			0	no pending transceiver event
			1	transceiver event pending at address 0x63
1	reserved	R	-	
0	SYSE	R		system event:
			0	no pending system event
			1	system event pending at address 0x61

Table 15 System event status register (address 61h)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	-	
4	PO(1)	R/W		power-on:
			0	no recent battery power-on
			1	the SIT1145GQ has left Off mode after battery power-on
3	reserved	R	-	
2	OTW	R/W		overtemperature warning:
			0	overtemperature not detected
			1	the global chip temperature has exceeded the overtemperature warning threshold ($T_{th(warn)otp}$)
1	SPIF	R/W		SPI failure:
			0	no SPI failure detected
			1	SPI failure detected
0	reserved	R	-	

(1) PO is cleared when the SIT1145GQ is forced to Sleep mode due to an undervoltage event. The information stored in PO could be lost if the transition to Sleep mode was forced by an undervoltage event. Bit NMS, which is set to 0 when the SIT1145GQ switches to Normal mode after power-on, compensates for this.

Table 16 Transceiver event status register (address 63h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R	-	
5	PNFDE	R/W		partial networking frame detection error:
			0	no partial networking frame detection error detected
			1	partial networking frame detection error detected
4	CBS	R/W		CAN-bus status:
			0	CAN-bus active
			1	no activity on CAN-bus for $t_{to(silence)}$
3:2	reserved	R	-	
1	CF [1]	R/W		CAN failure:
			0	no CAN failure detected
			1	CAN failure event detected
0	CW	R/W		CAN wake-up:
			0	no CAN wake-up event detected
			1	CAN wake-up event detected

(1) CF is only enabled in Normal mode while the transceiver is in CAN Active mode and is triggered if TXD is clamped dominant or a VCC undervoltage is detected (when CMC = 01).

Table 17 WAKE pin event status register (address 64h)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	
1	WPR	R/W		WAKE pin rising edge:
			0	no rising edge detected on WAKE pin
			1	rising edge detected on WAKE pin
0	WPF	R/W		WAKE pin falling edge:
			0	no falling edge detected on WAKE pin
			1	falling edge detected on WAKE pin

Table 18 System event capture enable register (address 04h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
1	OTWE	R/W		overtemperature warning enable:
			0	overtemperature warning disabled
			1	overtemperature warning enabled
0	SPIFE	R/W		SPI failure enable:
			0	SPI failure detection disabled
			1	SPI failure detection enabled

Bit	Symbol	Access	Value	Description
0	reserved	R	-	

Table 19 Transceiver event capture enable register (address 23h)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	-	
4	CBSE	R/W		CAN-bus silence enable:
			0	CAN-bus silence detection disabled
			1	CAN-bus silence detection enabled
3:2	reserved	R	-	
1	CFE	R/W		CAN failure enable:
			0	CAN failure detection disabled
			1	CAN failure detection enabled
0	CWE	R/W		CAN wake-up enable:
			0	CAN wake-up detection disabled
			1	CAN wake-up detection enabled

Table 20 WAKE pin event capture enable register (address 4Ch)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	
1	WPRE	R/W		WAKE pin rising-edge enable:
			0	rising-edge detection on WAKE pin disabled
			1	rising-edge detection on WAKE pin enabled
0	WPFE	R/W		WAKE pin falling-edge enable:
			0	falling-edge detection on WAKE pin disabled
			1	falling-edge detection on WAKE pin enabled

DEVICE ID

A byte is reserved at address 0x7E for a SIT1145GQ identification code.

Table 21 Identification register (address 7Eh)

Bit	Symbol	Access	Value	Description
7:0	IDS [7:0]	R		device identification code
			74h	SIT1145GQ/FD

LOCK CONTROL REGISTER

Sections of the register address area can be write-protected to protect against unintended modifications. Note that this facility only protects locked bits from being modified via the SPI and will not prevent the SIT1145GQ updating status registers etc.

Table 22 Lock control register (address 0Ah)

Bit	Symbol	Access	Value	Description
7	reserved	R	-	cleared for future use
6	LK6C	R/W		lock control 6: address area 0x68 to 0x6F - partial networking data byte registers
			0	SPI write-access enabled
			1	SPI write-access disabled
5	LK5C	R/W		lock control 5: address area 0x50 to 0x5F
			0	SPI write-access enabled
			1	SPI write-access disabled
4	LK4C	R/W		lock control 4: address area 0x40 to 0x4F - WAKE pin configuration
			0	SPI write-access enabled
			1	SPI write-access disabled
3	LK3C	R/W		lock control 3: address area 0x30 to 0x3F
			0	SPI write-access enabled
			1	SPI write-access disabled
2	LK2C	R/W		lock control 2: address area 0x20 to 0x2F - transceiver control and partial networking
			0	SPI write-access enabled
			1	SPI write-access disabled
1	LK1C	R/W		lock control 1: address area 0x10 to 0x1F
			0	SPI write-access enabled
			1	SPI write-access disabled
0	LK0C	R/W		lock control 0: address area 0x06 to 0x09 - general purpose memory
			0	SPI write-access enabled
			1	SPI write-access disabled

GENERAL-PURPOSE MEMORY

SIT1145GQ allocates 4 bytes of memory for general-purpose registers used to store user information. The general purpose registers can be accessed through the SPI at address 0x06 to 0x09 (see Table 23）.

VIO SUPPLY PIN

The VIO pin should be connected to the microcontroller supply voltage, which will allow the signal levels of the TXD, RXD and the SPI interface pins to be adjusted to the I/O levels of the microcontroller, enabling direct interfacing without the need for glue logic.

VCC/VIO UNDERVOLTAGE PROTECTION

If an undervoltage is detected on pins VCC or VIO, and it remains valid for longer than the undervoltage detection delay time, $t_{d(uvd)}$, the SIT1145GQ is forced to Sleep mode (see Fig 3). A number of preventative measures are taken when the SIT1145GQ is forced to Sleep mode to avoid deadlock and unpredictable states:

- Before SIT1145GQ switches to sleep mode, all previously captured events (address range 0x61 to 0x64) are cleared to avoid repeated wake attempts during undervoltage.
- Enable CAN WAKE up (CWE=1) and local wake up via the WAKE pin (WPFE=WPRE=1) to avoid deadlock situations where SIT1145GQ cannot be woken up after entering sleep mode.
- After SIT1145GQ recovers from the undervoltage event, Partial Networking (CPNC=0) is disabled to ensure immediate wake up in response to bus traffic.
- The Partial Networking Configuration bit is cleared (CPNOK = 0) to indicate that partial networking might not have been configured correctly when the SIT1145GQ switched to Sleep mode.

When SIT1145GQ is forced to Sleep mode due to an undervoltage event, the status bit FSMS is set to 1 (see Table 3). If an undervoltage event forces a conversion to sleep mode (FSMS = 1) after SIT1145GQ wakes up from Sleep mode, this bit can be sampled to readjust the settings for CWE, WPFE, WPRE, and CPNC.

SPI

The Serial Peripheral Interface (SPI) provides the communication link with the microcontroller, supporting multi-slave operations. The SPI is configured for full-duplex data transfer, so it returns status information when new control data is shifted in. The interface also provides a read-only access option, allows read-back registers to be applied without changing their contents.

The SPI uses four interface signals for synchronization and data transfer:

- SCSN: SPI chip select input; active LOW; default level is HIGH (pull-up)
- SCK: SPI clock; default level is LOW due to internal pull-down
- SDI: SPI data input
- SDO: SPI data output; floating when pin SCSN is HIGH (may need external pull-up or pull-down if not available in the host controller)

Bit sampling is performed on the falling edge of the clock and data is shifted in/out on the rising edge, as illustrated in Fig 9.

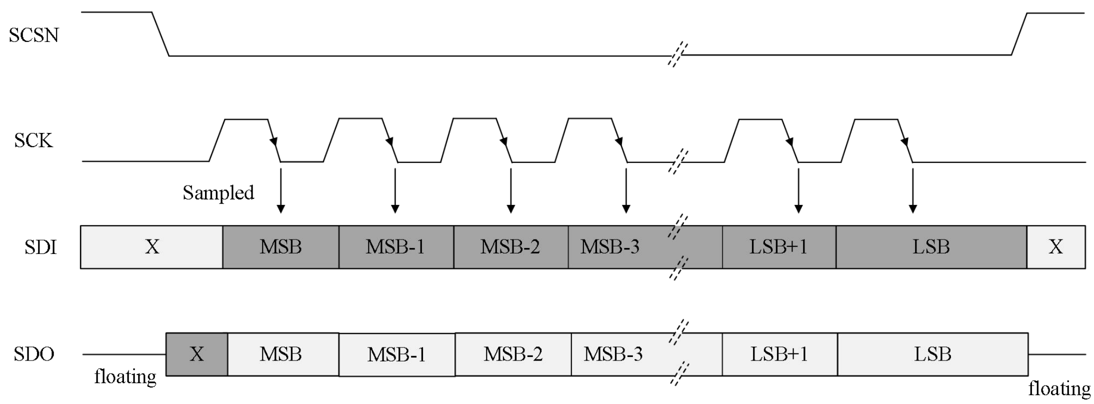


Fig 9 SPI timing protocol

The SPI data in the SIT1145GQ is stored in a number of dedicated 8-bit registers. Each register is assigned a unique 7-bit address. Two bytes (16 bits) must be transmitted to the SIT1145GQ for a single register read or write operation. The first byte contains the 7-bit address along with a “read-only” bit (the LSB). The read-only bit must be 0 to indicate a write operation (if this bit is 1, a read operation is assumed and any data on the SDI pin is ignored). The second byte contains the data to be written to the register.

24- and 32-bit read and write operations are also supported. The register address is automatically incremented, once for a 24-bit operation and twice for a 32-bit operation, as illustrated in Fig 10.

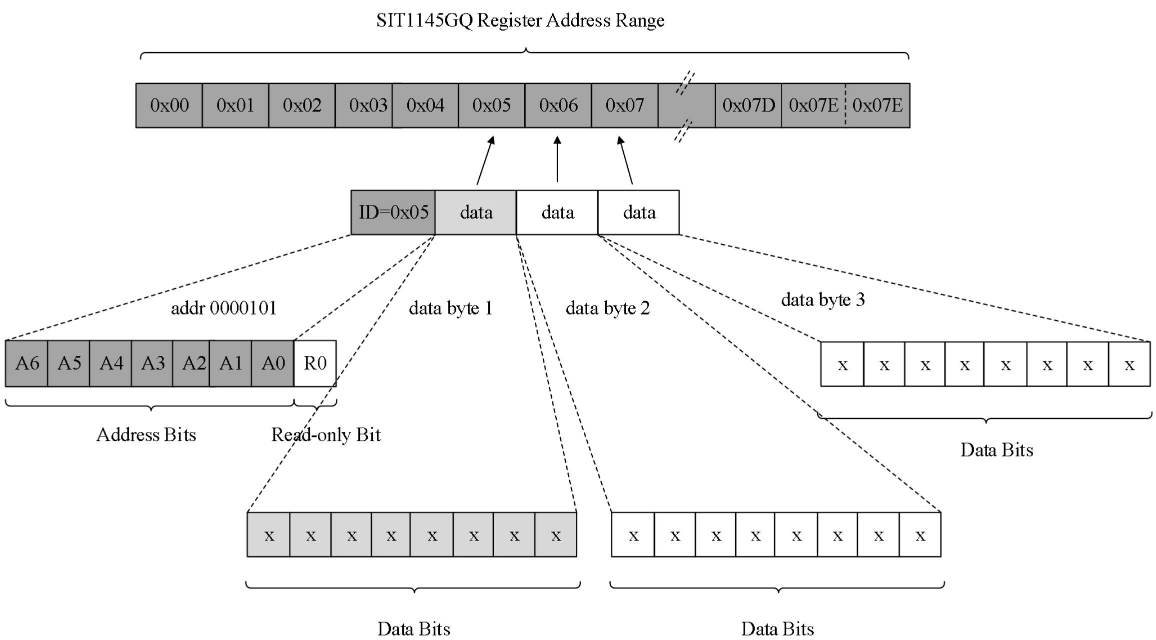


Fig 10 SPI data structure for a write operation (16-, 24- or 32-bit)

During an SPI data read or write operation, the contents of the addressed register(s) is returned via pin SDO. The SIT1145GQ tolerates attempts to write to registers that don't exist. If the available address space is exceeded during a write operation, the data above the valid address range is ignored (without generating an SPI failure event).

During a write operation, the SIT1145GQ monitors the number of SPI bits transmitted. If the number recorded is not 16, 24 or 32, then the write operation is aborted and an SPI failure event is captured (SPIF = 1).

If more than 32 bits are clocked in on pin SDI during a read operation, the data stream on SDI is reflected on SDO from bit 33 onwards.

REGISTER MAP

The addressable register space contains 128 registers with addresses from 0x00 to 0x7F. An overview of the register mapping is provided in Table 23 to Table 27. The functionality of the individual bits is discussed in more detail in relevant sections of the data sheet.

Table 23 Overview of primary control registers

Address	Register Name	Bit: 7	6	5	4	3	2	1	0
0x01	Mode control	reserved					MC		
0x03	Main status	FSMS	OTWS	NMS	reserved				
0x04	System event enable	reserved					OTWE	SPIFE	reserved
0x06	Memory 0	GPM [7:0]							
0x07	Memory 1	GPM [15:8]							
0x08	Memory 2	GPM [23:16]							
0x09	Memory 3	GPM [31:24]							
0x0A	Lock control	reserved	LK6C	LK5C	LK4C	LK3C	LK2C	LK1C	LK0C

Table 24 Overview of transceiver control and partial networking registers

Address	Register Name	Bit: 7	6	5	4	3	2	1	0
0x20	CAN control	reserved	CFDC	PNCOK	CPNC	reserved		CMC	
0x22	Transceiver status	CTS	CPNERR	CPNS	COSCS	CBSS	reserved	VCS	CFS
0x23	Transceiver event enable	reserved			CBSE	reserved		CFE	CWE
0x26	Data rate	reserved					CDR		
0x27	Identifier 0	ID [7:0]							
0x28	Identifier 1	ID [15:8]							
0x29	Identifier 2	ID [23:16]							
0x2A	Identifier 3	reserved			ID [28:24]				
0x2B	Mask 0	M [7:0]							

Address	Register Name	Bit: 7	6	5	4	3	2	1	0
0x2C	Mask 1	M [15:8]							
0x2D	Mask 2	M [23:16]							
0x2E	Mask 3	reserved			M [28:24]				
0x2F	Frame control	IDE	PNDM	reserved		DLC			
0x68	Data mask 0	DM0[7:0]							
0x69	Data mask 1	DM1[7:0]							
0x6A	Data mask 2	DM2[7:0]							
0x6B	Data mask 3	DM3[7:0]							
0x6C	Data mask 4	DM4[7:0]							
0x6D	Data mask 5	DM5[7:0]							
0x6E	Data mask 6	DM6[7:0]							
0x6F	Data mask 7	DM7[7:0]							

Table 25 Overview of WAKE pin control and status registers

Address	Register Name	Bit: 7	6	5	4	3	2	1	0
0x4B	WAKE pin status	reserved						WPVS	reserved
0x4C	WAKE pin enable	reserved						WPRE	WPFE

Table 26 Overview of Event Capture registers

Address	Register Name	Bit: 7	6	5	4	3	2	1	0
0x60	Event capture status	reserved				WPE	TRXE	reserved	SYSE
0x61	System event status	reserved			PO	reserved	OTW	SPIF	reserved
0x63	Transceiver event status	reserved		PNFDE	CBS	reserved		CF	CW
0x64	WAKE pin event status	reserved						WPR	WPF

Table 27 Overview of Identification register

Address	Register Name	Bit: 7	6	5	4	3	2	1	0
0x7E	Identification	IDS [7:0]							

REGISTER CONFIGURATION

A number of register bits may change state automatically when the SIT1145GQ switches from one operating mode to another. This is particularly evident when the SIT1145GQ switches to Off mode or when an undervoltage event forces a transition to Sleep mode. These changes are summarized in Table 28. If an SPI transmission is in progress when the SIT1145GQ changes state, the transmission is ignored (automatic state changes have priority).

Table 28 Register bit settings in SIT1145GQ operating modes

Symbol	Off (reset values)	Standby	Normal	Sleep	Overtemp	Forced Sleep
CBS	0	no change	no change	no change	no change	0
CBSE	0	no change	no change	no change	no change	no change
CBSS	1	actual state	actual state	actual state	actual state	actual state
CDR	101	no change	no change	no change	no change	no change
CF	0	no change	no change	no change	no change	0
CFDC	0	no change	no change	no change	no change	no change
CFE	0	no change	no change	no change	no change	no change
CFS	0	actual state	actual state	actual state	actual state	actual state
CMC	01	no change	no change	no change	no change	no change
COSCS	0	actual state	actual state	actual state	actual state	actual state
CPNC	0	no change	no change	no change	no change	0
CPNERR	1	actual state	actual state	actual state	actual state	actual state
CPNS	0	actual state	actual state	actual state	actual state	actual state
CTS	0	0	actual state	0	0	0
CW	0	no change	no change	no change	no change	0
CWE	0	no change	no change	no change	no change	1
DMn	11111111	no change	no change	no change	no change	no change
DLC	0000	no change	no change	no change	no change	no change
FSMS	0	no change	no change	0	no change	1
GPMn	00000000	no change	no change	no change	no change	no change
IDn	00000000	no change	no change	no change	no change	no change
IDE	0	no change	no change	no change	no change	no change
IDS	01110100	no change	no change	no change	no change	no change
LKnC	0	no change	no change	no change	no change	no change
Mn	00000000	no change	no change	no change	no change	no change
MC	100	100	111	001	don't care	001

Symbol	Off (reset values)	Standby	Normal	Sleep	Overtemp	Forced Sleep
NMS	1	no change	0	no change	no change	no change
OTW	0	no change	no change	no change	no change	0
OTWE	0	no change	no change	no change	no change	no change
OTWS	0	actual state	actual state	actual state	actual state	actual state
PNCOK	0	no change	no change	no change	no change	0
PNDM	1	no change	no change	no change	no change	no change
PNFDE	0	no change	no change	no change	no change	0
PO	1	no change	no change	no change	no change	0
SPIF	0	no change	no change	no change	no change	0
SPIFE	0	no change	no change	no change	no change	no change
SYSE	1	no change	no change	no change	no change	0
TRXE	0	no change	no change	no change	no change	0
VCS	0	actual state	actual state	actual state	actual state	actual state
WPE	0	no change	no change	no change	no change	0
WPF	0	no change	no change	no change	no change	0
WPFE	0	no change	no change	no change	no change	1
WPR	0	no change	no change	no change	no change	0
WPRE	0	no change	no change	no change	no change	1
WPVS	0	no change	no change	no change	no change	no change

STATIC CHARACTERISTICS

T_j = -40°C to 150°C; V_{BAT} = 4.5V to 28V; VCC = 4.5V to 5.5V; VIO = 1.7V to 5.5V; R_L = 60Ω; all voltages are defined with respect to ground; positive currents flow into the IC; unless otherwise specified, typical values are given at T_A=25°C, V_{BAT} = 13V.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply						
battery supply current	I_{BAT}	Normal mode; MC = 111	-	-	1.2	mA
		Sleep mode; MC = 001; CWE = 1; CAN Offline mode; V_{BAT} = 7V to18V		30	50	μA
		Standby mode; MC =100; CWE= 1; CAN Offline mode; V_{BAT} = 7V to 18V		36	60	μA
		additional current in CAN Offline Bias mode;	-	-	200	μA
		Standby or Sleep mode; additional current in CAN Offline Bias mode with active partial networking decoder; (1)	-	0.4	0.6	mA
		additional current from WAKE input; WPRE = WPFE = 1;	-	2	3	μA
Power-on detection threshold voltage on BAT pin	$V_{th(det)pon}$	V_{BAT} rising	4.0	-	4.5	V
Power-off detection threshold voltage on BAT pin	$V_{th(det)poff}$	V_{BAT} falling	2.8	-	3.3	V
CAN undervoltage recovery voltage on BAT pin	$V_{uvr(CAN)}$	V_{BAT} rising	4.5	-	5	V
CAN undervoltage voltage on BAT pin	$V_{uvd(CAN)}$	V_{BAT} falling	4.0	-	4.5	V
Supply current on VCC pin	I_{CC}	CAN Active mode; CAN recessive; V_{TXD} = V_{IO}	-	5	10	mA
		CAN Active mode; CAN dominant; V_{TXD} = 0V	-	45	65	mA
		Standby/Normal mode; CAN inactive;	-	0.4	8.5	μA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
		Sleep mode; CAN inactive;	-	0.3	7	μA
		Short circuit on bus lines; CAN dominant; V_{TXD} = 0V; -3V<(V_{CANH}=V_{CANL}) <+18V	-	55	110	mA
Undervoltage detection voltage on pin VCC	$V_{uxd(VCC)}$	V_{BAT}>4.5V	4.0	-	4.5	V
Supply current on pin VIO	I_{IO}	Standby/Normal mode;	-	0.3	11	μA
		Sleep mode	-	0.2	8	μA
Undervoltage detection voltage on pin VIO	$V_{uvd(VIO)}$	V_{BAT}>4.5V	1.5	-	1.7	V
Pin TXD						
Switching threshold voltage	$V_{th(sw)}$	VIO = 1.7V to 5.5V	$0.25V_{IO}$	-	$0.75V_{IO}$	V
Switching threshold voltage hysteresis	$V_{th(sw)hys}$	VIO = 1.7V to 5.5V	$0.05V_{IO}$	-	-	V
Pull-up resistance	R_{pu}	VIO = 2.8V to 5.5V	40	60	80	kΩ
Unpowered leakage current	$I_{LKG(OFF)}$	TXD = 5.5 V, VCC = VIO = 0 V	-2		2	μA
Pin RXD						
HIGH-level output current	I_{OH}	V_{RXD}= VIO-0.4V	-10	-	-1	mA
LOW-level output current	I_{OL}	V_{RXD} = 0.4V	1	-	10	mA
Pull-up resistance	R_{pu}	CAN Offline mode	40	60	80	kΩ
Unpowered leakage current	$I_{LKG(OFF)}$	RXD = 5.5 V, VCC = VIO = 0 V	-2		2	μA
Pins SDI，SCK，SCSN						
Switching threshold voltage	$V_{th(sw)}$	VIO = 1.7V to 5.5V	$0.25V_{IO}$	-	$0.75V_{IO}$	V
Switching threshold voltage hysteresis	$V_{th(sw)hys}$	VIO = 1.7V to 5.5V	$0.05V_{IO}$	-	-	V
Pull-down resistance on pin SCK	$R_{pd(SCK)}$	VIO = 2.8V to 5.5V	40	60	80	kΩ
Pull-up resistance on pin SCK	$R_{pu(SCSN)}$	VIO = 2.8V to 5.5V	40	60	80	kΩ
Pull-down resistance on pin SDI	$R_{pd(SDI)}$	VIO = 2.8V to 5.5V	40	60	80	kΩ
Pull-up resistance on pin SDI	$R_{pu(SDI)}$	VIO = 2.8V to 5.5V	40	60	80	kΩ

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Unpowered leakage current	$I_{LKG(OFF)}$	SDI=SCK=SCSN = 5.5 V, VCC = VIO = 0 V	-2		2	μA
Pin SDO						
HIGH-level output current	V_{OH}	V_{SDO}= VIO-0.4V	-10	-	-1	mA
LOW-level output current	I_{OL}	V_{SDO} = 0.4V	1	-	10	mA
Off-state output leakage current	$I_{LO(off)}$	$V_{SCSN} = V_{IO}$; V_O = 0V to V_{IO}	-2	-	+2	μA
Pin INH						
Output voltage	V_O	I_{INH} = -180μA	V_{BAT}-0.8	-	V_{BAT}	V
Pull-down resistance	R_{pd}	Sleep mode	2	5	10	MΩ
Pin WAKE						
Rising switching threshold voltage	$V_{th(sw)r}$		2.8	-	4.1	V
falling switching threshold voltage	$V_{th(sw)f}$		2.4	-	3.75	V
Input hysteresis voltage	$V_{hys(i)}$		250	-	800	V
Input current	I_i		-	-	+1.5	μA
Temperature protection						
Overtemperature protection activation threshold temperature	$T_{th(act)otp}$	(1)	165	180	190	℃
Overtemperature protection release threshold temperature	$T_{th(rel)otp}$	(1)	128	135	152	℃
Overtemperature protection warning threshold temperature	$T_{th(warn)otp}$	(1)	128	135	152	℃
Pins CANH and CANL						
Dominant output voltage on pin CANH	$V_{OH(Dom)}$	CAN Active mode; V_{TXD} = 0V, R_L= 50Ω to 65Ω	2.75	3.5	4.5	V
Recessive output voltage on pin CANL	$V_{OL(Dom)}$	CAN Active mode; V_{TXD} = 0V, R_L= 50Ω to 65Ω	0.5	1.5	2.25	V
Dominant differential output voltage	$V_{OD(Dom)}$	CAN Active mode (dominant); V_{TXD} = 0V; $t < t_{to(dom)TXD}$;				
		RL= 50Ω to 65Ω	1.5	-	3	V
		RL= 45Ω to 70Ω	1.4		3.3	V

Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
		$R_L = 2240\Omega$	1.5	-	5	V
Recessive output voltage	$V_{O(Rec)}$	CAN Active mode; $V_{TXD} = V_{IO}$; $R_L = 60\Omega$	2.2	2.5	2.8	V
		CAN Offline mode; R_L = no load	-0.1	-	+0.1	V
		CAN Offline Bias/ Listen-only mode; R_L = no load; $V_{CC} = 0V$	2	2.5	3	V
Recessive differential output voltage	$V_{OD(Rec)}$	CAN Active mode; $V_{TXD} = V_{IO}$; $R_L = 60\Omega$	-500	-	50	mV
		CAN Offline mode; R_L = no load	-0.2	-	0.2	V
		CAN Offline Bias/ Listen-only mode; R_L = no load; $V_{CC} = 0V$	-500	-	50	mV
Transmitter dominant voltage symmetry	$V_{dom(TX)sym}$	$V_{dom(TX)sym} = V_{CC} - V_{CANH} - V_{CANL}$	-400	-	400	mV
Transmitter voltage symmetry	V_{TXsym}	$V_{TXsym} = V_{CANH} + V_{CANL}$; (1) $C_{SPLIT} = 4.7nF$; f_{TXD} = 250kHz, 1MHz or 2.5MHz (2)	$0.9V_{CC}$	-	$1.1V_{CC}$	V
Dominant short-circuit output current	$I_{O(sc)dom}$	CAN Active mode; $V_{TXD} = 0V$; $V_{CC} = 5V$				
		Pin CANH; V_{CANH} = -15V to +27V	-100	-	+100	mA
		Pin CANL; V_{CANL} = -15V to +27V	-100	-	+100	mA
Recessive short-circuit output current	$I_{O(sc)rec}$	$V_{CANH} = V_{CANL}$ = -27V to 32V; $V_{TXD} = V_{IO}$	-5	-	5	mA
Bus receiver static characteristics						
Differential receiver threshold voltage	$V_{th(RX)dif}$	CAN Active/Listen-only modes $-30V \leq V_{CAN} \leq +30V$	0.5	0.7	0.9	V
		CAN Offline mode $-12V \leq V_{CAN} \leq +12V$	0.4	0.7	1.15	V
Differential receiver hysteresis voltage	$V_{hys(RX)dif}$	CAN Active/Listen-only modes; $-30V \leq V_{CANL} \leq +30$		60		mV
Receiver recessive voltage	$V_{rec(RX)}$	CAN Active/Listen-only modes $-30V \leq V_{CANL} \leq +30$	-4 (1)	-	0.5	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
		CAN Offline mode $-12V \le V_{CANL} \le +12V$	-4 (1)	-	0.4	V
Receiver dominant voltage	$V_{dom(RX)}$	CAN Active/Listen-only modes $-30V \le V_{CANL} \le +30$	0.9	-	9.0 (1)	V
		CAN Offline mode $-12V \le V_{CANL} \le +12V$	1.15	-	9.0 (1)	V
Leakage current	I_L	$V_{CC} = V_{BAT} = 0V$ or $V_{CC} = V_{BAT} =$ shorted to ground via 47 kΩ; $V_{CANH} = V_{CANL} = 5V$	-10	-	10	μA
Input resistance	R_i	$-2V \le CANH \le 7V$; $-2V \le CANL \le 7V$;	25	40	50	kΩ
Differential input resistance	$R_{i(diff)}$	$-2V \le CANH \le 7V$; $-2V \le CANL \le 7V$;	50	80	100	kΩ
Input resistance deviation	$\triangle R_i$	$0V \le CANH \le 5V$; $0V \le CANL \le 5V$	-3	-	+3	%
Common-mode input capacitance	$C_{i(cm)}$	(1)	-	-	40	pF
Differential input capacitance	C_{ID}	(1)	-	-	20	pF

(1) Not tested in production; guaranteed by design;

(2) The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Fig 15.

DYNAMIC CHARACTERISTICS

T_j = -40°C to 150°C; V_{BAT} = 4.5V to 40V; VCC = 4.5V to 5.5V; VIO = 1.7V to 5.5V; R_L= 60Ω; all voltages are defined with respect to ground; positive currents flow into the IC; unless otherwise specified, typical values are given at T_A=25°C, V_{BAT} = 13V.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Voltage source; pins BAT, VCC, VIO						
Start-up time	$t_{startup}$	From V_{BAT} exceeding the power-on detection threshold until INH active	-	2.8	4.7	ms
Undervoltage detection delay time	$t_{d(uvd)}$		6	-	54	µs
Delay time from undervoltage detection to sleep mode	$t_{d(uvd-sleep)}$	From undervoltage detection on VCC and/or VIO until SIT1145GQ forced to Sleep mode	150	-	440	ms
Serial peripheral interface timing; pins SCSN, SCK, SDI and SDO; see Fig 13						
Clock cycle time	$t_{cy(clk)}$	Normal/Standby mode	250	-	-	ns
		Sleep mode;	250	-	-	ns
SPI enable lead time	$t_{SPILEAD}$	Normal/Standby modes	50	-	-	ns
		Sleep mode;	50	-	-	ns
SPI enable lag time	t_{SPILAG}	Normal/Standby modes	50	-	-	ns
		Sleep mode;	50	-	-	ns
Clock HIGH time	$t_{clk(H)}$	Normal/Standby modes	100	-	-	ns
		Sleep mode;	100	-	-	ns
Clock LOW time	$t_{clk(L)}$	Normal/Standby modes	100	-	-	ns
		Sleep mode;	100	-	-	ns
Data input set-up time	$t_{su(D)}$	Normal/Standby modes	50	-	-	ns
		Sleep mode;	50	-	-	ns
Data input hold time	$t_{h(D)}$	Normal/Standby modes	50	-	-	ns
		Sleep mode;	50	-	-	ns
Data output valid time	$t_{v(Q)}$	Normal/Standby mode; Pin SDO; C_L = 20pF	-	-	50	ns
		Sleep mode; Pin SDO; C_L = 20pF;	-	-	50	ns
SDI to SDO delay time	$t_{d(SDI-SDO)}$	SPI address bits and read-only bit; C_L = 20pF	-	-	50	ns

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Chip select pulse width HIGH	$t_{WH(S)}$	Pin SCSN	2	-	-	µs
Delay time from SCK LOW to SCSN LOW	$t_{d(SCKL\text{-}SCSNL)}$		50	-	-	ns
CAN transceiver timing: pins CANH, CANL, TXD and RXD						
Delay time from TXD to bus dominant	$t_{d(TXD\text{-}busdom)}$	Fig 11, Fig 14	-	-	80	ns
Delay time from TXD to bus recessive	$t_{d(TXD\text{-}busrec)}$	Fig 11, Fig 14	-	-	80	ns
Differential output signal rise time	$t_{r(BUS)}$	Fig 11, Fig 14	20	30	50	ns
Differential output signal fall time	$t_{f(BUS)}$	Fig 11, Fig 14	20	30	50	ns
Delay time from bus dominant to RXD	$t_{d(busdom\text{-}RXD)}$	Fig 11, Fig 14	-	-	110	ns
Delay time from bus recessive to RXD	$t_{d(busrec\text{-}RXD)}$	Fig 11, Fig 14	-	-	110	ns
RXD output signal rise time (1)	$t_{r(RXD)}$	Fig 11, Fig 14	-	8	-	ns
RXD output signal fall time	$t_{f(RXD)}$	Fig 11, Fig 14	-	8	-	ns
Delay time from TXD LOW to RXD LOW	$t_{d(TXDL\text{-}RXDL)}$	$t_{bit(TXD)}$ = 200ns Fig 12, Fig 14	40	-	190	ns
Delay time from TXD HIGH to HIGH LOW	$t_{d(TXDH\text{-}RXDH)}$	$t_{bit(TXD)}$ = 200ns Fig 12, Fig 14	40	-	190	ns
Transmitted recessive bit width	$t_{bit(bus)}$	$t_{bit(TXD)}$ = 500ns Fig 12, Fig 14	455	-	510	ns
		$t_{bit(TXD)}$ = 200ns Fig 12, Fig 14	155	-	210	ns
Bit time on pin RXD	$t_{bit(RXD)}$	$t_{bit(TXD)}$ = 500ns	420	-	520	ns
		$t_{bit(TXD)}$ = 200ns	120	-	220	ns
Bus dominant wake-up time	$t_{wake(busdom)}$	CAN Offline mode	0.5	-	1.8	µs
Bus recessive wake-up time	$t_{wake(busrec)}$	CAN Offline mode	0.5	-	1.8	µs
Bus wake-up time-out time	$t_{to(wake)bus}$	Between first and second dominant pulses; CAN Offline mode	0.8	-	9	ms
TXD dominant time-out	$t_{to(dom)TXD}$	CAN Active mode;	2.4	-	3.6	ms

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
time		V_{TXD} =0V				
Bus silence time-out time	$t_{to(silence)}$	Recessive time measurement started in all CAN modes	0.8	-	1.2	s
Delay time from bus active to bias	$t_{d(busact-bias)}$		-	-	200	μs
CAN start-up time	$t_{startup(CAN)}$	When switching to Active mode (CTS = 1)	-	-	220	μs
CAN FD timing characteristics according to ISO 11898-2:2024 parameter set B ($t_{bit(TXD)} \geq$ 200 ns, up to 5 Mbit/s); see Fig 12						
transmitted recessive bit width deviation	$\Delta t_{bit(BUS)}$	$\Delta t_{bit(BUS)}=t_{bit(BUS)}-t_{bit(TXD)}$	-45	-	10	ns
receiver timing symmetry	Δ trec	$\Delta t_{rec}=t_{bit(RXD)}-t_{bit(BUS)}$	-45	-	+15	ns
received recessive bit width deviation	$\Delta t_{bit(RXD)}$	$\Delta t_{bit(RXD)}=t_{bit(RXD)}-t_{bit(TXD)}$	-80	-	20	ns
CAN FD timing characteristics according to ISO 11898-2:2024 parameter set C ($t_{bit(TXD)} \geq$ 125 ns, up to 8 Mbit/s); see Fig 12						
transmitted recessive bit width deviation (1)	$\Delta t_{bit(BUS)}$	$\Delta t_{bit(BUS)}=t_{bit(BUS)}-t_{bit(TXD)}$	-10	-	10	ns
receiver timing symmetry (1)	Δ trec	$\Delta t_{rec}=t_{bit(RXD)}-t_{bit(BUS)}$	-20	-	+15	ns
received recessive bit width deviation (1)	$\Delta t_{bit(RXD)}$	$\Delta t_{bit(RXD)}=t_{bit(RXD)}-t_{bit(TXD)}$	-30	-	20	ns
CAN partial networking						
Number of idle bits	$N_{bit(idle)}$	Before a new SOF is accepted; (1) CFDC = 1	6	-	10	-
Dominant bit filter time	$t_{fltr(bit)dom}$	Arbitration data rate ≤ 500 kbit/s; (1) CFDC = 1 (2)	5	-	17.5	%
Pin RXD: interrupt/wake-up event timing (valid in CAN Offline mode only)						
Event capture delay time	$t_{d(event)}$	CAN Offline mode	0.9	-	1.1	ms
Blanking time	t_{blank}	When switching from Offline to Active/Listen-only mode	-	-	25	μs
Pin WAKE						
Wake-up time	t_{wake}		50	-	-	μs
Pin INH						
Delay time from bus wake-up to INH HIGH	$t_{d(buswake-INHH)}$		-	-	100	μs

(1) Not tested in production; guaranteed by design.

(2) Up to 2Mbit/s data speed.

TIMING WAVEFORM

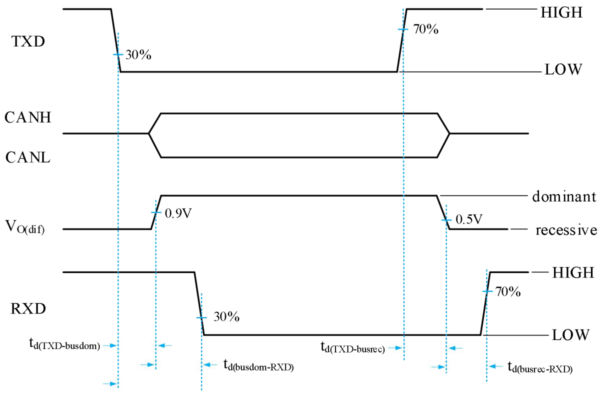


Fig 11 CAN transceiver timing diagram

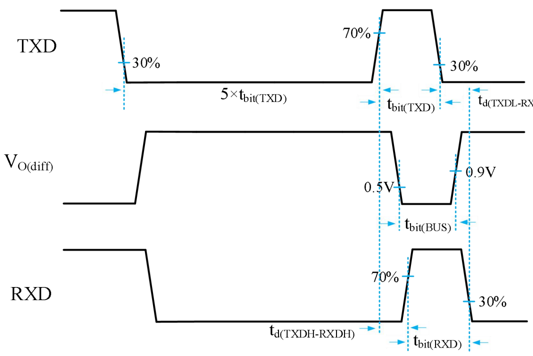
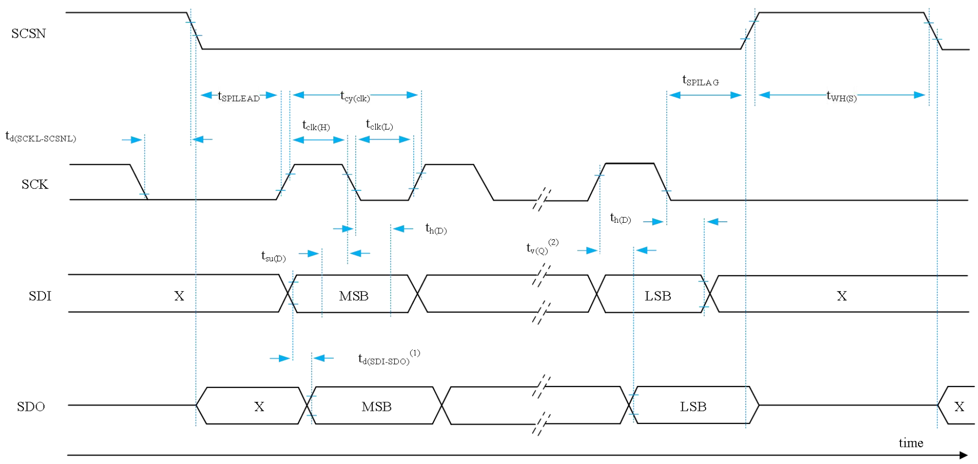


Fig 12 CAN FD timing definitions according to ISO 11898-2:2024



(1) The SDI to SDO delay time is valid for SPI address bits and the read-only bit.
(2) The data output valid time is valid for the SPI data bits

Fig 13 SPI timing diagram

TEST INFORMATION

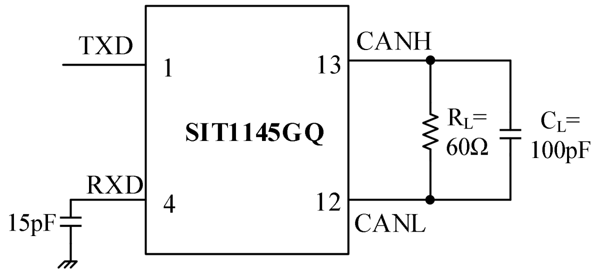


Fig 14 Timing test circuit for CAN transceiver

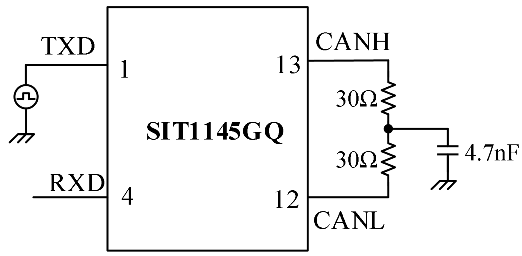


Fig 15 Test circuit for measuring transceiver driver symmetry

TYPICAL APPLICATION

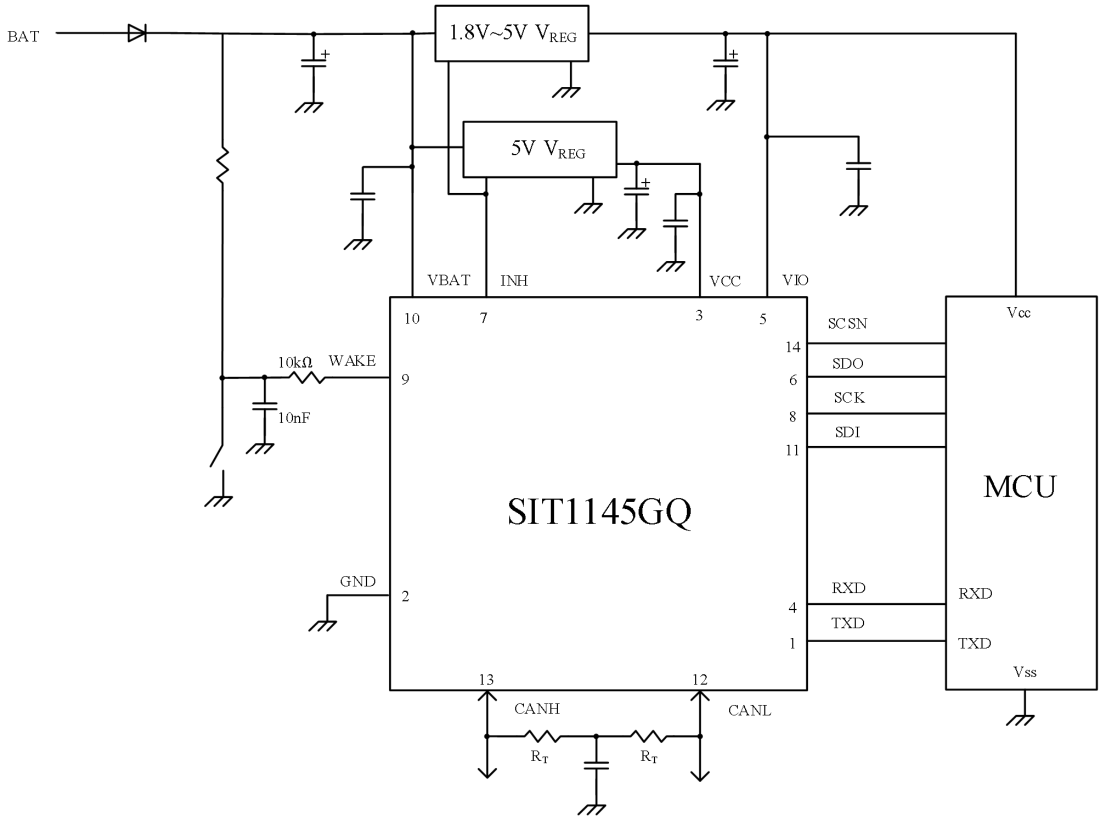


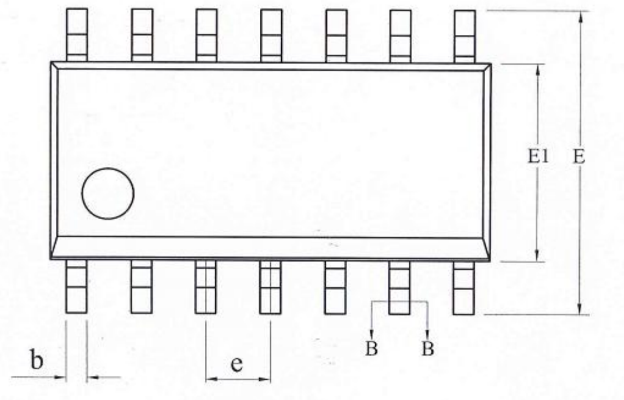
Fig 16 Typical application of the SIT1145GQ

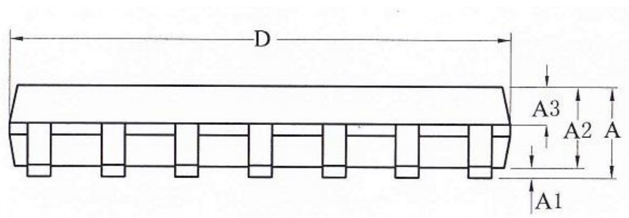
Note: It is recommended to use R_T as a termination resistor with a value of 60Ω. If not used for termination, a value of 1.3kΩ is suggested.

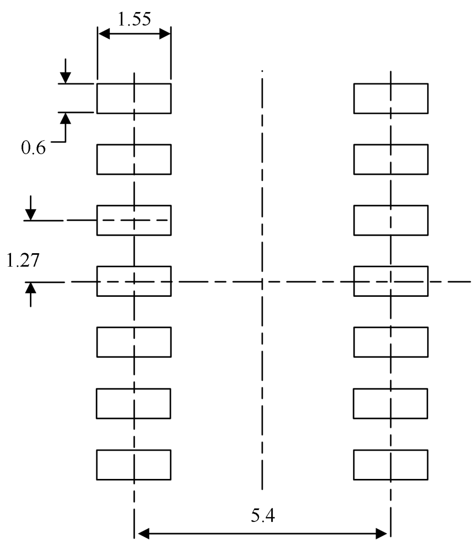
SOP14 DIMENSIONS

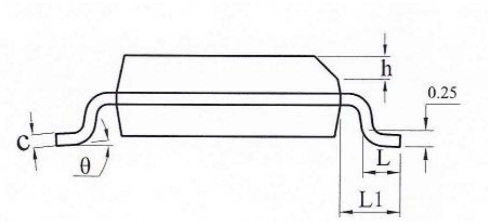
PACKAGE SIZE

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.05	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°







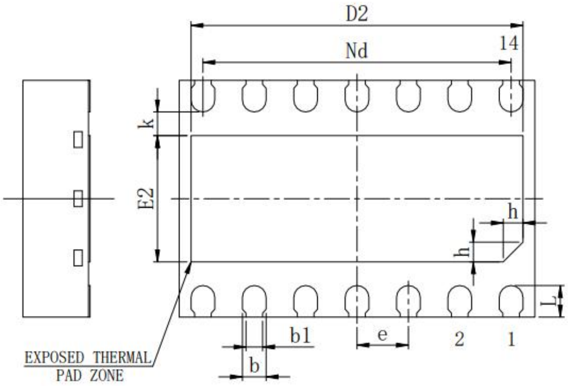


LAND PATTERN EXAMPLE (Unit: mm)

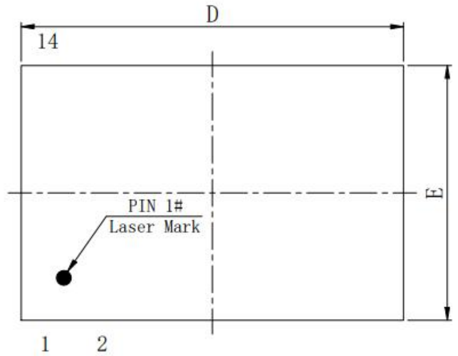
DFN4.5×3-14 DIMENSIONS

PACKAGE SIZE

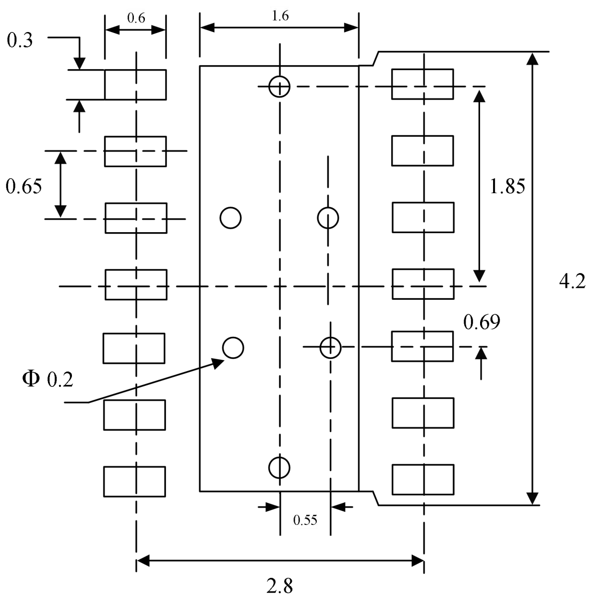
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.25	0.30	0.35
b1	0.21REF		
c	0.203REF		
D	4.40	4.50	4.60
D2	4.10	4.20	4.30
e	0.65BSC		
Nd	3.90BSC		
E	2.90	3.00	3.10
E2	1.50	1.60	1.70
L	0.35	0.40	0.45
h	0.20	0.25	0.30
K	0.30REF		

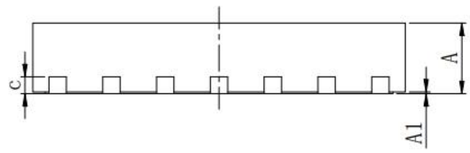


BOTTOM VIEW



TOP VIEW

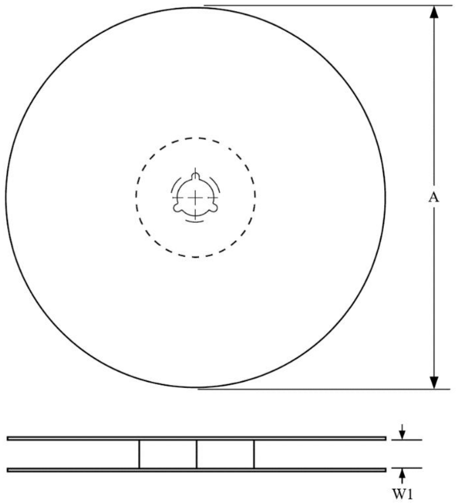




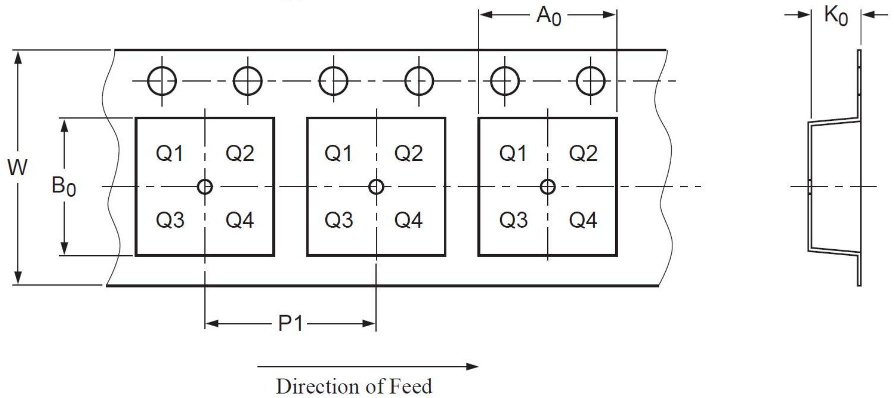
SIDE VIEW

LAND PATTERN EXAMPLE (Unit: mm)

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



PIN1 is in quadrant 1

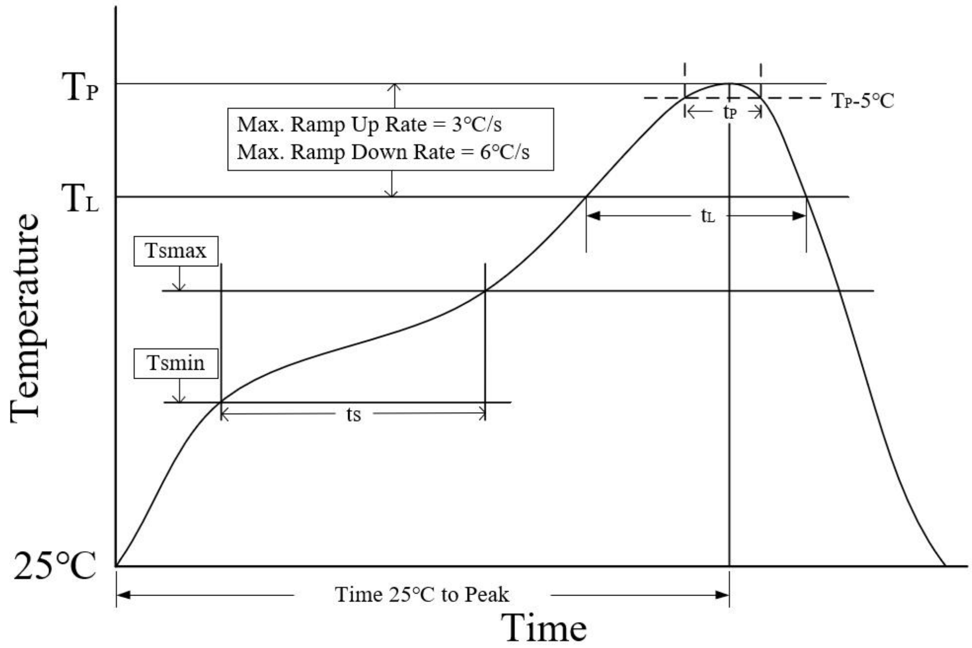
Package type	Reel diameter A (mm)	Tape width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
SOP14	330±1	12.4	$6.50^{+0.20}_{-0.1}$	$9.30^{+0.20}_{-0.1}$	2.0±0.10	8.00±0.1	16.00±0.10
DFN14	329±1	12.4	3.75±0.1	4.25±0.1	1.00±0.1	8.00±0.1	12.00±0.3

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	MSL	PACKING
SIT1145GQT/FD	SOP14	MSL3	Tape and reel
SIT1145GQTK/FD	DFN4.5×3-14	MSL3	Tape and reel

SOP14 is packed with 2500 pieces/disc in braided packaging. Leadless DFN4.5×3-14 is packed with 3000 pieces/disc in braided packing.

REFLOW SOLDERING



Parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	3 °C/second max
Preheat time ts (T_{smin}=150 °C to T_{smax}=200 °C)	60-120 seconds
Melting time t_L)T_L=217 °C)	60-150 seconds
Peak temp T_P	260-265 °C
5°C below peak temperature t_P	30 seconds
Ave cooling rate (T_P to T_L)	6 °C/second max
Normal temperature 25°C to peak temperature TP time	8 minutes max

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

VERSION HISTORY

Version number	Data sheet status	Revision Date
V1.0	Initial version.	March 2026