FEATURES

- Compatible with the ISO 11898-2:2024 and SAE J2284-1~ SAE J2284-5 standard
- AEC-Q100 Grade 1 qualified
- Thermally protected
- ±42V BUS Protection
- Transmit Data (TXD) dominant time-out function
- Low-power standby mode with wake-up function
- SIT1044GQT/3 and SIT1044GQTK/3 I/O pins support 1.8V, 3.3V and 5V MCU
- Undervoltage protection on pins VCC and VIO
- High-speed CAN, supporting the optimized 8Mbps Flexible Data-Rate (CAN FD)
- High ElectroMagnetic Immunity
- Unpowered state disengages from the bus
- Available in SOP8 and DFN3*3-8 packages. DFN3*3-8 with improved Automated Optical Inspection (AOI) capability.

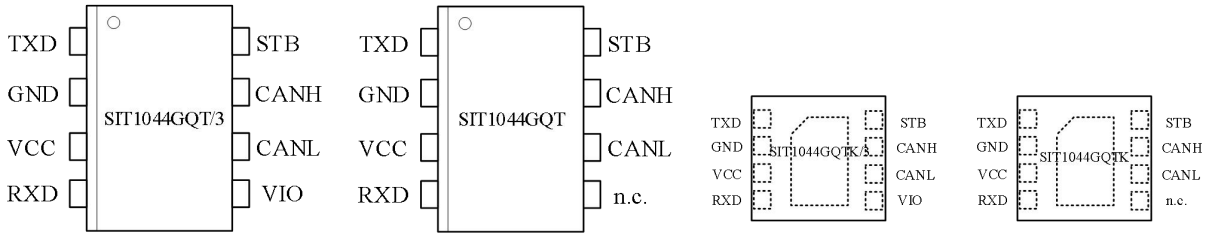
DESCRIPTION

SIT1044GQ is an interface chip used between the CAN protocol controller and the physical bus. It can be used for in-vehicle, industrial control and other fields. It supports 8Mbps (CAN FD), and has the ability to perform differential signal transmission between bus and the CAN protocol controller.

SIT1044GQ is fully compatible with the SIT1044Q and other family products. SIT1044GQ features improved bus signal symmetry and lower electromagnetic radiation performance.

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
Bus supply voltage	VCC	4.5	5.5	V
MCU side port supply voltage	VIO	1.7	5.5	V
CANH/CANL input or output voltage	V_{can}	-42	+42	V
Bus differential voltage	V_{diff}	1.5	3.0	V
Ambient temperature	T_{amb}	-40	125	℃
Virtual junction temperature	T_j	-40	150	℃

PIN CONFIGURATION



PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	TXD	transmit data input
2	GND	ground
3	VCC	supply voltage
4	RXD	receive data output
5	VIO	transceiver I/O level conversion power supply voltage (SIT1044GQT/3, SIT1044GQTK/3)
	n.c.	Not connected in SIT1044GQT and SIT1044GQTK version.
6	CANL	LOW-level CAN-bus line
7	CANH	HIGH-level CAN-bus line
8	STB	standby mode control input, low level is high speed mode

Note: The metal pad on the back of the DFN3*3-8 package is recommended to be grounded.

LIMITING VALUES

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
Supply voltage	VCC, VIO	pins VCC, VIO	-0.3~+7	V
MCU side port	V_{TXD}, V_{RXD}, V_{STB}	pins TXD, RXD, STB	-0.3~+7	V
Bus side input voltage	V_{CANL}, V_{CANH}	pins CANH, CANL	-42~+42	V
Bus differential breakdown voltage	$V_{CANH-CANL}$		-42~+42	V
Contact discharge model (IEC)	VESD_IEC (2)	pins CANH, CANL	-8~+8	kV
Human body model (HBM)	VESD_HBM (3)	All pins	-4~+4	kV
		pins CANH and CANL	-8~+8	kV
Charged device model (CDM)	VESD_CDM (4)	All pins	-2000~+2000	V
Transient voltage	V_{trt} (5)	Pulse 1	-100	V
		Pulse 2a	75	V
		Pulse 3a	-150	V
		Pulse 3b	100	V
Storage temperature	T_{stg}		-55~150	℃
Ambient temperature	T_{amb}		-40~125	℃
Virtual junction temperature	T_j		-40~150	℃

(1) The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

(2) According to IEC 61000-4-2.

(3) According to AEC-Q100-002.

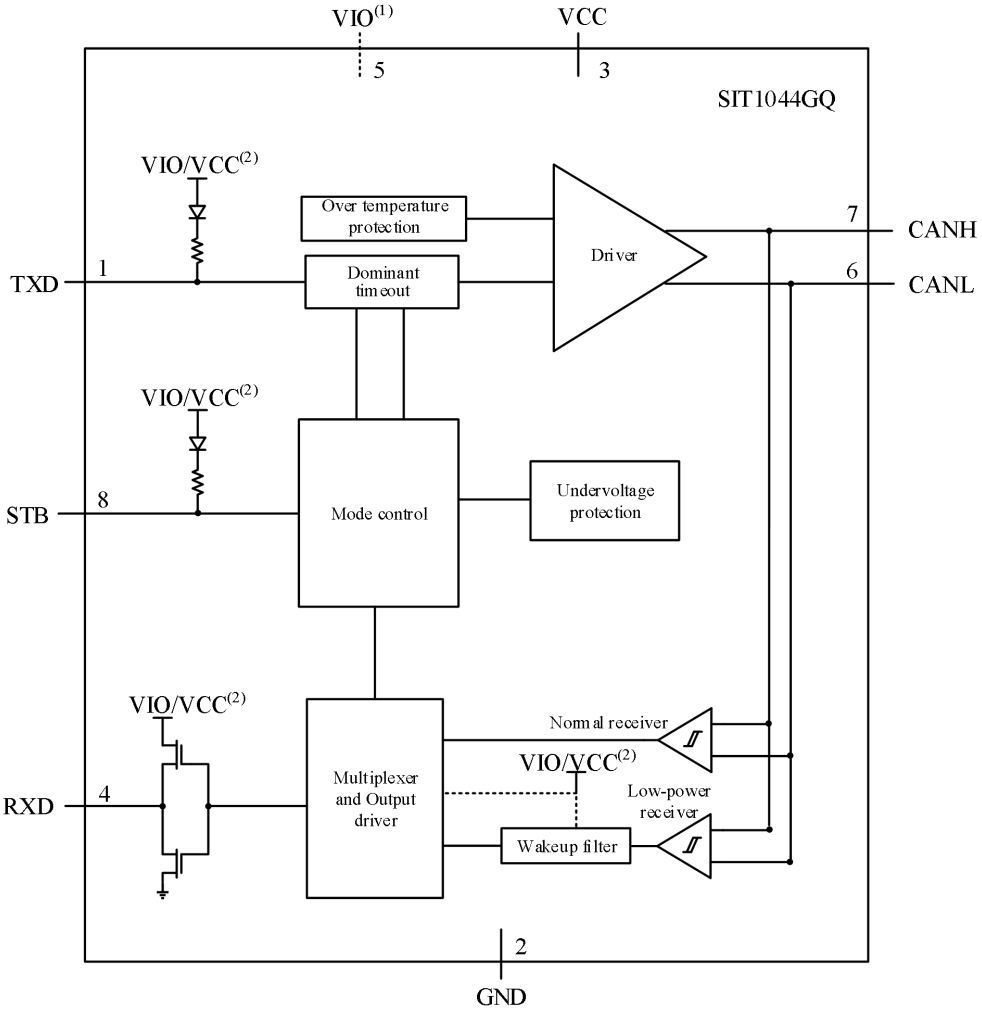
(4) According to AEC-Q100-011.

(5) Verified by an external test house according to IEC 62228-3; parameters for standard pulses defined in ISO7637.

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	SOP8	95	℃/W
		DFN3*3-8	65	℃/W
$R_{\theta JC}$	Junction-to-case thermal resistance	SOP8	46	℃/W
		DFN3*3-8	35	℃/W

INTERNAL CIRCUIT BLOCK DIAGRAM



(1) VIO is only available in SIT1044GQT/3 and SIT1044GQTK/3 version, pin 5 is not connected in SIT1044GQT and SIT1044GQTK.

(2) VIO is in SIT1044GQT/3 and SIT1044GQTK/3 version and VCC is in SIT1044GQT and SIT1044GQTK.

STATIC CHARACTERISTICS

Unless specified otherwise; all values are tested in recommended operating conditions: T_j=-40℃~150℃, VCC=4.5V~5.5V, VIO=1.7V~5.5V (SIT1044GQT/3 and SIT1044GQTK/3), R_L=60Ω.

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply: pin VCC						
Supply voltage	VCC		4.5	-	5.5	V
Standby undervoltage detection voltage	$V_{uvd(stb)}$		3.4	-	4.5	V
Standby undervoltage hysteresis voltage	$V_{uvhys(stb)}$ (2)		50	-	-	mV
Switch-off undervoltage detection voltage	$V_{uvd(swoff)}$	SIT1044GQT/3 and SIT1044GQTK/3	1.2	-	1.7	V
VCC supply current	I_{CC}	Normal mode; dominant; $t<t_{to(dom)TXD}$; V_{TXD}=0V	-	40	70	mA
		Normal mode; dominant; short circuit on bus lines; V_{TXD}=0V; -3V< (V_{CANH}=V_{CANL}) <+40V	-	-	125	mA
		Normal mode; recessive; V_{TXD}=VIO (1)	-	5.1	10	mA
		Standby mode; SIT1044GQT/3 and SIT1044GQTK/3	-	-	2	μA
		Standby mode; SIT1044GQT and SIT1044GQTK	-	-	26	μA
I/O level adapter supply; pin VIO (SIT1044GQT/3 and SIT1044GQTK/3)						
Supply voltage	VIO		1.7	-	5.5	V
Switch-off undervoltage detection voltage	$V_{uvd(swoff)}$		1.2	-	1.7	V
VIO supply current	I_{IO}	Normal mode; dominant; V_{TXD}=0V	-	220	760	μA
		Normal mode; recessive; V_{TXD}=VIO (1)	-	110	460	μA
		Standby mode	-	-	24	μA
Pin TXD characteristics						
HIGH-level input voltage	V_{IH}	SIT1044GQT and SIT1044GQTK	0.7VCC	-	-	V
		SIT1044GQT/3 and SIT1044GQTK/3	0.7VIO (1)	-	-	V
LOW-level input voltage	V_{IL}	SIT1044GQT and SIT1044GQTK	-	-	0.3VCC	V
		SIT1044GQT/3 and SIT1044GQTK/3	-	-	0.3VIO (1)	V
Hysteresis voltage	$V_{hys(TXD)}$ (2)	SIT1044GQT/3 and SIT1044GQTK/3	50	-	-	mV

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Pull-up resistance	R_{pu}	2.8V<VIO<5.5V	20	-	80	kΩ
Unpowered leakage current on pin TXD	I_O(off)	VCC=VIO=0V TXD=5V	-1	-	1	μA
Input capacitance	C_i (2)		-	-	10	pF
Pin RXD characteristics						
HIGH-level output current	$I_{OH(RXD)}$	V_{RXD}=VIO-0.4V (1)	-10	-	-1	mA
LOW-level output current	$I_{OL(RXD)}$	Bus dominant; V_{RXD}=0.4V	1	-	10	mA
Pin STB characteristics						
HIGH-level input voltage	V_{IH}	SIT1044GQT and SIT1044GQTK	0.7VCC	-	-	V
		SIT1044GQT/3 and SIT1044GQTK/3	0.7VIO (1)	-	-	V
LOW-level input voltage	V_{IL}	SIT1044GQT and SIT1044GQTK	-	-	0.3VCC	V
		SIT1044GQT/3 and SIT1044GQTK/3	-	-	0.3VIO (1)	V
Hysteresis voltage	V_{hys} (2)	SIT1044GQT/3 and SIT1044GQTK/3	50	-	-	mV
Pull-up resistance	R_{pu}	2.8V<VIO<5.5V	20	-	80	kΩ
Unpowered leakage current on pin STB	I_O(off)	VCC=VIO=0V; STB=5V	-1	-	1	μA
Input capacitance	C_i (2)		-	-	10	pF
Overtemperature protection						
Shutdown junction temperature	$T_{j(sd)}$ (2)		-	190	-	°C
Release shutdown junction temperature	T_{hys} (2)		-	20	-	°C
Bus lines; pins CANH and CANL						
Dominant output voltage on pin CANH	$V_{O(dom)}$	$t<t_{to(dom)TXD}$; V_{TXD}=0V; R_L=50Ω to 65Ω	2.89	3.55	4.26	V
Dominant output voltage on pin CANL			0.77	1.45	2.13	V
Transmitter voltage symmetry	V_{TXsym}	$V_{TXsym}=V_{CANH}+V_{CANL}$; C_{SPLIT}=4.7nF; f_{TXD}=250kHz, 1MHz or 2.5MHz	0.9VCC	-	1.1VCC	V
Common mode voltage step	$V_{cm(step)}$ (2)		-150	-	150	mV
Peak-to-peak common mode voltage	$V_{cm(p-p)}$ (2)		-300	-	300	mV
Differential output voltage	$V_{O(diff)}$	Normal mode; $t<t_{to(dom)TXD}$; V_{TXD}=0V; R_L=50Ω to 65Ω	1.5	-	3	V
		Normal mode; $t<t_{to(dom)TXD}$; V_{TXD}=0V; R_L=45Ω to 70Ω	1.4	-	3.3	V

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
		Normal mode; dominant; $t<t_{to(dom)TXD}$; V_{TXD}=0V; R_L=2240Ω	1.5	-	5	V
		Normal mode; recessive; V_{TXD}=VIO [1]; No load	-50	-	+50	mV
		Normal mode; recessive; V_{TXD}=VIO [1]; R_L =60Ω	-50	-	+50	mV
		Standby mode; dominant; No load	-0.2	-	+0.2	V
Output voltage	$V_{O(rec)}$	Normal mode; V_{TXD}=VIO [1]; No load	2	0.5VCC	3	V
		Normal mode; V_{TXD}=VIO [1]; R_L =60Ω	2.2	0.5VCC	2.8	V
		Standby mode; No load	-0.1	-	+0.1	V
Differential receiver threshold voltage	$V_{th(RX)diff}$	Normal mode; -12V≤V_{CANH}≤12V -12V≤V_{CANL}≤12V	0.5	-	0.9	V
		Standby mode; -12V≤V_{CANH}≤12V -12V≤V_{CANL}≤12V	0.4	-	1.1	V
Receiver recessive voltage	$V_{rec(RX)}$	Normal mode; -12V≤V_{CANH}≤12V -12V≤V_{CANL}≤12V	-4	-	0.5	V
		Standby mode; -12V≤V_{CANH}≤12V -12V≤V_{CANL}≤12V	-4	-	0.4	V
Receiver dominant voltage	$V_{dom(RX)}$	Normal mode; -12V≤V_{CANH}≤12V -12V≤V_{CANL}≤12V	0.9	-	9	V
		Standby mode; -12V≤V_{CANH}≤12V -12V≤V_{CANL}≤12V	1.1	-	9	V
Differential receiver hysteresis voltage	$V_{hys(RX)dif}$	Normal mode; -12V≤V_{CANH}≤12V -12V≤V_{CANL}≤12V	-	60	-	mV
Short-circuit output current	$I_{O(SC)}$	V_{CANH}=-15V to 40V; V_{CANL}=-15V to 40V	-	-	115	mA
Recessive short-circuit output current	$I_{O(SC)rec}$	V_{CANH}=-27V to 32V; V_{CANL}=-27V to 32V; V_{TXD}=VIO for $t>t_{d(TXD-busrec)end}$	-5	-	5	mA
Leakage current	I_L	VCC=VIO= 0V or pins shorted to GND via 47kΩ; T_j<105℃ V_{CANH}=V_{CANL}=5V	-10	-	10	μA
Input resistance	R_i	-2V≤V_{CANH}≤7V -2V≤V_{CANL}≤7V	25	40	50	kΩ
Input resistance deviation	$\triangle R_i$	0V≤V_{CANH}≤5V 0V≤V_{CANL}≤5V	-3		3	%
Differential input resistance	R_{ID}	-2V≤V_{CANH}≤7V -2V≤V_{CANL}≤7V	50	80	100	kΩ
Common-mode input capacitance	$C_{i(cm)}$ [2]		-	-	24	pF

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Differential input capacitance	$C_{i(diff)}$ (2)		-	-	12	pF
Slew Rate	SR(2)	R_L=60Ω, C_L=100pF	-	-	70	V/μs

DYNAMIC CHARACTERISTICS

Unless specified otherwise; all values are tested in recommended operating conditions: T_j=-40℃~150℃, VCC=4.5V~5.5V, VIO=1.7V~5.5V (SIT1044GQT/3 and SIT1044GQTK/3), R_L=60Ω.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CAN timing characteristics; $t_{bit(TXD)}$≥200ns; Figure 1, Figure 3 and Figure 4						
Delay time from TXD to bus dominant	$t_{d(TXD-busdom)}$	Normal mode	-	-	80	ns
Delay time from TXD to bus recessive	$t_{d(TXD-busrec)}$	Normal mode	-	-	80	ns
Delay time from bus dominant to RXD	$t_{d(busdom-RXD)}$	Normal mode	-	-	110	ns
Delay time from bus recessive to RXD	$t_{d(busrec-RXD)}$	Normal mode	-	-	110	ns
Delay time from TXD LOW to RXD LOW	$t_{d(TXDL-RXDL)}$	Normal mode	40	-	190	ns
Delay time from TXD HIGH to RXD HIGH	$t_{d(TXDH-RXDH)}$	Normal mode	40	-	190	ns
CAN FD timing characteristics (According to ISO 11898-2:2024 set B); Figure 1 and Figure 4						
Transmitted recessive bit width	$t_{bit(bus)}$	$t_{bit(TXD)}$=500ns	455	-	510	ns
		$t_{bit(TXD)}$=200ns	155	-	210	ns
Bit time on pin RXD	$t_{bit(RXD)}$	$t_{bit(TXD)}$=500ns	420	-	520	ns
		$t_{bit(TXD)}$=200ns	120	-	220	ns
Transmitted recessive bit width deviation	$\Delta t_{bit(BUS)}$	$\Delta t_{bit(BUS)}=t_{bit(bus)}- t_{bit(TXD)}$	-45	-	10	ns
Receiver timing symmetry	Δt_{rec}	$\Delta t_{rec}=t_{bit(RXD)}- t_{bit(bus)}$	-45	-	15	ns
Received recessive bit width deviation	$\Delta t_{bit(RXD)}$	$\Delta t_{bit(RXD)}=t_{bit(RXD)}- t_{bit(TXD)}$	-80	-	20	ns
CAN FD timing characteristics (According to ISO 11898-2:2024 set C); Figure 1 and Figure 4						
Transmitted recessive bit width	$t_{bit(bus)}$ (2)	$t_{bit(TXD)}$=500ns	490	-	510	ns
		$t_{bit(TXD)}$=200ns	190	-	210	ns
		$t_{bit(TXD)}$=125ns	115	-	135	ns
Bit time on pin RXD	$t_{bit(RXD)}$ (2)	$t_{bit(TXD)}$=500ns	470	-	520	ns
		$t_{bit(TXD)}$=200ns	170	-	220	ns
		$t_{bit(TXD)}$=125ns	95	-	145	ns
Transmitted recessive bit width deviation	$\Delta t_{bit(BUS)}$ (2)	$\Delta t_{bit(BUS)}=t_{bit(bus)}- t_{bit(TXD)}$	-10	-	10	ns
Receiver timing symmetry	Δt_{rec} (2)	$\Delta t_{rec}=t_{bit(RXD)}- t_{bit(bus)}$	-20	-	15	ns

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Received recessive bit width deviation	$\Delta t_{bit(RXD)}$ (2)	$\Delta t_{bit(RXD)}=t_{bit(RXD)}- t_{bit(TXD)}$	-30	-	20	ns
TXD dominant time-out time						
TXD dominant time-out time	$t_{to(dom)TXD}$	VTXD=0V; Normal mode	0.8	-	9	ms
Bus wake-up times; pins CANH and CANL; Figure 10						
Bus dominant wake-up time	$t_{wake(busdom)}$	Standby mode	0.5	-	1.8	μs
Bus recessive wake-up time	$t_{wake(busrec)}$	Standby mode	0.5	-	1.8	μs
Bus wake-up time-out time	$t_{to(wake)bus}$	Standby mode	0.8	-	9	ms
Mode transitions						
RXD start up time	$t_{startup(RXD)}$ (2)	Switches to standby mode after waking up	4	-	50	μs

(1) VIO only in SIT1044GQT/3 and SIT1044GQTK/3 version.

(2) Guaranteed by design, not tested in production.

TEST CIRCUIT

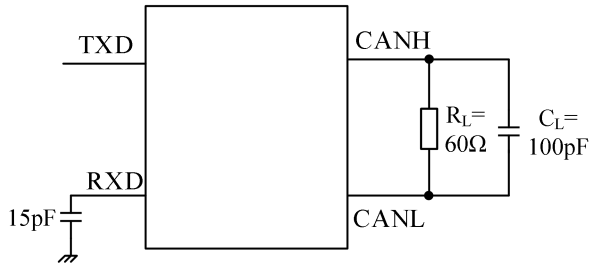


Figure 1 CAN transceiver timing test circuit

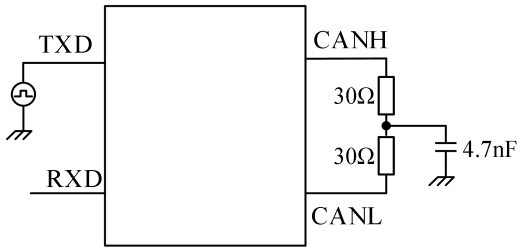


Figure 2 Test circuit for measuring transceiver driver symmetry

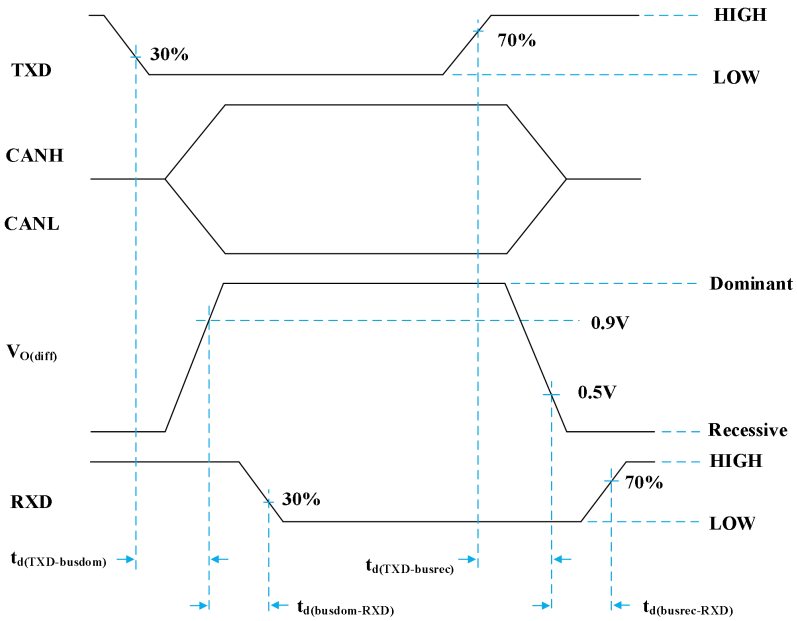


Figure 3 CAN transceiver timing diagram

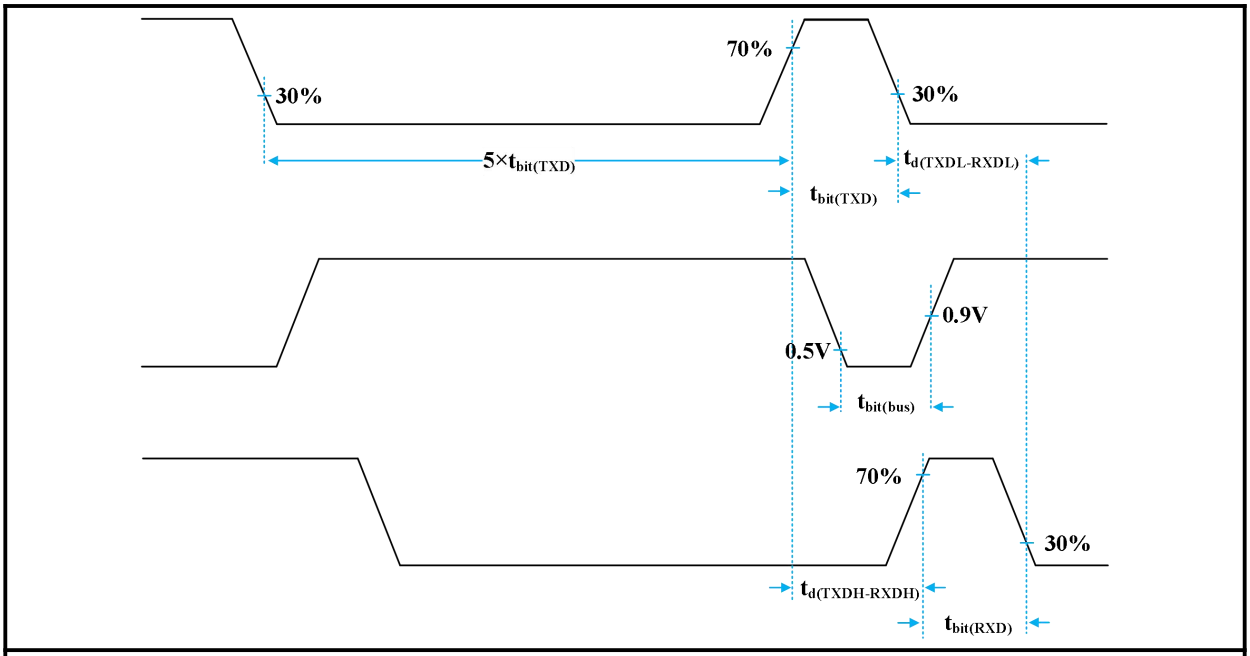
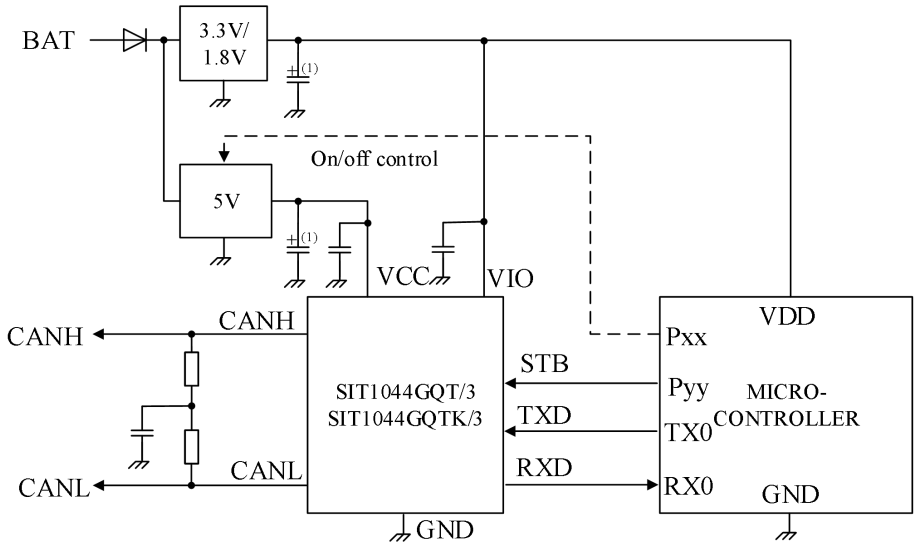


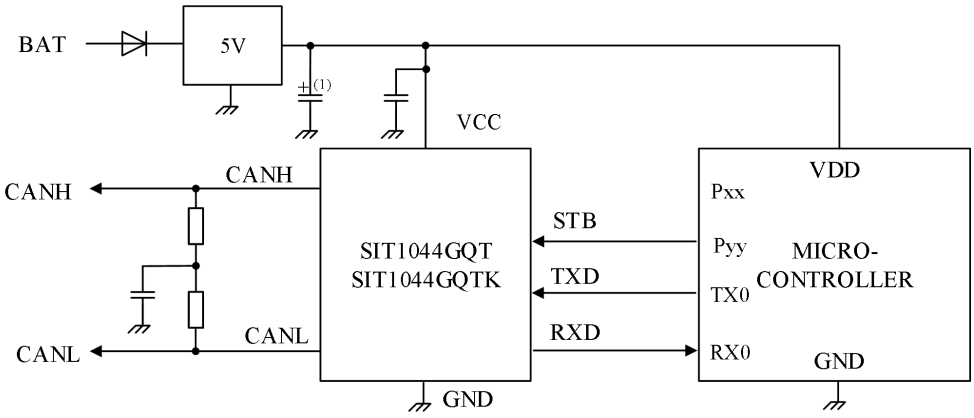
Figure 4 CAN FD timing definitions according to ISO 11898-2:2024

APPLICATION INFORMATION



(1) Optional, depends on regulator.

Figure 5 Typical SIT1044GQT/3 and SIT1044GQTK/3 application with a 3.3V/1.8V microcontroller



(1) Optional, depends on regulator.

Figure 6 Typical SIT1044GQ application with a 5V microcontroller

ADDITIONAL DESCRIPTION

1 Sketch

The SIT1044GQ is an interface chip designed for use between CAN protocol controllers and the physical bus, applicable in automotive and industrial control fields. It supports Flexible Data-Rate of up to 8Mbps and features differential signal transmission capability between the bus and the CAN protocol controller.

2 Overtemperature protection

The device is protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, the CAN bus drivers are disabled. When the junction temperature drops below $T_{j(sd)rel}$, the CAN bus drivers recover once TXD has been reset to HIGH and Normal mode is selected (waiting for TXD to go HIGH prevents output driver oscillation due to small variations in temperature).

3 Undervoltage protection

If VCC drops below the standby undervoltage detection threshold ($V_{uvd(stb)}$), the transceiver switches to Standby mode. The logic state of pin STB is ignored until VCC has recovered.
In SIT1044GQT/3 and SIT1044GQTK/3 version, if VIO drops below the switch-off undervoltage detection threshold ($V_{uvd(swoff)}$), the transceiver switches to Off mode and disengages from the bus (high-ohmic) until VIO has recovered.
In the SIT1044GQ, if VCC drops below the switch-off undervoltage detection threshold ($V_{uvd(swoff)}$), the transceiver switches to Off mode and disengages from the bus (high-ohmic) until VCC has recovered.

4 Operating modes

SIT1044GQ supports three operating modes, Normal, Standby and Off. The operating mode is selected via pin STB. The following table shows the corresponding mode status.

Mode	Inputs		Outputs	
	STB	TXD	CAN driver	RXD
Normal	LOW	LOW	Dominant	LOW
		HIGH	Recessive	LOW when bus dominant
				HIGH when bus recessive
Standby	HIGH	X	Biased to ground	Follows BUS when wake-up detected
				HIGH when no wake-up detected
Off (1)	X	X	High-ohmic state	High-ohmic state

(1) Off mode is entered when the voltage on pin VIO or pin VCC is below the switch-off undervoltage detection threshold.

4.1 Off mode

The SIT1044GQ switches to Off mode from any mode when the supply voltage falls below the switch-off undervoltage threshold $V_{uvd(swoff)}$. This is the default mode when powered on.
In Off mode, the pins CAN and RXD are in a high-ohmic state.

4.2 Standby mode

When the supply voltage rises above the switch-off undervoltage detection threshold, the SIT1044GQ starts to boot up, triggering an initialization procedure.

Standby mode is selected when pin STB goes HIGH. In this mode, the transceiver is unable to transmit or receive data and a low-power receiver is activated to monitor the bus for a wake-up pattern. The transmitter and Normal-mode receiver blocks are switched off and the bus pins are biased to ground to minimize system supply current. Pin RXD follows the bus after a wake-up request has been detected.

A transition to Normal mode is triggered when STB is forced LOW.

If the supply voltage is below the Standby undervoltage hysteresis voltage $V_{uvd(stb)}$ when STB goes LOW, the SIT1044GQ will remain in Standby mode.

Pending wake-up events will be cleared and differential data on the bus pins converted to digital data via the low-power receiver and output on pin RXD.

In SIT1044GQT/3 and SIT1044GQTK/3 version, the low-power receiver is supplied from VIO and can detect CAN bus activity when VIO is above switch-off undervoltage detection voltage $V_{uvd(swoff)}$ (even if VIO is the only available supply voltage).

4.3 Normal mode

A LOW level on pin STB selects Normal mode, provided the supply voltage on pin VCC is above the standby undervoltage detection threshold, $V_{uvd(std)}$.

In this mode, the transceiver can transmit and receive data via bus lines CANH and CANL. Pin TXD must be HIGH at least once in Normal Mode before transmission can begin. The differential receiver converts the analog data on the bus lines into digital data on pin RXD. The slopes of the output signals on the bus lines into digital data on pin RXD. The differential receiver converts the analog data on the bus lines into digital data on pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME. In order to support high bit rates, especially in CAN FD systems, the Signal Improvement function largely eliminates topology-related reflections and impedance mismatches. In recessive state, the output voltage on the bus pins is VCC/2.

4.4 Operating modes and gap-free operation

Gap-free operation guarantees defined behavior at all voltage levels. Supply voltage-to-operating mode mapping is detailed in **Figure 9** in the state diagrams (**Figure 7** and **Figure 8**)。

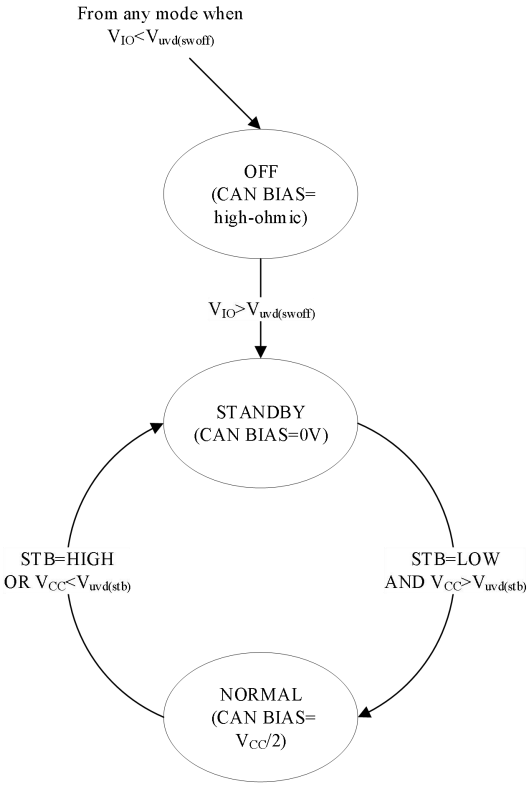


Figure 7 SIT1044GQT/3 and SIT1044GQTK/3 state diagram

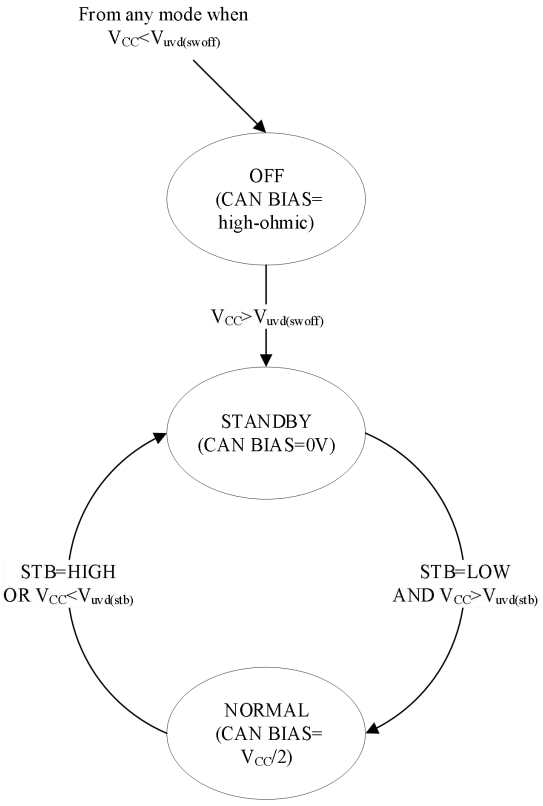


Figure 8 SIT1044GQ state diagram

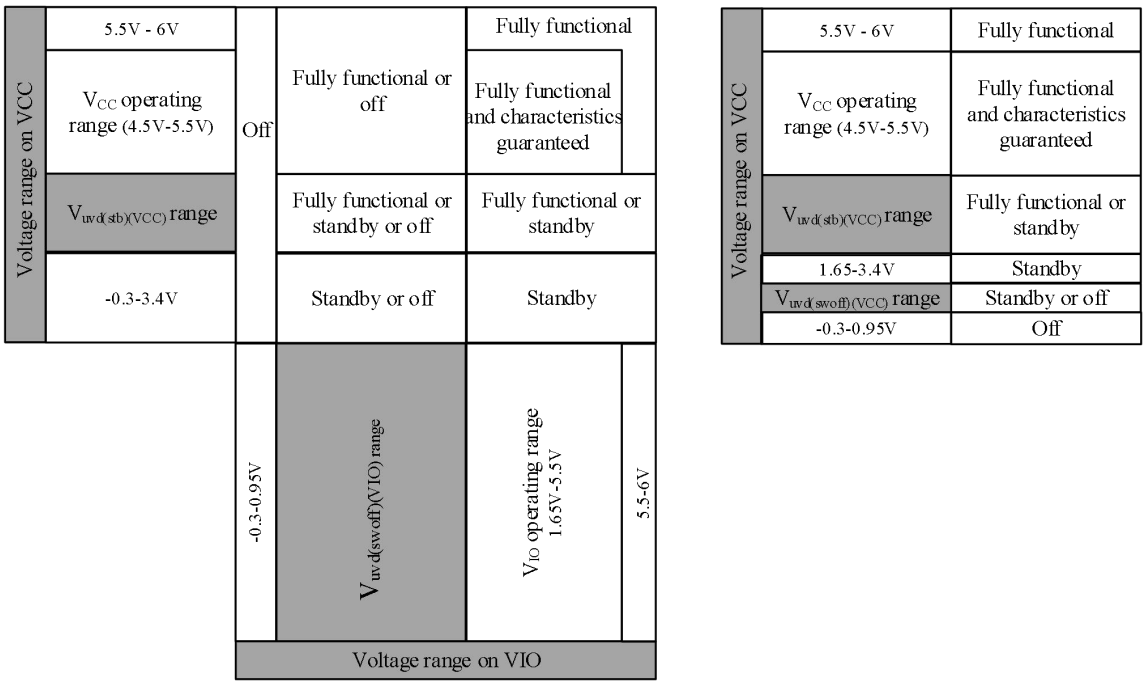


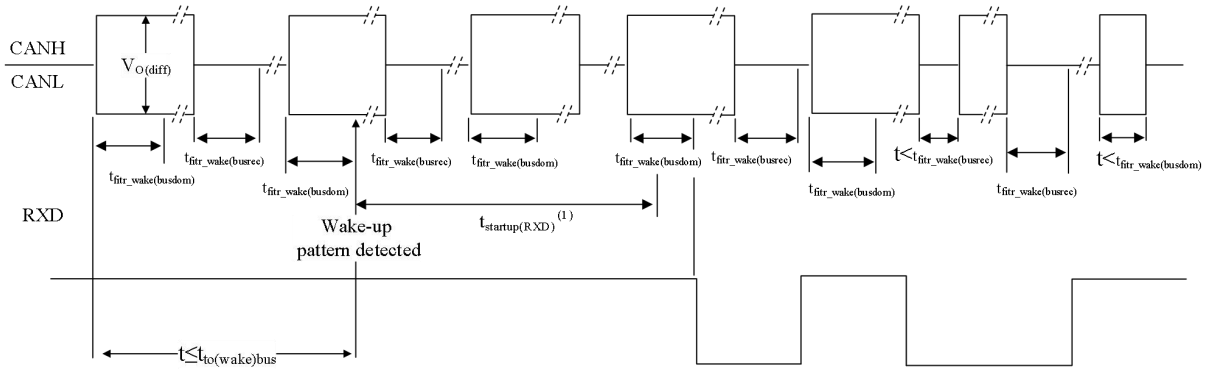
Figure 9 Supply voltage ranges and gap-free operation

5 Dominant timeout function

A "TXD dominant time-out" timer is started when pin TXD is set LOW. If the LOW state on this pin persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD goes HIGH.

6 Remote wake-up

SIT1044GQ wakes up from Standby mode when dedicated wake-up pattern is detected on the bus. Wake-up timing is shown in the **Figure 10**.



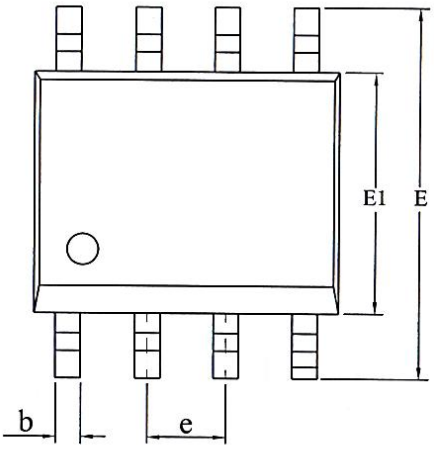
(1) During $t_{startup(RXD)}$, the low-power receiver is on but pin RXD is not active (i.e. HIGH/recessive). The first dominant pulse of width ≥ $t_{filr_(wake)bus}$ that ends after $t_{startup(RXD)}$ will trigger RXD to go LOW/dominant.

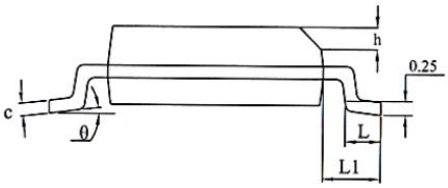
Figure 10 Wake-up timing

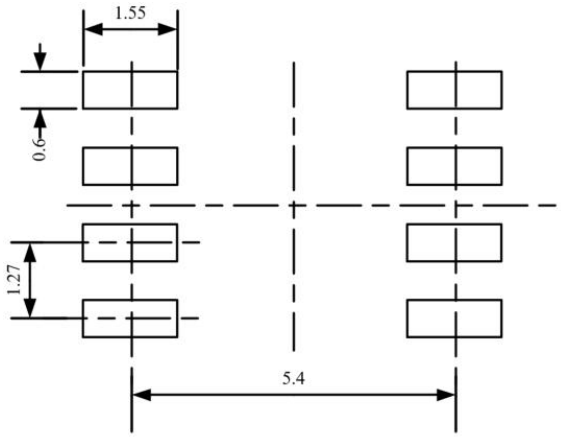
SOP8 DIMENSIONS

Package size

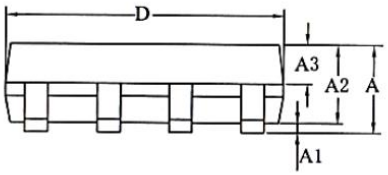
Symbol	Min./mm	Typ./mm	Max./mm
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.50	-	0.80
L1	1.05REF		
c	0.20	-	0.24
θ	0°	-	8°







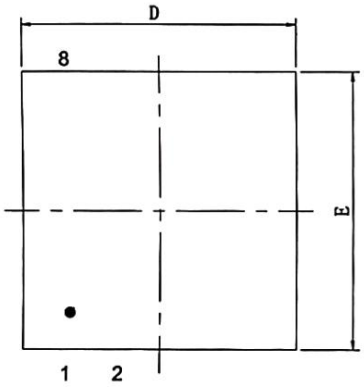
LAND PATTERN EXAMPLE (Unit: mm)

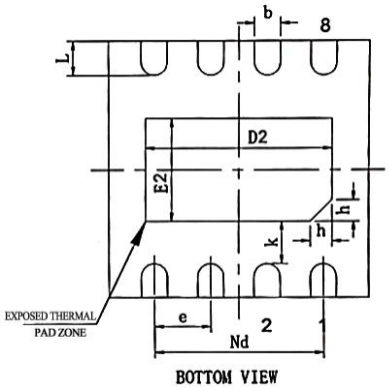


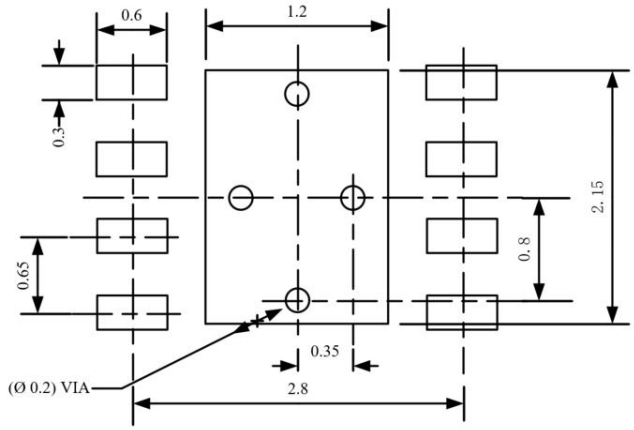
DFN3*3-8 DIMENSIONS

Package size

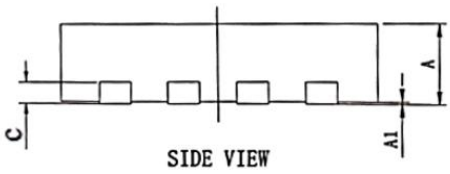
Symbol	Min./mm	Typ./mm	Max./mm
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.203 REF	
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	2.05	2.15	2.25
Nd		1.95BSC	
E2	1.10	1.20	1.30
b	0.25	0.30	0.35
e		0.65BSC	
k		0.50REF	
L	0.35	0.40	0.45
h	0.20	0.25	0.30



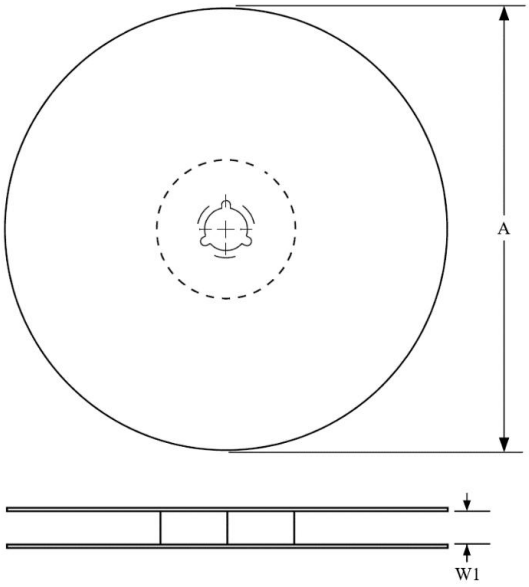




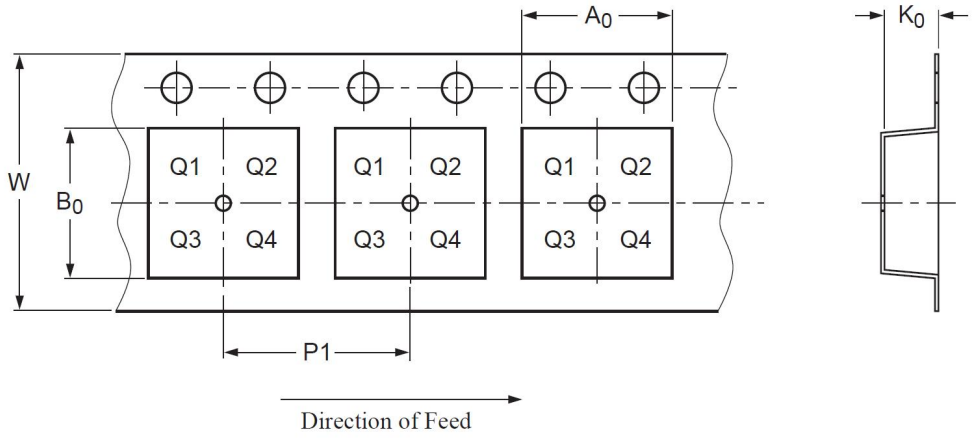
LAND PATTERN EXAMPLE (Unit: mm)



TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



PIN1 is in quadrant 1

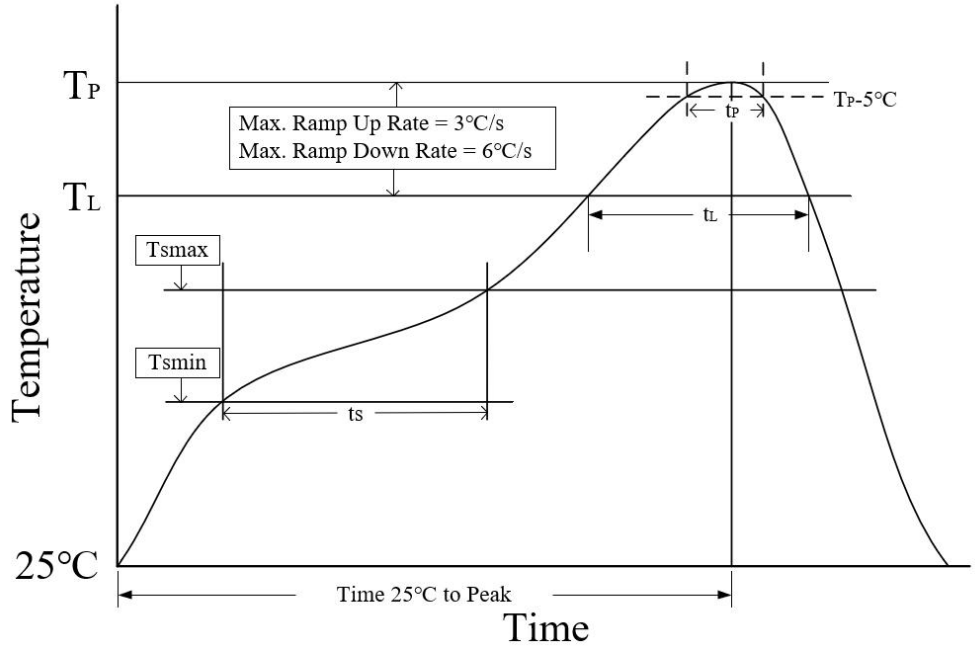
Package Type	Reel Diameter A (mm)	Tape Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
SOP8	330±1	12.4	6.60±0.1	5.30±0.10	1.90±0.1	8.00±0.1	12.00±0.1
DFN3*3-8	329±1	12.4	3.30±0.1	3.30±0.1	1.10±0.1	8.00±0.1	12.00±0.3

ORDERING INFORMATION

Type number	Package	MSL	Packing
SIT1044GQT/3	SOP8	MSL3	Tape and reel
SIT1044GQT	SOP8	MSL3	Tape and reel
SIT1044GQTK/3	DFN3*3-8	MSL1	Tape and reel
SIT1044GQTK	DFN3*3-8	MSL1	Tape and reel

SOP8 is packed with 2500 pieces/disc in braided packaging; Leadless DFN3*3-8 is packed with 6000 pieces/disc in braided packaging.

REFLOW SOLDERING



Parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	3 °C/second max
Preheat time ts (T_{smin}=150 °C to T_{smax}=200 °C)	60-120 seconds
Melting time t_L (T_L=217 °C)	60-150 seconds
Peak temp T_P	260-265 °C
5 °C below peak temperature t_P	30 seconds
Ave cooling rate (T_P to T_L)	6 °C/second max
Normal temperature 25°C to peak temperature T_P time	8 minutes max

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Data sheet status	Revision date
V1.0	Initial version.	October 2025
V1.1	Updated the value of IEC; Updated the expression format of the ESD test conditions; Added power consumption of SIT1044GQT and SIT1044GQTK in standby mode; Added the parameter of Slew Rate.	March 2026
V1.2	Updated the value of SR; Added MSL Ratings; Error corrected (Adjusted I_{CC} standby mode current specification for SIT1044GQT/SIT1044GQTK: updated value to 26μA).	April 2026
V1.3	Optimized Flexible Data-Rate; Added CAN FD timing characteristic specifications that meet ISO 11898-2:2024 set C requirements.	August 2026
V1.4	Added the AEC-Q100 qualification grade; Added ambient temperature; Added “guaranteed by design” flags for hysteresis and overtemperature-related parameters.	September 2026