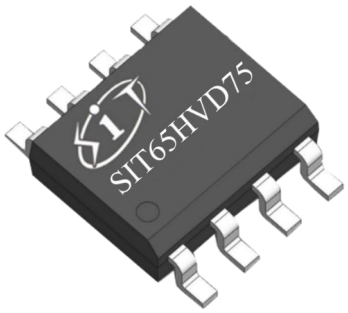
FEATURES

- 3.0V~5.5V Wide Power Range, Half-Duplex
- ESD protection for RS-485 I/O pins ±15kV HBM
- Bus fault tolerance and withstand voltage reach ±15V
- Driver short-circuit output protection
- Low power off function
- Receiver open-circuit failure protection
- Strong anti-noise ability
- Integrated transient voltage suppression function
- Data transmission up to 20Mbps in an electric noise environment
- provides small shape DFN3*3-8, MSOP8/VSSOP8 and BGA packages

PRODUCT APPEARANCE



Provide green and environmentally friendly lead-free package

DESCRIPTION

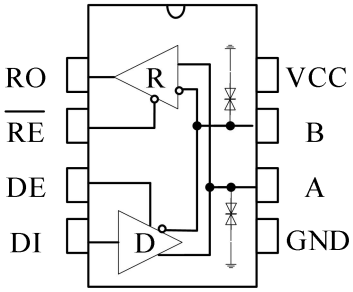
SIT65HVD75 is a RS-485 transceiver with 3.0V~5.5V wide power supply, bus port ESD protection capacity of over ±15kV HBM, bus withstand voltage range of ±15V, half duplex, low power consumption, and fully meet the requirements of TIA/EIA-485 standard.

SIT65HVD75 includes a driver and a receiver, both of which can be enabled and closed independently. When both are disabled, both the driver and the receiver output are high resistance state. It can realize error-free data transmission up to 20Mbps.

SIT65HVD75 has a working voltage range of 3.0~5.5V, and has the functions of fail-safe, current-limiting protection and over-voltage protection, etc.

PIN CONFIGURATION

SIT65HVD75



SIT65HVD75C

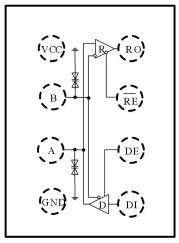


Fig 1 SIT65HVD75 Pin Configuration (Top view)

PIN DESCRIPTON

SYMBOL	SIT65HVD75 PIN	SIT65HVD75C PIN	DESCRIPTION
RO	**1**	**8**	Receiver Output. When /RE is low and if A - B≥-10mV, RO will be high; if A - B≤-200mV, RO will be low.
/RE	**2**	**7**	Receiver Output Enable. Drive /RE low to enable RO; RO is high impedance when /RE is high. Drive /RE high and DE low to enter low-power shutdown mode.
DE	**3**	**6**	Driver Output Enable. Drive DE high to enable driver outputs. These outputs are high impedance when DE is low. Drive/RE high and DE low to enter low-power shutdown mode.
DI	**4**	**5**	Driver Input. With DE high, a low on DI forces non-inverting output low and inverting output high. Similarly, a high on DI forces non-inverting output high and inverting output low.
GND	**5**	**4**	Ground.
A	**6**	**3**	non-inverting Receiver Input and non-inverting Driver Output.
B	**7**	**2**	Inverting Receiver Input and Inverting Driver Output.
VCC	**8**	**1**	Positive Supply.

Note: The metal pad on the back of the DFN3*3-8 and MSOP8/VSSOP8 package is recommended to be grounded.

LIMITING VALUES

PARAMETER	SYMBOL	VALUE	UNIT
Supply voltage	VCC	+7	V
Control Input Voltage	/RE, DE, DI	-0.3~VCC+0.5	V
Receiver Input Voltage	A, B	-15~+15	V
Receiver Output Voltage	RO	-0.3~VCC+0.5	V
Operating Temperature Ranges	T_A	-40~125	℃
Storage Temperature Range	T_{stg}	-60~150	℃
Lead Temperature		300	℃

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

DRIVER DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Differential Driver Output （No load）	V_{OD1}		2.5		5.5	V
Differential Driver Output	V_{OD2}	Fig 2, RL=54Ω, VCC=3.3V	1.5	1.8	VCC	V
		Fig 2, RL=54Ω, VCC=5V	1.5	3	VCC	V
Change in Magnitude of Driver Differential Output Voltag（NOTE1）	ΔV_{OD}	Fig 2, RL=54Ω			0.2	V
Driver Common-Mode Output Voltage	V_{OC}	Fig 2, RL=54Ω			3	V
Change in Magnitude of Common-Mode Output Voltage（NOTE1）	ΔV_{OC}	Fig 2, RL=54Ω			0.2	V
Input High Voltage	V_{IH}	DE, DI, /RE	2.0			V
Input Low Voltage	V_{IL}	DE, DI, /RE			0.8	V
Logic Input Current	I_{IN1}	DE, DI, /RE	-2		2	μA
Output short-circuit current, short-circuit to high	I_{OSD1}	short-circuit to 0V~12V			250	mA
Output short-circuit current, short-circuit to low	I_{OSD2}	short-circuit to -7V~0V	-250			mA

(Unless otherwise noted, T_A=-40℃~125℃，T_A=25℃，VCC=5V).

NOTE1：ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.

RECEIVER DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input current (A, B)	I_{IN2}	DE=0V, VCC=0 or 5V, V_{IN}=12V		500	1000	μA
		DE=0V, VCC=0 or 5V, V_{IN}=-7V	-800	-300		μA
Positive input threshold voltage	V_{IT+}	-7V≤V_{CM}≤12V			-10	mV
Reverse input threshold voltage	V_{IT-}	-7V≤V_{CM}≤12V	-200			mV
Input hysteresis voltage	V_{hys}	-7V≤V_{CM}≤12V	10	30		mV

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Receiver Output High Voltage	V_{OH}	I_{OUT}=−2.5mA, V_{ID}=+200mV	VCC-1.5			V
Receiver Output Low Voltage	V_{OL}	I_{OUT}=+2.5mA, V_{ID}=-200mV			0.4	V
Three-State Output Current at Receiver	I_{OZR}	0.4V<V_O<2.4V			±1	μA
Receiver Input Resistance	R_{IN}	-7V≤V_{CM}≤12V	12			kΩ
Receiver Short-Circuit Output Current	I_{OSR}	0 V≤V_O≤VCC	±8		±90	mA

(Unless otherwise noted, T_A=-40℃~125℃，T_A=25℃，VCC=5V).

SUPPLY CURRENT

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current	I_{CC1}	/RE=0V, DE=0V, VCC=3.3V		240	650	μA
		/RE=0V, DE=0V, VCC=5V		270	750	μA
	I_{CC2}	/RE=VCC, DE=VCC, VCC=3.3V		360	650	μA
		/RE=0V, DE=0V, VCC=5V		400	750	μA
Shutdown current	I_{SHDN}	/RE=VCC, DE=0V, VCC=3.3V		0.2	10	μA
		/RE=VCC, DE=0V, VCC=5V		0.2	10	μA

DRIVER SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Driver differential Output delay	t_{DD}	R_L=60Ω, C_L=100pF Fig 3 & Fig 4		15	32	ns
Driver differential output Transition time	t_{TD}			9	20	ns
Drive propagation delay From low to high	t_{PLH}	R_L=27Ω, Fig 3 & Fig 4		18	40	ns
Drive propagation delay From high to low	t_{PHL}			18	40	ns

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
$\|t_{PLH}-t_{PHL}\|$	t_{PDS}			2	6	ns
Driver Enable to Output High	t_{PZH}	R_L=110Ω, Fig 5 & Fig 6		16	45	ns
Driver Enable to Output low	t_{PZL}			16	45	ns
Driver Disable Time from Low	t_{PLZ}	R_L=110Ω, Fig 5 & Fig 6		22	85	ns
Driver Disable Time from high	t_{PHZ}			22	85	ns
In Shutdown mode, Enable to Output High	t_{PSH}	R_L=110Ω, Fig 5 & Fig 6		20	100	ns
In Shutdown mode, Enable to Output low	t_{PSL}	R_L=110Ω, Fig 5 & Fig 6		20	100	ns

RECEIVER SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Receiver Input to output from low to high	t_{RPLH}	C_L=15pF Fig 7 & Fig 8		35	60	ns
Receiver Input to output from high to low	t_{RPHL}			35	60	ns
$\|t_{RPLH} - t_{RPHL}\|$	t_{RPDS}			3	8	ns
Receiver Enable to Output Low	t_{RPZL}	C_L=15pF Fig 7 & Fig 8		16	30	ns
Receiver Enable to Output high	t_{RPZH}	C_L=15pF Fig 7 & Fig 8		16	30	ns
Receiver Disable Time from Low	t_{RPLZ}	C_L=15pF Fig 7 & Fig 8		30	50	ns
Receiver Disable Time from high	t_{RPHZ}	C_L=15pF Fig 7 & Fig 8		30	50	ns
In Shutdown mode, Enable to Output High	t_{RPSH}	C_L=15pF Fig 7 & Fig 8		150	500	ns
In Shutdown mode, Enable to Output low	t_{RPSL}	C_L=15pF Fig 7 & Fig 8		150	500	ns
Time to Shutdown	t_{SHDN}	NOTE2	50		300	ns

NOTE2: If the enable inputs are RE=high and DE=low for less than 50ns, the device is guaranteed not to enter shutdown. If the enable inputs are in this state for at least 300ns, the device is guaranteed to have entered shutdown.

FUNCTION TABLE

Driver Function

CONTROL		INPUT	OUTPUT	
/RE	DE	DI	A	B
X	1	1	H	L
X	1	0	L	H
0	0	X	Z	Z
1	0	X	Z(shutdown)	
X=irrelevant; Z=high impedance				

Receiver Function

CONTROL		INPUT	OUTPUT
/RE	DE	A-B	RO
0	X	≥-10mV	H
0	X	≤-200mV	L
0	X	Open/short circuit	H
1	X	X	Z
X=irrelevant; Z=high impedance			

TEST CIRCUIT

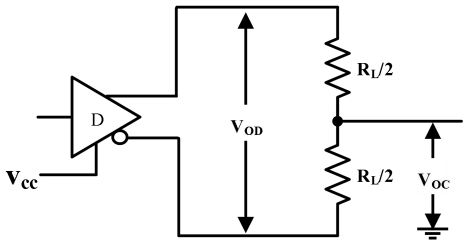
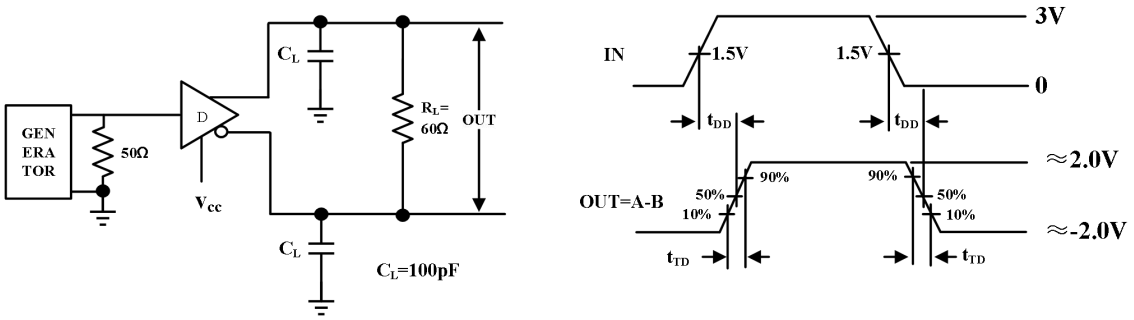


Fig 2 Driver DC test load



CL includes probe and stray capacitance (the same below)

Fig 3 Differential delay and transit time of driver

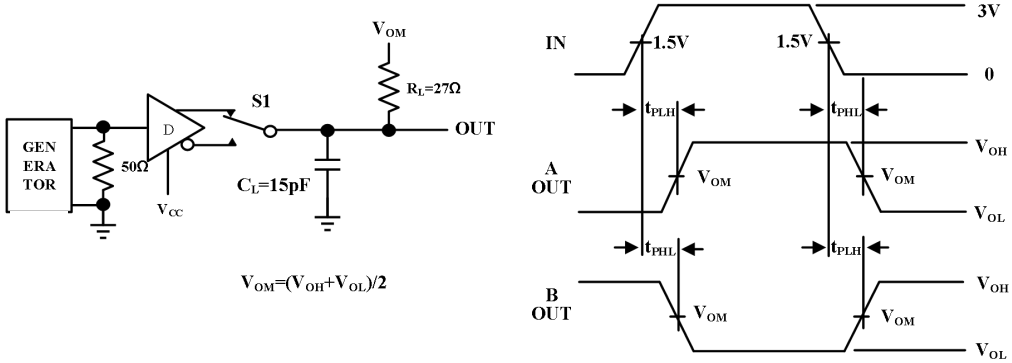


Fig 4 Drive propagation delay

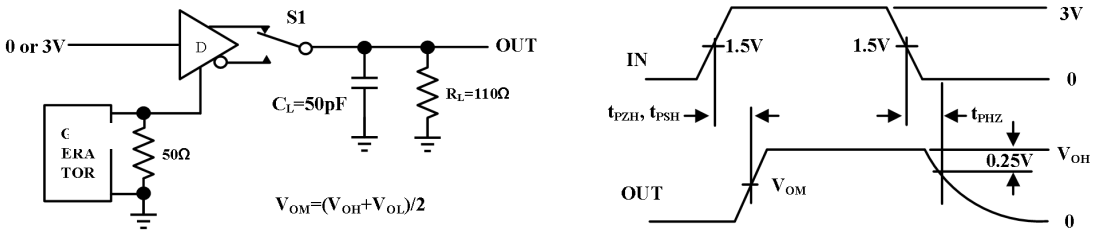


Fig 5 Drive enable and disable time

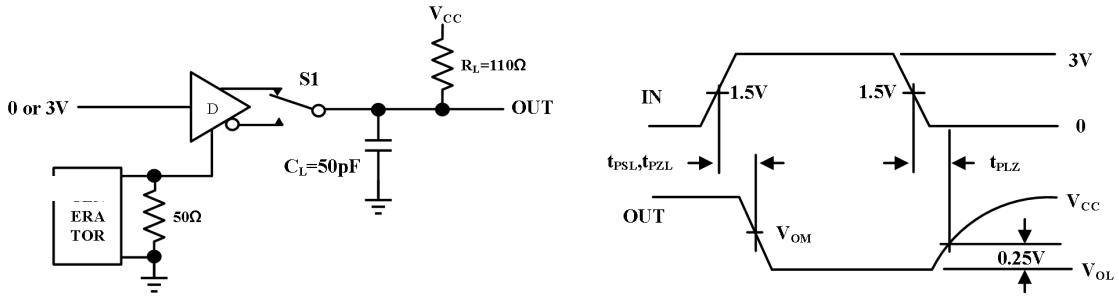


Fig 6 Drive enable and disable time

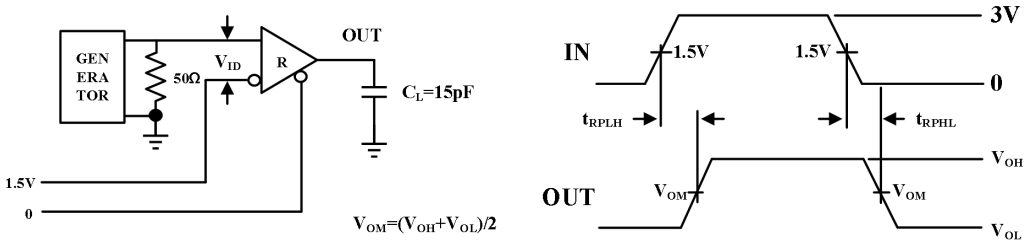
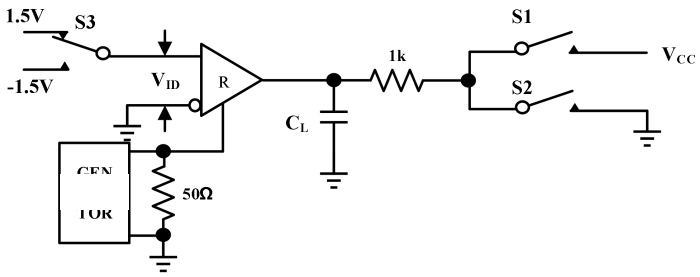


Fig7 Receiver propagation delay test circuit



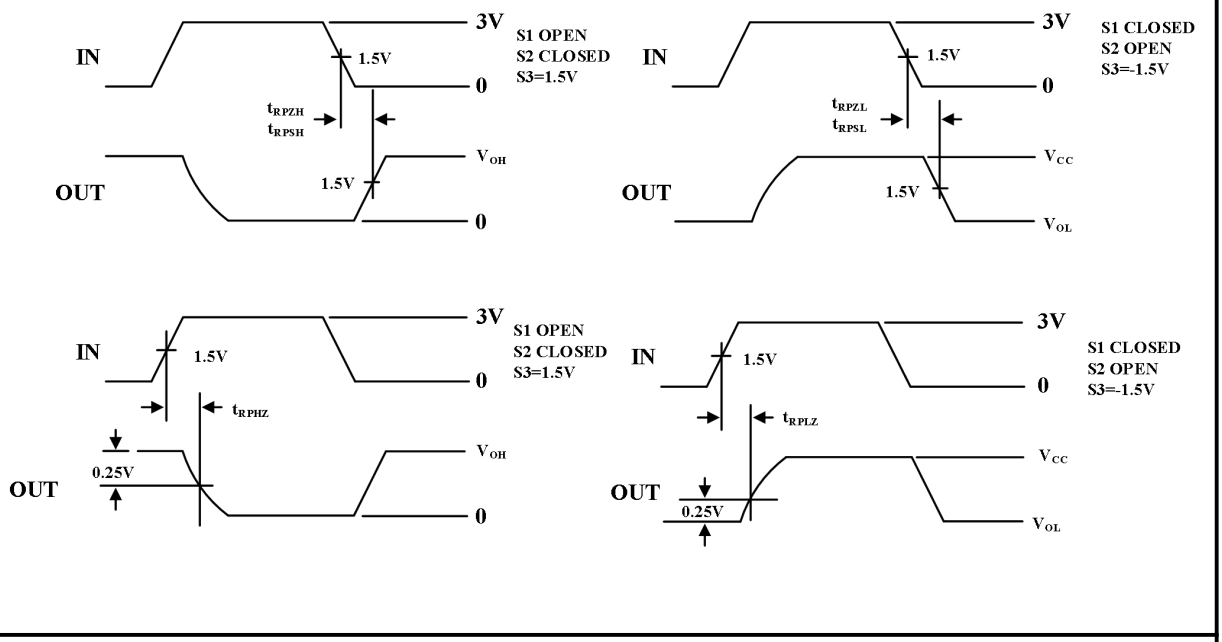


Fig 8 Receiver enable and disable time

ADDITIONAL DESCRIPTION

1 Sketch

SIT65HVD75 is a half-duplex high-speed transceiver with 3.0V~5.5V wide power supply, bus port ESD protection capacity of more than ±15kV HBM, bus DC withstand voltage of more than ±15V, used for RS-485/RS-422 communication, including a driver and receiver. It has the functions of fail-safe, over-voltage protection and over-current protection. SIT65HVD75 realizes error-free data transmission up to 20Mbps.

2 Driver output protection

Overcurrent and overvoltage protection mechanisms are used to prevent excessive output current and power consumption caused by faults or bus conflicts. Fast short-circuit protection is provided throughout the common mode voltage range (refer to typical operating characteristics).

3 Typical Applications

3.1 Bus Networking: SIT65HVD75 RS485 transceiver is designed for bidirectional data communication on multi-point bus transmission line. Fig 9 shows a typical network application circuit. These devices can also be used as linear repeaters with cables longer than 4000 feet. In order to reduce reflection, terminal matching should be carried out at both ends of the transmission line with its characteristic impedance, and the length of branch lines outside the main line should be as short as possible.

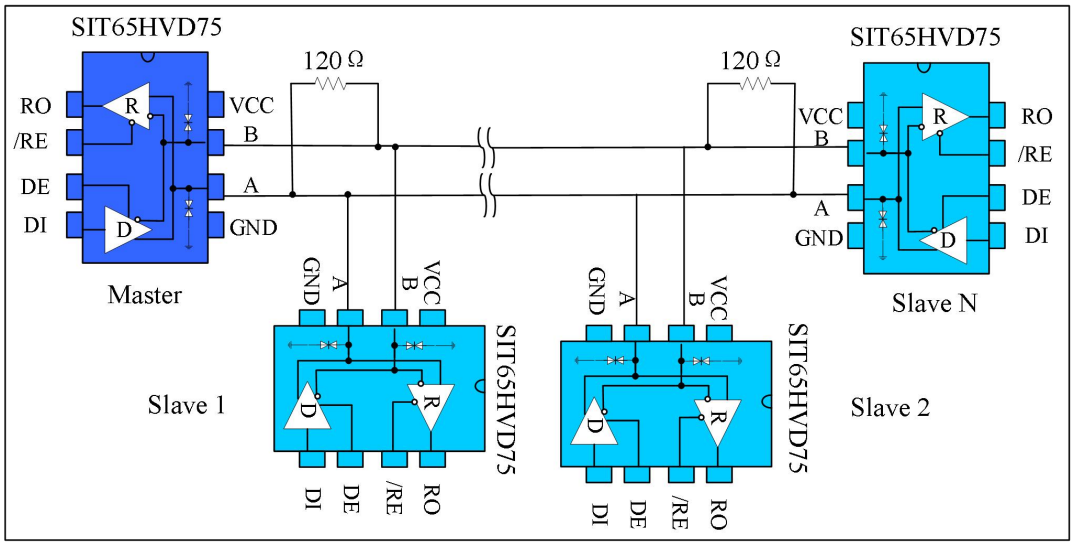


Fig 9 Bus type RS485 half-duplex communication network

3.2 Hand in hand Networking: also known as daisy chain topology, is the standard and specification of RS485 bus wiring, and is the RS485 bus topology recommended by TIA and other organizations. The wiring mode is that the main control equipment and a plurality of slave control equipment form a hand-held connection mode, as shown in Fig 10, and the hand-held mode is no branches. This wiring mode has the advantages of small signal reflection and high communication success rate.

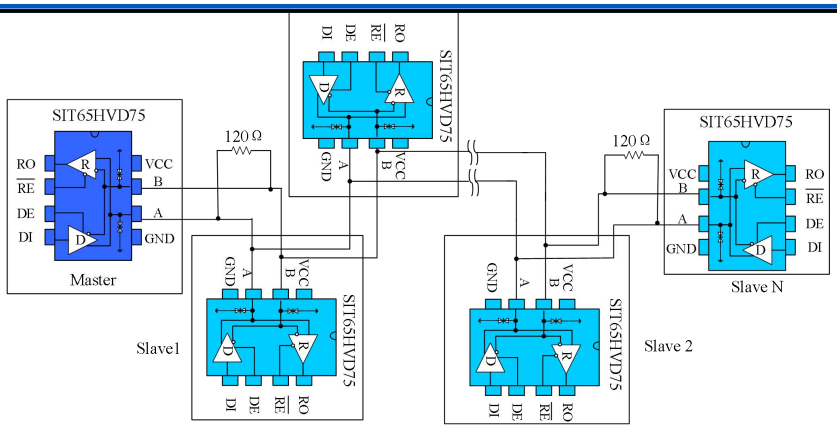


Fig10 Hand in hand RS485 half-duplex communication network

3.3 Bus port protection: in severe environment, RS485 communication port is usually provided with electrostatic protection, lightning surge protection and other additional protection, and even the plan to prevent 380V market electricity access is needed to avoid the damage of intelligent instrument and industrial control host. Fig11 shows three common RS485 bus port protection schemes. The first is the scheme of three-level protection by connecting TVS devices in parallel with A, B port to the protective ground, TVS devices in parallel with A, B port, thermistor in series with A,B port, gas discharge tube in parallel to the protective ground; the second is the scheme of three-level protection by connecting TVS in parallel with A, B port to the ground, thermistor in series with A, B port, and varistor in parallel with A, B port; the third is the scheme of three-level protection by connecting AB with pull-up or pull-down resistor to power and ground respectively, connecting TVS between A & B, A or B port connecting thermistor.

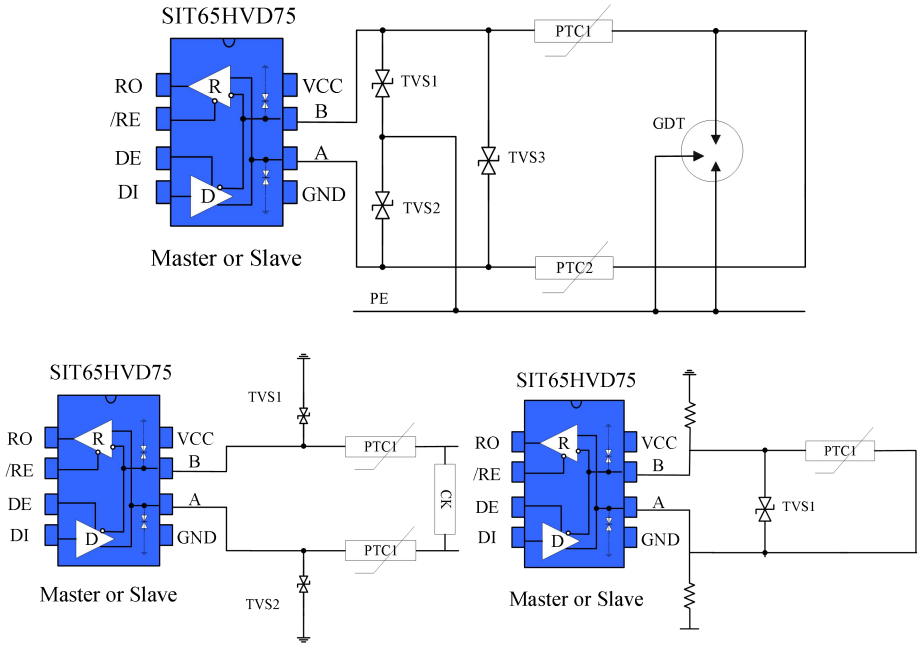
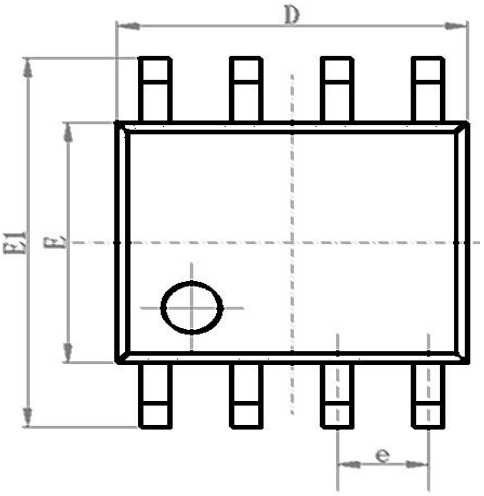


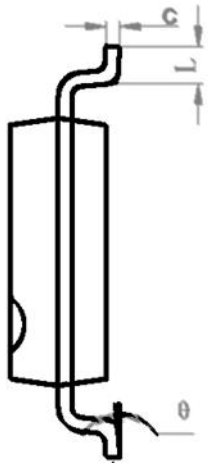
Fig 11 Port protection scheme

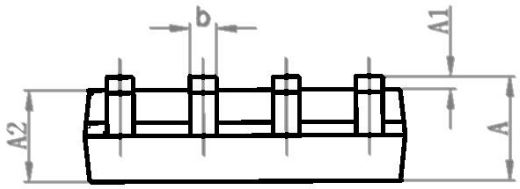
SOP8 DIMENSIONS

PACKAGE SIZE

SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	1.50	1.60	1.70
A1	0.1	0.15	0.2
A2	1.35	1.45	1.55
b	0.355	0.400	0.455
D	4.800	4.900	5.00
E	3.780	3.880	3.980
E1	5.800	6.000	6.200
e		1.270BSC	
L	0.40	0.60	0.80
c	0.153	0.203	0.253
θ	-2°	-4°	-6°



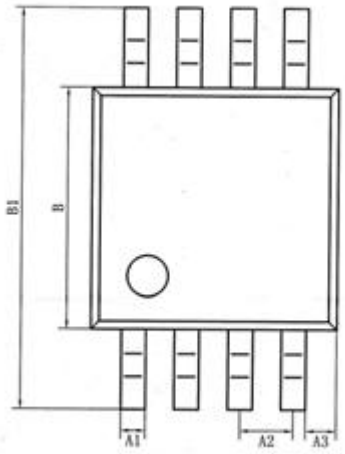


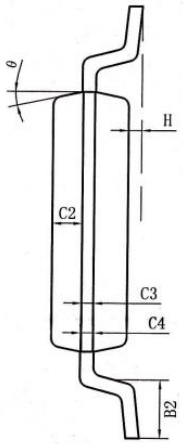


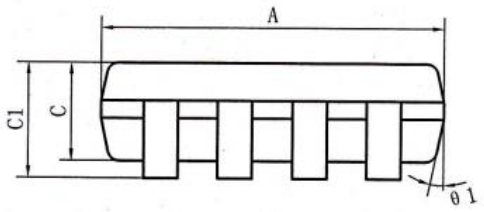
MSOP8/8μMAX/VSSOP8 DIMENSIONS

PACKAGE SIZE

SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	2.90	3.0	3.10
A1	0.28		0.35
A2	0.65TYP		
A3	0.375TYP		
B	2.90	3.0	3.10
B1	4.70		5.10
B2	0.45		0.75
C	0.75		0.95
C1			1.10
C2	0.328 TYP		
C3	0.152		
C4	0.15		0.23
H	0.00		0.09
θ	12°TYP		



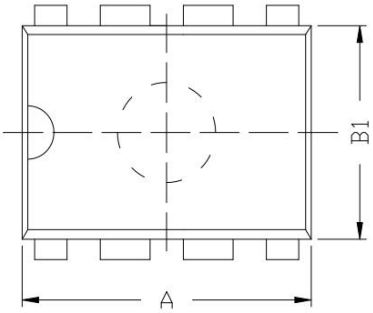


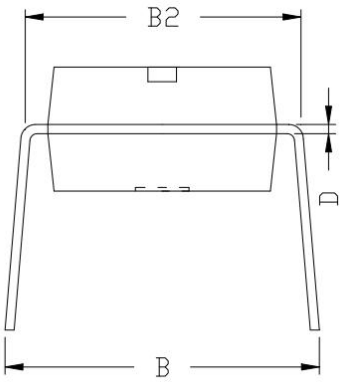


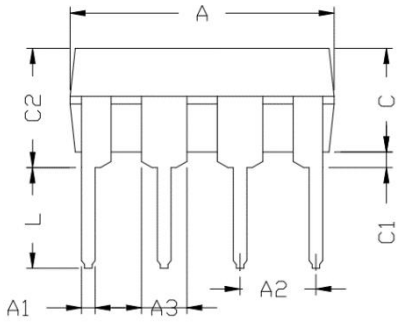
DIP8 DIMENSIONS

PACKAGE SIZE

SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	9.00	9.20	9.40
A1	0.33	0.45	0.51
A2		2.54TYP	
A3		1.525TYP	
B	8.40	8.70	9.10
B1	6.20	6.40	6.60
B2	7.32	7.62	7.92
C	3.20	3.40	3.60
C1	0.50	0.60	0.80
C2	3.71	4.00	4.31
D	0.20	0.28	0.36
L	3.00	3.30	3.60



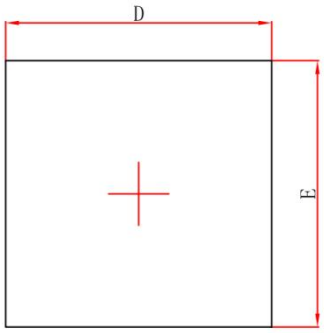


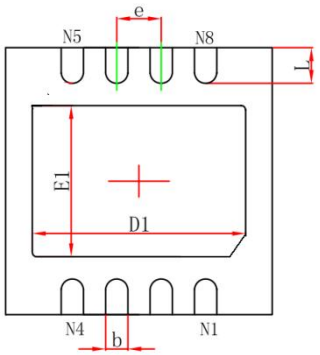


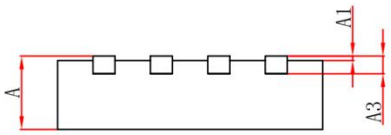
DFN3*3-8 DIMENSIONS

PACKAGE SIZE

SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	0.700		0.900
A1	0.000	0.02	0.050
A3	0.203 REF		
D	2.900	3.000	3.100
E	2.900	3.000	3.100
D1	2.200	2.3	2.400
E1	1.400	1.5	1.600
b	0.2	0.25	0.33
e	0.65 TYP		
L	0.250		0.575



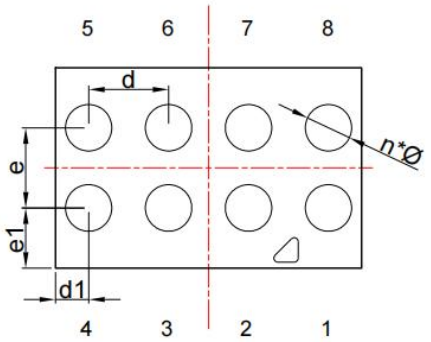


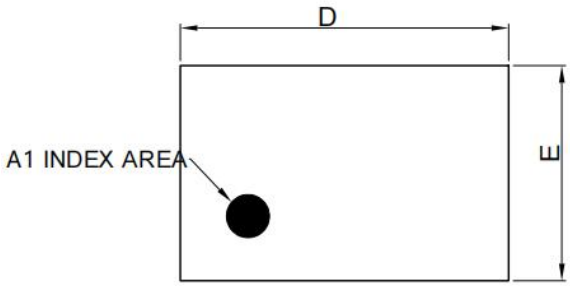


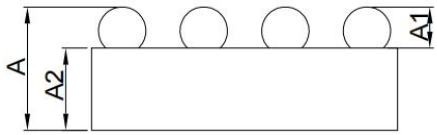
BGA DIMENSIONS

PACKAGE SIZE

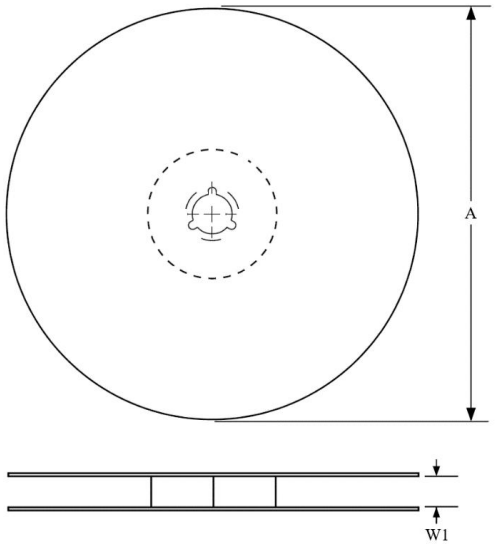
SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	0.535	0.600	0.665
A1	0.175	0.200	0.225
A2	0.367	0.400	0.433
⌀	0.207	0.232	0.257
D	1.505	1.530	1.555
E	0.975	1.000	1.025
d	0.400		
e	0.400		
d1	0.165		
e1	0.300		
n	8		



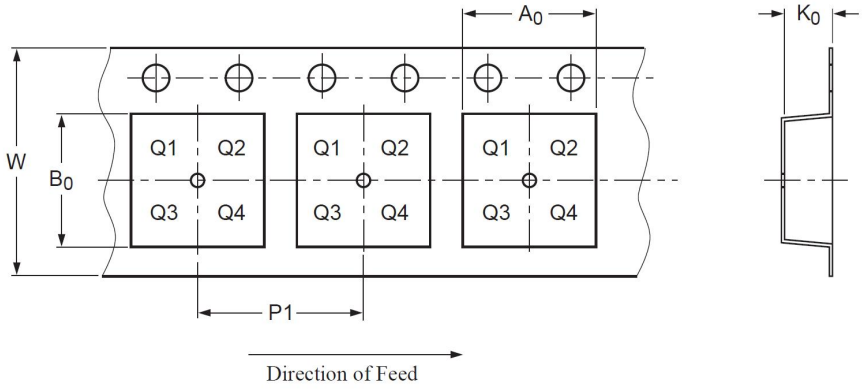




TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



PIN1 is in quadrant 1

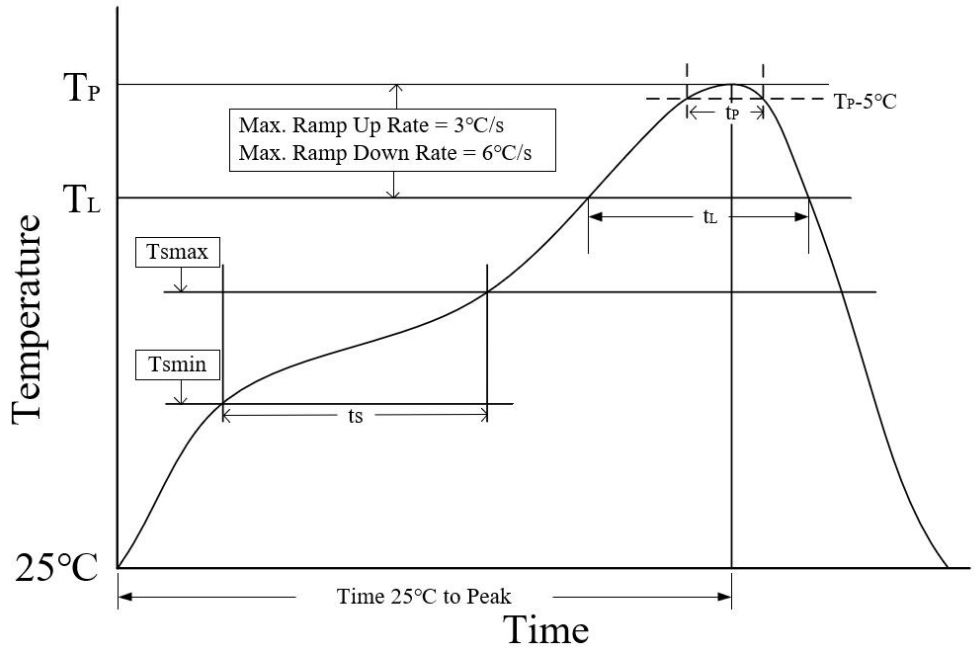
Package Type	Reel Diameter A (mm)	Tape width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
SOP8	330	12.5±0.20	6.50±0.1	5.30±0.10	2.05±0.1	8.00±0.1	12.00±0.1
MSOP8	330	12.5±0.20	5.33±0.10	3.40±0.10	1.53±0.10	8.00±0.10	$12.00^{+0.30}_{-0.10}$
DFN3*3-8	330	12.5±0.20	3.30±0.10	3.30±0.10	1.10±0.1	8.00±0.10	$12.00^{+0.30}_{-0.10}$
BGA	330±2	8.4^{+2}_{-0}	1.15±0.05	1.74±0.05	0.72±0.05	4.00±0.10	$8.00^{+0.30}_{-0.10}$

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	PACKING
SIT65HVD75DR	SOP8	Tape and reel
SIT65HVD75DGK	MSOP8/VSSOP8/8μMAX	Tape and reel
SIT65HVD75P	DIP8	Tube
SIT65HVD75ETK	DFN3*3-8	Tape and reel
SIT65HVD75C	BGA	Tape and reel

SOP8 and MSOP8/VSSOP8/8μMAX are packed with 2500 pieces/disc in braided packaging. DFN3*3-8 is packed with 5000 pieces/disc in braided packaging. BGA is packed with 3000 pieces/disc in braided packaging. DIP8 is packed with 50 pieces/tube in tubed packaging.

REFLOW SOLDERING



Parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	3°C/second max
Preheat time ts (T_{smin}=150°C to T_{smax}=200°C)	60-120 seconds
Melting time t_L (T_L=217°C)	60-150 seconds
Peak temp T_P	260-265°C
5°C below peak temperature t_P	30 seconds
Ave cooling rate (T_P to T_L)	6°C/second max
Normal temperature 25°C to peak temperature T_P time	8 minutes max

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Datasheet status	Revision date
V1.0	Initial version.	April 2020
V1.1	Updated R_{IN} minimum; Updated test circuit; Added tape and reel information; Updated ordering information; Added reflow soldering; Added important statement; Added revision history.	February 2023
V1.2	Added SIT65HVD75C.	April 2026
V1.3	Updated SIT65HVD75C's pin diagram; Update packing quantity parameter of BGA package.	September 2026